



Addis Ababa University  
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Department of Electrical and Computer Engineering

**INVESTIGATION OF VSC-HVDC SYSTEM FOR DYNAMIC  
PERFORMANCE IMPROVEMENT OF  
EPCO HIGH VOLTAGE GRID**

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## ACRONYMS

AC	Alternate Current
DC	Direct Current
DIgSILENT	Digital Simulation and Electrical Network calculation program
EETPCo	Ethiopian Electric Power Corporation
FACTS	Flexible Alternating Current Transmission Systems
HVAC	High Voltage Alternate Current
HVDC	High Voltage Direct Current
ICS	Interconnected System
IGBT	Insulated Gate Bipolar Transistor
kEUR	Thousands of European Currency Unit
kV	kilo Volt
LCC	Line Commutated Converter
MVA	Mega Volt Ampere
PI	Proportional plus Integral
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
STATCOM	Static Synchronous Compensator
TSO	Transmission System Operator
VSC	Voltage Source Converter

# TABLE OF CONTENT

ACKNOWLEDGEMENT .....	ii
ACRONYMS.....	iii
LIST OF TABLES.....	vii
LIST OF FIGURES .....	viii
LIST OF APPENDICES.....	x
ABSTRACT.....	xi
CHAPTER 1. INTRODUCTION .....	1
1.1    Background.....	1
1.2    Statement of the Problem.....	3
1.3    Objectives of the Study.....	4
1.4    Thesis Outline .....	4
CHAPTER 2. LITERATURE REVEIW .....	6
2.1    Power System Dynamic Performance Analysis .....	6
2.2    Power System Stability Improvement Strategies.....	7
2.2.1    Flexible Alternating Current Transmission Systems (FACTS).....	9
2.2.2    HVDC as stability improvement tool .....	9
2.3    Related Research Works .....	10
2.4    High Voltage DC Transmission Overview .....	11
2.4.1    HVDC transmission technologies.....	12
2.4.2    HVDC transmission schemes .....	13
2.5    The VSC-HVDC System.....	14
2.5.1    Converters .....	15
2.5.2    Phase reactors .....	17
2.5.3    Transformers.....	17

2.5.4	DC operating voltage .....	18
2.5.5	DC capacitor .....	18
2.5.6	Shunt filters.....	19
2.6	VSC-HVDC Principle of Operation .....	20
2.7	Pulse Width Modulation (PWM).....	22
2.8	Capability Curve of VSC-HVDC .....	24
2.9	Economics of VSC-HVDC Transmission .....	25
<b>CHAPTER 3. CONTROL OF VSC-HVDC SYSTEM.....</b>		<b>27</b>
3.1	Introduction.....	27
3.2	Current Vector Control .....	28
3.3	VSC-HVDC Mathematical Modeling .....	29
3.4	The Inner Current Control Loop.....	33
3.4.1	PI regulator .....	33
3.4.2	PWM converter.....	34
3.4.3	System transfer equation.....	34
3.4.4	Tuning the current controller .....	37
3.5	Outer Controllers .....	39
3.5.1	PQ-controllers.....	40
3.5.2	DC-voltage controller .....	40
3.5.3	Tuning the DC voltage controller .....	42
<b>CHAPTER 4. SIMULATION STUDIES.....</b>		<b>44</b>
4.1	Testing the Control System.....	44
4.1.1	Active power flow direction reversal.....	46
4.1.2	Reactive power control .....	48
4.1.3	DC voltage step responses .....	49
4.1.4	Three phase to ground fault at VSC-1 Bus and VSC-2 Bus.....	51
4.2	VSC-HVDC Integration to North-Western EEP Co System.....	54
4.3	Simulation Results .....	55
4.3.1	The effect of clearance time on the post disturbance voltage profile .....	56

4.3.2	Post disturbance voltage profile and rotor angle stability with VSC-HVDC integration .....	57
4.3.3	Post disturbance bus voltage profile of the over all system` .....	60
4. 3.4	AC-DC grid operation at half load and average load .....	65
CHAPTER 5. CONTRIBUTIONS, CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK .....		68
5.1	Conclusions.....	68
5.2	Recommendation.. .....	69
5.2	Suggestions for Future Works .....	69
REFERENCES .....		70
APPENDICES .....		74

## LIST OF TABLES

Table 2.1: Average investment cost of transmission system technologies [39] .....	26
Table 4.1: Test system Parameters .....	45
Table A.1: Transmission line data .....	74
Table A.2 load data.....	74
Table A.3: Generator data from ARIVA [37] with some assumptions .....	75
Table A.4: Governor Data of the generators from ARIVA [37] with some assumptions	75



## LIST OF FIGURES

Figure 1.1: EEPCo generation expansion in MW.....	2
Figure 2.1: Power system stability improvement strategies .....	8
Figure 2.2: HVDC configuration schemes: a) Back-to-back b) Monopolar c) Bipolar ...	14
Figure 2.3: The VSC-HVDC basic system.....	15
Figure 2.4: Three-phase two level converter topology and produced wave form .....	16
Figure 2.5: Three-phase three-level converter topology and produced wave form.....	16
Figure 2.6: Circuit diagram of VSC-HVDC converter station .....	20
Figure 2.7: Active and reactive power flow control of VSC-HVDC .....	22
Figure 2.8: Sinusoidal PWM based on triangular carrier signal [32] .....	24
Figure 2.9: Capability curve of VSC-HVDC.....	25
Figure 3.1: Control block diagram depicting how the errors are generated and how the outer controllers feed the inners.....	29
Figure 3.2: Equivalent circuit of VSC station.....	29
Figure 3.3: The inner current control loop set up .....	33
Figure 3.4: The inner current control loops with the compensation terms .....	36
Figure 3.5: Reduced form of the inner current control loop.....	37
Figure 3.6: Step response of the inner current control loop with the designed current controller .....	39
Figure 3.7: The PQ-controllers .....	40
Figure 3.8: Block diagram representation of the DC voltage control loop.....	41
Figure 3.9: Step response of the designed DC voltage control loop.....	43
Figure 4.1: The controller test system .....	44
Figure 4.2: Transients at active power reversal .....	47
Figure 4.3: Responses for the step change of reference reactive power.....	49
Figure 4.4: Transients at step change in $V_{dc\_ref}$ .....	50
Figure 4.5: Transient response of the system for 3-phase to ground fault at VSC-1 bus .	51
Figure 4.6: Transient response of the system for 3-phase to ground fault at VSC-2 bus .	53

Figure 4.7: DIgSILENT model of the North-Western and Northern EEPCo system with VSC-HVDC .....	54
Figure 4.8: The effect of clearance time on post disturbance voltage profiles .....	56
Figure 4.9: Voltage profile improvement at Mota 230 kV bus .....	57
Figure 4.10: Bus voltage dynamics of Debre Markos 230 kV .....	58
Figure 4.11: Tis abay II and Tekeze generator rotor angle oscillations .....	60
Figure 4.12: Bus voltage dynamics with and with out VSC-HVDC for a fault at Mekele 230kV bus.....	61
Figure 4.13: Bus voltage dynamics with and with out VSC-HVDC for a fault at Bahir Dar II 230kV bus.....	62
Figure 4.14: Bus voltage dynamics with and with out VSC-HVDC for a fault at one of the double line from Tis Abay II to Bahir Dar II.....	63
Figure 4.15: Bus voltage dynamics with and with out VSC-HVDC for a fault at Mota 230kV bus.....	64
Figure 4.16 Bahir Dar II 132 kV bus voltage profile at different system load.....	65
Figure 4.17 Bus voltage profile control through reactive power compensation.....	66
Figure 4.18 Tis abay II 132kV and Mekele 230 kV bus voltage profiles upon reactive power compensation .....	67

## LIST OF APPENDICES

Appendix A: Northern and North-Western EEPCo model system Data .....	74
Appendix B: DIgSILENT implementation of the controllers .....	76
Appendix C: Controller equations, initial condition codes and block status checks on DIgSILENT .....	79
Appendix D: Matlab code for step response plot of the designed current controllers and DC voltage controller .....	84

## **ABSTRACT**

The Ethiopian Electric Power Corporation (EEPCO) is, currently, undertaking a huge electric power generation expansion. The generation capacity under construction is about 7757 MW. This huge expansion demands existing AC transmission line upgrading and new transmission line installations. On the other hand, instability problems have occurred frequently within EEPCo system manifesting themselves in the form of system blackouts.

Considering these two problems this thesis work proposes integration of Voltage Source Converter Based High Voltage Direct Current (VSC-HVDC) transmission system for improving future system stability and enhancing power transfer capability.

The thesis investigates the dynamic performance improvements that can be attained through integrating VSC-HVDC transmission system. The investigation started by developing a monopolar VSC-HVDC transmission model with a complete control system on Digital Simulation and Electrical Network calculation program (DIgSILENT power factory) software. Different controllers are designed including, faster inner current controllers having transient response specifications: rise time 0.0003 s, settling time 0.000842 s; DC voltage controller having transient response specifications: rise time 0.00156 s, settling time 0.0132 s; and outer PQ controllers. Then the performance of the control system is evaluated and found to function satisfactorily at supporting bidirectional power flow and at maintaining stability during disturbances. Finally the designed VSC-HVDC link is integrated to North-Western EEPCo high voltage grid model and time domain simulations are carried out to investigate system dynamic performance improvement. It is obtained that with the proposed option the system pre-disturbance bus voltage values are improved from below 0.95 pu to 1 pu and post disturbance bus voltage values are improved from below 0.9 pu to above 0.95 pu. On the other hand system low load higher voltage values that go beyond upper limit of 1.05 are managed to come within the limit. A better damping of generators' rotor angle oscillations is also attained showing general system dynamic performance improvement.

**KEY WORDS:** Dynamic performance improvement, VSC-HVDC, Vector Control, North-Western EEPCo, bus voltage profiles.

# CHAPTER 1

## INTRODUCTION

### 1.1 Background

Electric power system is the system of equipments and controls dedicated for the generation, transmission and consumption of electrical power. Electrical energy is the most suitable form of energy for transportation and distribution. Due to this important behavior it is being intensively utilized as a means of energy transfer. This in turn resulted the appearance of huge electric power transmission systems. Electric power transmission systems play the role of transporting electrical energy for a wide range of distances ranging from few kilometers up to hundreds even thousands of kilometers. They connect energy generating parts and energy consuming parts of a power system. These transmission systems operate under carefully designed and controlled conditions in order to achieve the energy transmission tasks.

Today increased energy demands resulted in intensive power system growths. The growth makes power systems to get wider in coverage and get complex in interconnection. This situation gives rise to the complexity of stability problems. Keeping the power system stability and improving the power transfer capability of power systems is an issue that must be dealt at the expansion planning stage of power systems.

In Ethiopia the energy demand is, currently, doubling in every three year [1]. Due to this the Ethiopian federal government is now undertaking extensive generation and transmission system expansions. Gilgel Gibe III, Chemoga-Yeda, Amertinesh, Ashegoda ( wind farm ), and the Grand Millennium ( Heddasié ) hydro power generating plant projects are expected to come to the power system up to 2017. The planned power generation expansions under different stages are shown in figure 1.1. The transmission system expansions are also under way. These include: Bedele–Metu 132 kV line, Alemata-Combolcha-Cotebie-Kaliti 230 kV line, Combolcha-Semera-Dichoto 132 kV line, BahirDar-Debremarkos-Sululta 400 kV line. A 132 kV double line is under construction from Dire Dawa to Djibouti, and another 132 kV line is also under construction from Metema to Sudan. Feasibility studies to connect Ethiopia with Kenya through HVDC are being under taken [2, 3].

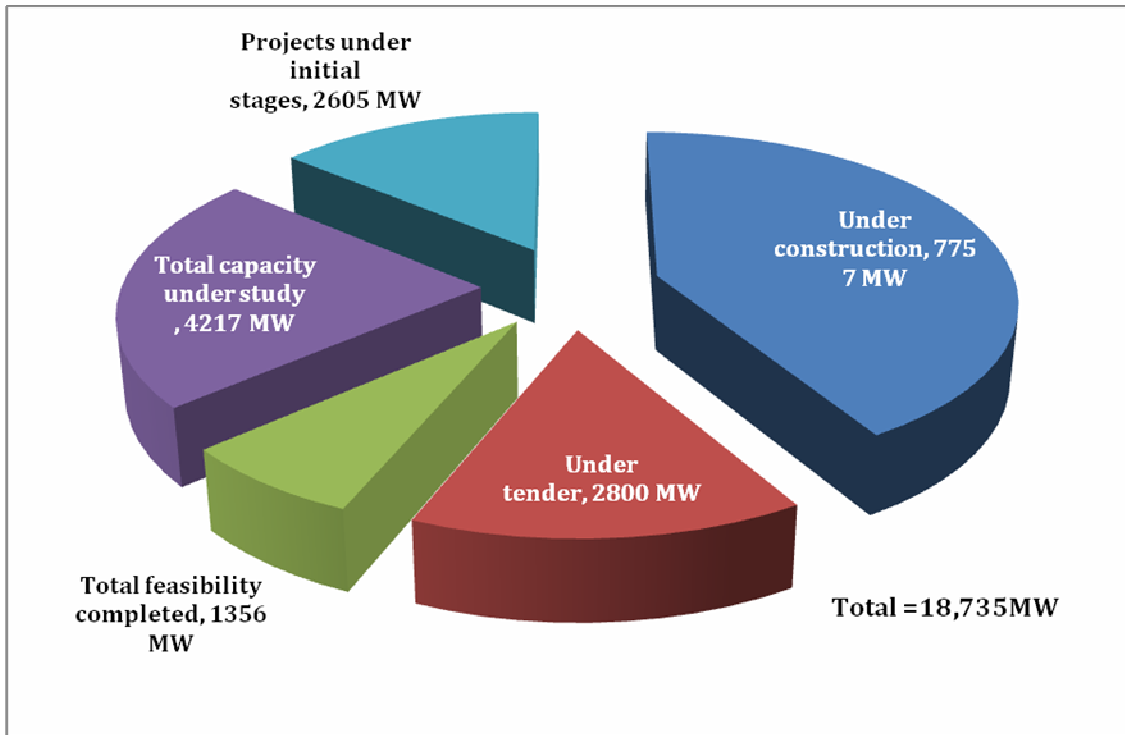


Figure 1.1: EEPCo generation expansion in MW

Currently, due to the boosting of electric power generation at EEPCo system particularly at the North-Western EEPCo system, it is found necessary to install new transmission lines and to revise the existing transmission systems. Tasks that have to be done with the existing transmission lines include line upgradings and replacements. With regard to improvements that have to be done with the transmission system, this thesis is a design recommendation to the upcoming EEPCo transmission system so as to utilize HVDC transmission based on voltage source converters (VSC) to improve the dynamic performance of the system and to increase power transfer capability of the whole system.

HVDC transmission based on voltage source converters (VSC) is a very promising solution for the improvement of power systems stability and improving the over all power transfer capability. When VSC-HVDC transmission system is integrated to AC grids reactive power is controlled at the end terminals independent of one another. This reactive power control is essential for dynamic system voltage regulation following contingencies.

Through the application of HVDC system based on voltage source converter (VSC), both active power transmission as well as grid reactive power support tasks, which are the future EEPCo system requirements can be achieved. Hence, the purpose of installing VSC-HVDC can not only be stability issue but also a transmission medium provision for controlled active power flow.

The integration of VSC-HVDC to the EEPCo system can be done in two possible ways. The first is through network restructuring by replacing old, stressed lines and the other is to make future expansions through the proposed design option. This thesis investigates the first application option and done by replacing the already existing Mota-Debre Markos transmission line. This strategy benefits the over all power system by improving voltage profiles to North, North-Western as well as central inter connected EEPCo system (ICS). Secondly it greatly enhances the power transmission capability of the newly coming Bahir Dar-Debre markos-Sululta 400 kV AC transmission line and many upcoming expansions in the area. This will reduce the number of future new AC line installations by operating few transmission lines up to their thermal limits.

### **1.2 Statement of the Problem**

Many blackout events have been registered in the Ethiopian electric power system, in the past four years. According to the blackout reports collected from National Grid Control Center, it has been registered 8 significant blackouts from 2007 to 2010. Among these, the primary reason for blackout of November 30/2007 was reported as voltage stability problem. This situation shows that the reactive power provision and control within the system is poor.

On the other hand EEPCo is now undertaking huge electric power generation and transmission expansions. The North-Western part of the EEPCo system is the first and the significant center of system expansion. The existing Beles hydro power plant and the upcoming Grand Millennium (Heddasie) and Chemoga-Yeda hydro power plants together with Tis Abay II hydro power plant will make the area to take more than 50% share of future power generation. This will force to upgrade the existing transmission systems and make new installations in this area.

The upcoming expansions will have their own impact on the stability of the system depending on the studies made at expansion planning stage and type of technology used. Therefore, it is necessary to consider design solutions that maintain the future system stability thereby increasing the existing system transfer capability.

On this respect, this thesis investigates the integration of VSC-HVDC transmission so as to improve the existing as well as the upcoming EEPCo system dynamic performance.

### **1.3 Objectives of the Study**

The primary objective of this research work is to investigate the advantages of integrating VSC-HVDC transmission system in the Ethiopian electric power system for improving the dynamic performance of the system and enhance transmission capability. As a specific objective it targeted at:

- Developing monopolar VSC-HVDC transmission test system model on DIgSILENT software.
- Developing and implementing control system for VSC-HVDC transmission model on the DIgSILENT software.
- Testing the performance of the developed control system.
- Modeling Northern and North-Western part of the EEPCo power system.
- Carrying out time domain simulations with and without VSC-HVDC transmission scheme and show system dynamic performance improvement under various disturbance scenarios.
- Assessing the dynamic performance of Northern and North-Western EEPCo's power system with VSC-HVDC.

### **1.4 Thesis Outline**

This thesis is organized into five chapters and four appendices.



Chapter-1 is an introductory part giving a background of the study. The basic problem is described here. Finally, the objectives of the thesis work are described.

Chapter-2 deals with the basic definition of power system dynamics and importance of power system dynamic performance analysis, power system dynamics improvement strategies, related research works, HVDC system over view, HVDC transmission schemes, VSC-HVDC system components and design issues as well as VSC-HVDC principle of operation.

Chapter-3 discusses about modeling of VSC-HVDC for the stability studies, developing a complete control system, and tuning of the controllers using suitable tuning techniques.

Chapter-4 contains control system test simulations and discussions, simulation results for various incidences with the VSC-HVDC system integrated to the North-Western EEPCCo system, investigation of the resulting AC-DC system operation under different system loading condition.

Chapter-5 reveals conclusions, recommendations and suggests future works.

## **CHAPTER 2**

### **LITERATURE REVEIW**

In this chapter the basics of power system dynamic performance and the importance of power system dynamic performance analysis is discussed. Different power system dynamic performance improvement strategies are also presented. HVDC system is overviewed and finally VSC-HVDC transmission system components and design issues as well as principle of operation are discussed.

#### **2.1 Power System Dynamic Performance Analysis**

Power system dynamic performance, popularly known as power system stability may be broadly defined as the property of a power system that enables it to remain in a state of operating equilibrium under normal operating conditions and to regain an acceptable state of equilibrium after being subjected to a disturbance [4].

According to the IEEE/ CIGRE joint task force classification power system stability is classified to the following categories [2].

- Rotor angle stability (oscillatory, transient-stability)
- Voltage stability (short-term, long-term, dynamic)
- Frequency stability

Inability to maintain the stability of a power system makes the ability of a power system to transmit power to be impaired. The stability problems are hindrance for effective power transfers within the system. It is therefore necessary to design and operate power systems so that transient events (i.e. probable contingencies), can be withstood without the loss of load or loss of synchronism in the power system [4]. There are different solutions that can improve the stability of power systems so that increased power transfer capability can be achieved.

Dynamic performance analyses are very crucial tools to identify system stability problems and demonstrate the effectiveness of stability improvement solutions [5]. Power system dynamics analysis involves the study of the behavior of a power system under conditions before and after sudden changes in load or generation, during faults and outages. Hence, power system dynamics analysis is an important part of power system operation and planning.

Different simulation software, both commercial and free, are available for carrying out dynamic performance analyses. These include Power System Computer Assisted Design (PSCAD), SimPower, Power System Software for Engineers (PSS/E) and DIgSILENT power factory.

An important part of power system dynamics studies is power system equipment modeling. The type of models of power system equipments employed greatly affects the dynamic analysis. The analysis in this thesis is done on DIgSILENT power factory in order to exploit the accuracy of both AC and DC models.

DIgSILENT power factory is a dedicated electrical power system simulation tool used by the power-system utilities world wide. It has the ability to simulate load flow, RMS simulations and electromagnetic transient events. DIgSILENT has faster simulation time when compared to PSCAD and SimPower systems in MATLAB. In terms of accuracy of the results and implementation of the models, all the software is similar in nature [6]. DIgSILENT provides highly accurate, built in models for generators, loads, transmission lines and other AC/DC system equipments. In this study for system modeling a 5<sup>th</sup> order synchronous generator model, which is described by three electrical and two mechanical equations,  $\pi$ -model of transmission lines, and constant impedance loads are used. Details on models of system elements for stability analysis on DIgSILENT are discussed in [6].

## **2.2 Power System Stability Improvement Strategies**

The stability of power systems depends on the active and reactive power balance between generation and load within the system. Losing this balance leads to loss of system integrity leading to system collapse which has damaging impact on daily economic activities. In order

to avoid such devastating impacts there should be effective mechanism for maintaining this balance [4]. These days different solution mechanisms are continued to be employed by power utilities worldwide for insuring this balance and bring about improved system stability.

Strategies for power system stability improvement are implemented at two levels as shown in the chart in figure 2.1. The first is at generating units through the action of power system stabilizers (PSSs), automatic voltage regulators (AVRs) and other supplementary controllers. The power utilities worldwide are currently implementing PSSs and AVRs as excitation controllers to enhance power system stability. However, due to limited capacity and large system voltage variations introduced during disturbances upon utilizing them, they are getting insufficient to create system wide influences [7]. The other solution group is through the application of FACTS devices and HVDC controls at the transmission level.

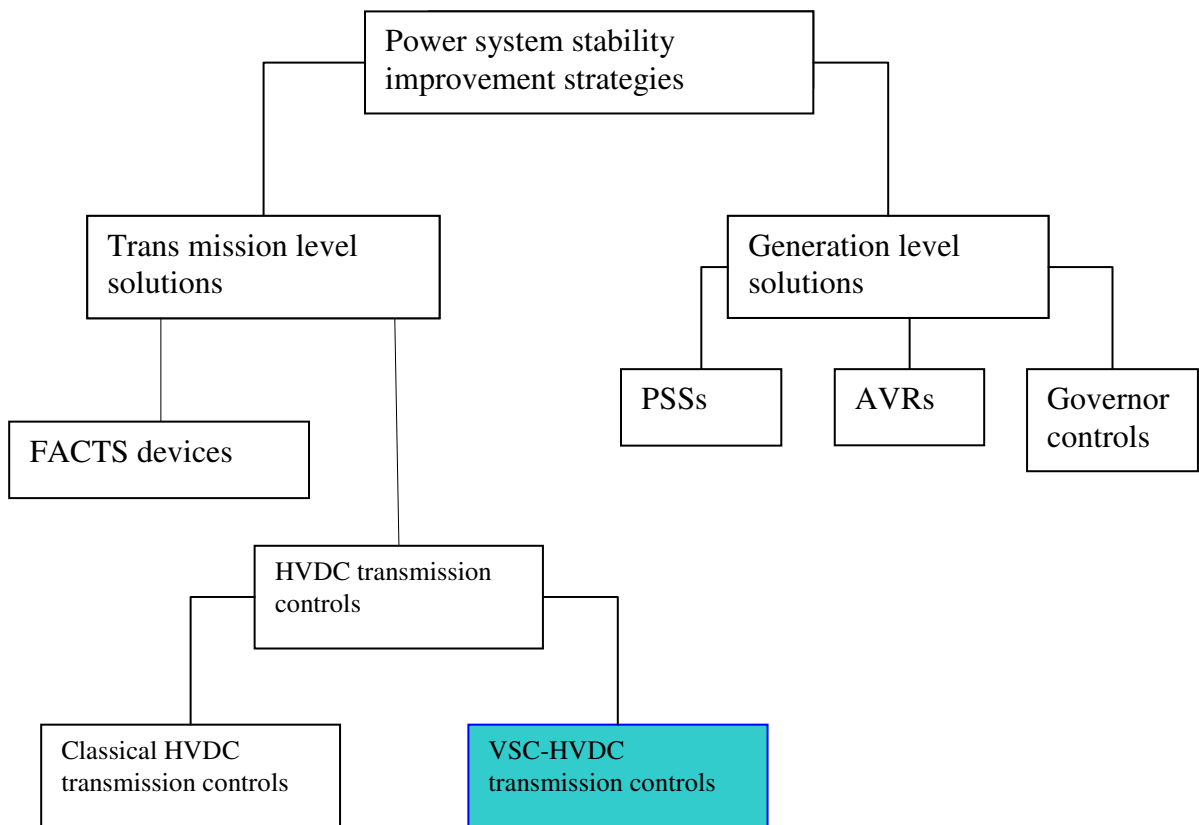


Figure 2.1: Power system stability improvement strategies

Coming to EEPCo system, the mechanisms employed for stability control are generator level AVR controls and manually switched shunt reactors at substations to reduce Ferranti over

voltages and over voltages that arise due to load rejection. However these mechanisms are not sufficient and hence, it can be said that EEPCo system doesn't have effective stability controlling mechanism.

### **2.2.1 Flexible Alternating Current Transmission Systems (FACTS)**

FACTS is defined by the IEEE as a power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability [8].

There are two groups of FACTS devices. The first group employs conventional thyristor-switched capacitors and reactors, and quadrature tap-changing transformers. This includes the Static Var Compensator (SVC), the Thyristor- Controlled Series Capacitor (TCSC), and the Thyristor-Controlled Phase Shifter (TCPS). The second group utilizes gate turn-off (GTO) thyristor-switched converters as voltage source converters (VSCs). This group contains Static Synchronous Compensator (STATCOM), the Static Synchronous Series Compensator (SSSC), the Unified Power Flow Controller (UPFC), and the Interline Power Flow Controller (IPFC) [7].

FACTS devices have been mainly used for solving various power system steady state control problems such as voltage regulation, power flow control, and transfer capability enhancement [9]. As supplementary functions, damping the interarea modes and enhancing power system stability using FACTS controllers have been extensively studied and investigated [10]. These regulatory tasks are accomplished through appropriate reactive power compensation, or by series capacitive compensation of line inductances, or by phase angle shifting.

However it is not found to be cost-effective to install FACTS devices for the sole purpose of power system stability enhancement [7].

### **2.2.2 HVDC as stability improvement tool**

The control system design and operation of HVDC based on line commutated converter (LCC) for power system stability improvement is discussed in detail in [11]. But HVDC based

on line commutated converters have limitations that restricted the range of its application. VSC-HVDC on the other hand provides the power system with many important benefits which greatly improve system stability. The following are advantages of VSC-HVDC over classical HVDC [12].

- Independent Active and reactive power control and power quality control.
- High quality voltage waveform generation, thereby reducing filtering requirements.
- Unlike LCC-HVDC unlimited power reversal.
- Reduced power losses in interconnected AC systems.
- Increased transfer capacity in the existing system.
- Powerful damping control using P and Q simultaneously.
- Fastest restoration after blackouts.

In VSC-HVDC transmission system reactive power is controlled at each terminal independent of one another. This reactive power control can be used for dynamic voltage regulation to support the interconnected AC systems following contingencies. This helps to increase the over all system power transfer levels and improve system dynamic performance [12, 13].

VSC-HVDC can be an attractive option to efficiently and timely relieve network constraints, thus reducing the need for building new HVAC lines. In addition, VSC-HVDC may offer a lower environmental impact and a smaller territorial footprint due to a compact station design. Also, both HVDC and VSC-HVDC offer undergrounding possibilities by using cables as a transmission medium.

### **2.3 Related Research Works**

In [5] the application of SVC for power system dynamic performance improvement is investigated. [7] studied the application of FACTS controllers to improve power system stability. [14] studied optimal placement of STATCOMs to the Ethiopian electric power system to minimize power loss and improve voltage profiles at bus bars. In [15] application of UPFC to improve power transfer capability of Bahirdar-Alamata transmission line is investigated.

In [16] it is investigated how the power electronics based converters, including VSC-HVDC can support the grid and solve grid problems. Application of VSC based compensation for mitigating voltage dip and improving sub synchronous resonance is discussed in [17]. [18, 19] are studied on VSC-HVDC application for wind power integration. One of the attractive applications of the VSC-HVDC is that it can be used to connect a wind farm to an AC grid to solve some potential problems such as voltage flicker [20]. In [21] back-to-back VSC-HVDC based network reinforcement to alleviate network constraints that occur at the planning stage is studied. VSC-HVDC application for power supply to industrial systems is studied in [22]. In [23] the application of VSC-HVDC to damp out subsynchronous oscillations is studied. In [24] it is studied the VSC-HVDC application for long term voltage stability improvement. In [25] the importance of VSC-HVDC in minimization of power loss and voltage stability is studied for meshed networks. The study is made on both the IEEE 14 and IEEE 118 bus system. It has been shown that losses can be reduced if VSC-HVDC transmission is integrated to meshed AC system.

Basically the study of VSC-HVDC is the study of the control system and the study of interaction of the control system with the rest of the grid. In [22, 26, 27] the control system of VSC-HVDC for wind application and industrial system application is studied. These works developed an appropriate control system and studied different tuning techniques of the controllers for better performance.

This thesis work focuses on showing the possibility of improving the dynamic performance of EEPCo high voltage grid through utilizing VSC-HVDC as one part of its transmission system. It differs from above research works in that it investigates VSC-HVDC system as a transmission medium and as a FACTS device for reactive power support and voltage dynamics control using the existing section of EEPCo grid model.

## **2.4 High Voltage DC Transmission Overview**

The first electric power commercially generated by Thomas Elva Edison was DC. The transmission was also DC. However, due to the impossibility of transmitting DC over longer distances at lower voltages that brings high power losses the need shifted towards AC

transmission systems [26]. The appearance of transformers and the increased importance of induction machines at industries were other factors that made AC transmissions dominant.

High Voltage DC transmission (HVDC) is power electronics based transmission system. In HVDC through the controlled actions of power electronics devices, AC power is converted to DC power and made ready for transmission. For applications of Power transmission via cables, bulk-power transmission over long-distance, unsynchronized AC-system connection, power system stability improvement and firewall function against instability spread, HVDC transmission is more advantageous than HVAC transmission.

#### **2.4.1 HVDC transmission technologies**

There are two technologies of HVDC transmission: the LCC-HVDC and VSC-HVDC transmission.

The line commutated converter based HVDC is also known as classical HVDC. It is currently a widely used DC transmission system. It uses thyristor based converters. Thyristor converters turning off need the current flow through them to be zero. Hence the switching frequency is system frequency 50 or 60 Hz. This results in production of low order harmonics and a requirement of larger filters for filtering out the generated harmonics.

LCC-HVDC always consumes reactive power. This is due to the lagging current which is generated by delayed firing of the converter switches. This reactive power demand is a disadvantage to the surrounding AC network. The reactive power supply is done by shunt capacitors or Static Var Compensators (SVC) installed at the end terminals.

On the other hand, VSC-HVDC is the transmission technology based on voltage source converters and pulse width modulation (PWM). In VSC-HVDC transmission the converters are insulated gate bipolar transistors (IGBTs) with anti parallel diodes working on a high frequency PWM switching. As a result of high frequency harmonics generation by very fast PWM switching, filter sizes employed are smaller as compared to LCC-HVDC. In this respect, VSC-HVDC is more advantageous than LCC-HVDC. More over, unlike classical



HVDC they do not want reactive power provision for their operation. This avoids additional costs for reactive power supply equipments.

#### 2.4.2 HVDC transmission schemes

There are several HVDC transmission schemes. The selection of each scheme at planning stage depends on the operational requirements, flexibility of demand, reliability issue and cost [11, 22]. The following are the most common HVDC configuration schemes.

- a. **Monopolar:** In this configuration scheme a single line is used between the converters and either a positive or negative voltage is used for the transmission. The ground or sea can be used as a return path. Alternatively, a metallic return path can be used. Most HVDC installations start as a monopolar transmission, latter developing to the advanced schemes such as bipolar or homopolar schemes.
- b. **Bipolar:** Here power transmission is carried out using two conductors of opposite polarity. It is a combination of two monopolar systems. Due to this doubling reliability of the system is increased. When one pole of the transmission is removed the other part resumes the normal operation using ground as a return path.
- c. **Back-to-back:** This is a zero distance transmission. The two converters are connected to each other without any DC line. Back-to-back scheme is applied when two transmission systems of different frequency and different control principle are interconnected.

The schematic diagrams of the different configurations are shown in figure 2.2.

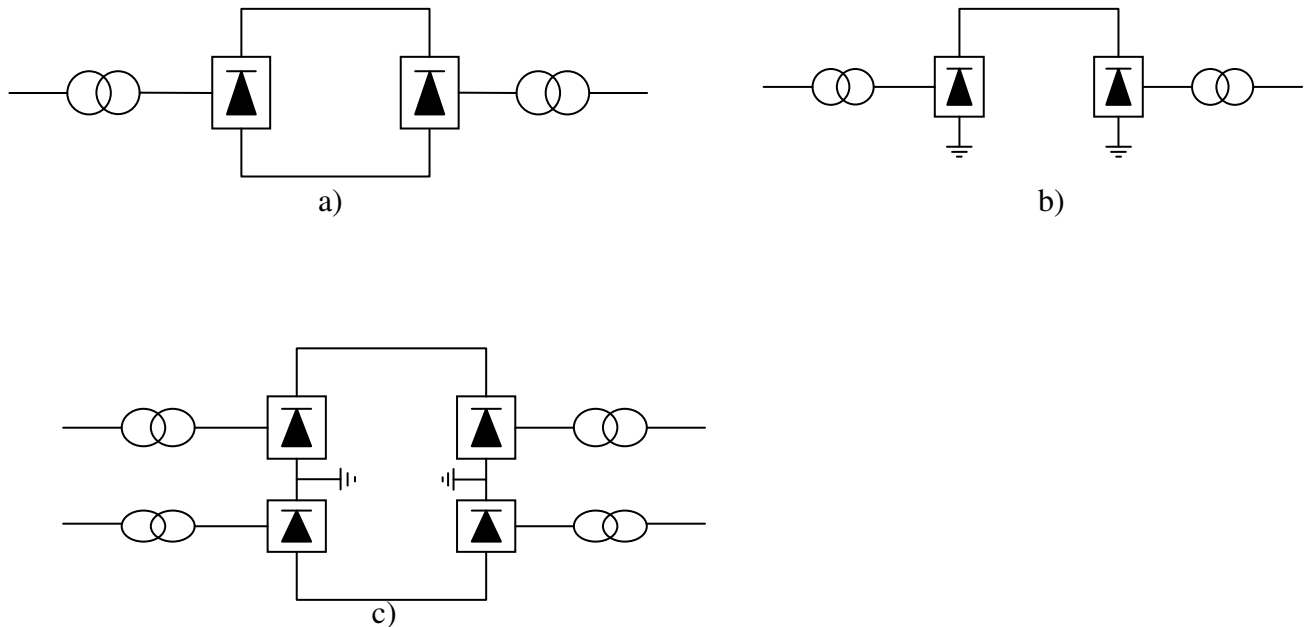


Figure 2.2: HVDC configuration schemes: a) Back-to-back b) Monopolar c) Bipolar

## 2.5 The VSC-HVDC System

It is important to discuss the components of VSC-HVDC transmission and their design aspects before proceeding to its modeling and control. Studying VSC-HVDC transmission components and the design aspects is an important part of economic as well as technical analysis. A detailed component studies and knowledge make system planners and designers to be able to optimize the tradeoff between cost and quality.

VSC-HVDC transmission system basically consists of converter valves, phase reactors, filters, power transformers and DC lines. The VSC-HVDC basic system is shown below in figure 2.3 and brief descriptions and design issues are discussed in the subsequent sections.

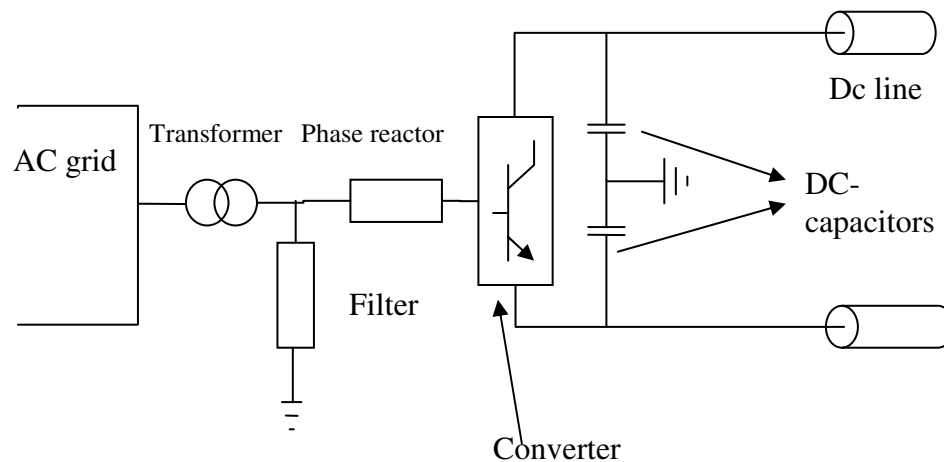


Figure 2.3: The VSC-HVDC basic system

### 2.5.1 Converters

Converters are the most important parts of VSC-HVDC system. They play the role of converting AC power to DC power or DC power to AC power. The converter valves are built with IGBT power semiconductors. They are provided with R-C snubbers and series R-L elements to reduce  $dv/dt$  and  $di/dt$  stresses that occur during ON/OFF transitions. In VSC-HVDC transmission one of the converter acts as a rectifier and the other acts as an inverter. The two converters can be connected either via a dc cable, or an over head line or in back-to-back connection depending on the application.

The IGBT valves are arranged in different ways resulting converter topologies. There are different converter topologies. These topologies are broadly classified as two level topology and a multi level topology [32]. Common aims of these topologies are:

- (i) To minimize the switching losses of the semiconductors inside the VSC.
- (ii) To produce a high-quality sinusoidal voltage waveform with minimum or no filtering requirements.

The two level converter topology is the simplest circuit configuration that can be used to construct 3-phase VSC. It consists of six valves and generates only two DC voltage values,  $\pm U_{dc}$ .

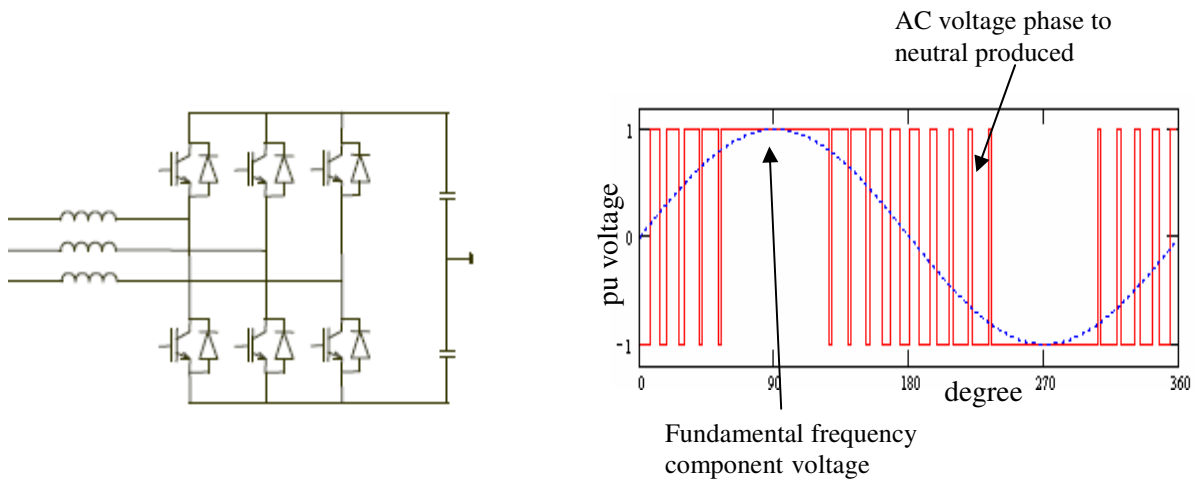


Figure 2.4: Three-phase two level converter topology and produced wave form

Simple power and control circuitry, small DC capacitor size, small foot print environmentally and same semi conductor duty ratio are some of the advantages related to a two-level VSC.

A multi level topology is a converter topology which has greater than two levels. The multilevel VSC found various applications in power systems due to its high power density, excellent performance, low conversion loss and high reliability [31].

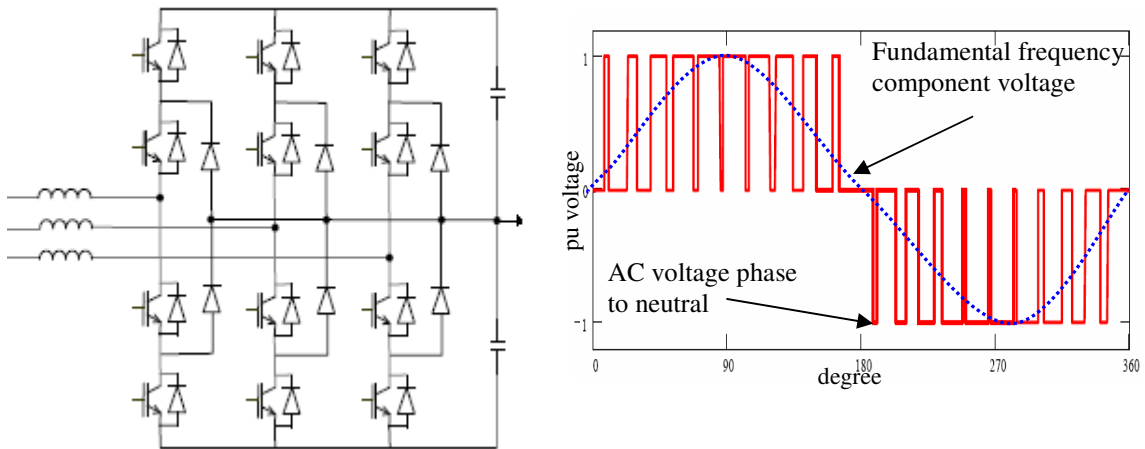


Figure 2.5: Three-phase three-level converter topology and produced wave form

### 2.5.2 Phase reactors

They are made up of large inductance with small resistance. They are used to regulate the active and reactive power flow to the ac grid. It is also part of low pass filter that prevent high frequency harmonics from entering the transformer [30].

The inductive reactance  $L$  between rectifier and AC supply is used to reduce commutation dips produced by the rectifier, to limit fault current and to soften voltages spikes of the mains.

The inductor dimensioning is done in order to guarantee the current ripple will be less than 10% [31].

### 2.5.3 Transformers

Transformers are used for converting the system voltage to a value suitable for the converter. For VSC-HVDC application standard transformers are used. The leakage reactance of the transformer is usually in the range 0.1-0.2 pu [22].

As the filter is located between the transformer and the converter the problem of power loss due to the harmonics in the transformer winding is not a serious problem. Often the transformer is equipped with tap changer on the secondary side to increase the reactive power range [29].

In this thesis VSC-HVDC transmission test system development the converter transformers convert 230 kV to 45 kV which is suitable for the converters. The transformers configuration is star ground-star (Yg-Y) to avoid phase angle shift between the primary and secondary voltages. Due to the fact that a transformer can be represented by its equivalent inductance and resistance in series, the power regulating task of the reactor is made to be fully covered by the converter transformers [32]. The dimensioning is done according to [31]. Accordingly the transformers are chosen to have inductance  $L=12.9$  mH and resistance  $R= 0.20253 \Omega$ .

### 2.5.4 DC operating voltage

The large proportion of the cost of HVDC links is the cost of the converter bridges. Higher voltage levels, which usually chosen for large power transfer, require many valves to be put in series, thus higher costs [21]. Thus the choice of the voltage levels mainly touches economical issues. As a result, the selection of operating voltages constitutes one part economic optimization of VSC-HVDC transmission installations.

Fundamental frequency component voltage output of the converter can be related to the DC operating voltage by the following equation.

$$U_{L-L} = \frac{\sqrt{3}M \cdot U_{DC}}{2\sqrt{2}} \approx 0.612 M \cdot U_{DC} \quad (2.1)$$

Where  $U_{L-L}$  – line to line voltage

$U_{DC}$  –DC voltage

M - Modulation index

The modulation index (M) is a ratio of a triangular wave amplitude and reference sinusoidal reference wave amplitude and given by:

$$M = \frac{\hat{U}_{triangular}}{\hat{U}_{reference}} \quad (2.2)$$

In this thesis VSC-HVDC transmission model development, using equation 2.1 with M= 0.9 and  $U_{L-L} = 45$  kV the DC link voltage  $U_{DC} = 81.7$  kV is computed.

### 2.5.5 DC capacitor

The dc capacitor is an important part of the converter for maintaining the DC voltage at constant value. Hence, designing the dc capacitor is of a prime importance. The capacitor is designed in a way to achieve a small ripple in the DC voltage. The DC capacitor size is characterized by the time constant  $\tau$  defined as a ratio between the DC powers stored at the DC side of the converter to the converter nominal apparent power [22, 28].

In order to obtain a small ripple in the DC voltage, large DC capacitors are required. However, application of large DC capacitors results in slow changes of the DC voltage in response to changes in power exchanged at the DC side of the converter. On the other hand, application of small DC capacitors results in fast response to changes in instantaneous power exchanged but at the expense of larger ripple in the dc voltage. Thus, the total capacitance of the dc capacitors can be approximated by [22]:

$$\tau = \frac{1/2 C_{dc} U_{dc}^2}{S_N} \quad (2.3)$$

Usually  $\tau$  assumes the value between 4ms-10ms. Here in this thesis time constant of 4ms is used so as to achieve a small ripple in the DC voltage. For having DC voltage of 81.7 kV at a base power of  $S_n = 45$  MVA the capacitance will be  $C_{dc} = 53.933 \mu F$ . Base power is selected taking into consideration the average power, 40 MW being transmitted by Mota-Debre Markos line, currently.

### 2.5.6 Shunt filters

Shunt filters are utilized for the filtering out of the generated harmonics. Together with the phase reactor they form part of the low pass filter. They are tuned for filtering higher frequency harmonics so that the fundamental frequency component is amplified. It prevents harmonics from entering to the AC system. The generated harmonics depend on the switching frequency.

In the case of VSC-HVDC the harmonic generated are of higher order determined by the frequency modulation ratio ( $m_f$ ). Frequency modulation ratio is the ratio of converter switching frequency ( $f_{switch}$ ) to the fundamental frequency ( $f_{fundamental}$ ) given by:

$$m_f = \frac{f_{switch}}{f_{fundamental}} \quad (2.4)$$

Hence the required filters are smaller in size as compared to classical HVDC filters. The harmonics are generated at frequencies ( $f_k$ ):

$$f_k = (jm_f \pm k)f_{\text{fundamental}} \quad (2.5)$$

Where  $j$  and  $k$  are integers and the sum  $j+k$  is odd.

The filters are installed between the reactor and the transformer. They protect the transformer from getting stressed by high frequency harmonics and prevent the harmonics from entering to the AC system [29].

### 2.6 VSC-HVDC Principle of Operation

Through controlled PWM pulse signals that applied to converter switches VSC-HVDC is capable of serving the purpose of grid reactive power support and active power transmission.

The operation of a VSC-HVDC can be explained by considering each terminal as a voltage source connected to an AC transmission network via series reactors. Let consider the following one phase equivalent electrical circuit of VSC-HVDC station.

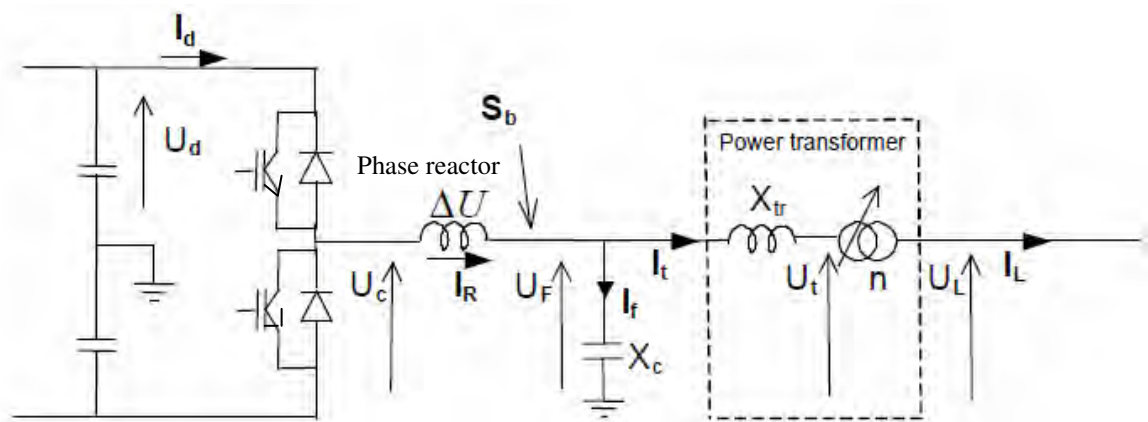


Figure 2.6: Circuit diagram of VSC-HVDC converter station

From the circuit diagram above the power between the converter reactor and the filter is calculated as:



$$\bar{S}_b = P + jQ = \sqrt{3} \bar{U}_F \bar{I}_R^* \quad (2.6)$$

Where  $\bar{S}_b$  – Base apparent power

P – Active power

Q - Reactive power

$\bar{U}_F$  – Filter bus voltage

$\bar{I}_R^*$  – Complex conjugate of the current through the reactor

The active and reactive power between converter and filter bus for a lossless reactor (considering R=0) is given by [30]:

$$P = \frac{U_F U_c}{X_{reactor}} \sin \delta \quad (2.7)$$

$$Q = \frac{U_F (U_F - U_C \cos \delta)}{X_{reactor}} \quad (2.8)$$

Where  $U_F$  -filter phase voltage

$U_C$  -converter voltage

$\delta$  -is the phase angle difference between converter bus and filter bus.

$X_{reactor}$  - Reactance of the reactor

Equation (2.7) shows that the active power flow is dependent on phase angle difference between the filter bus voltage and the converter voltage. If  $U_C$  is in phase lag to  $U_F$ , the active power flows from AC to DC side. This is rectifier mode operation of the converter. On the other hand if  $U_C$  is in phase lead to  $U_F$ , active power flows from DC to AC side which is inverter mode of operation. This principle of operation is illustrated in Figure 2.7a.

On the other hand, according to equation (2.8) the reactive power flow depends on the voltage difference between the filter bus and converter output.

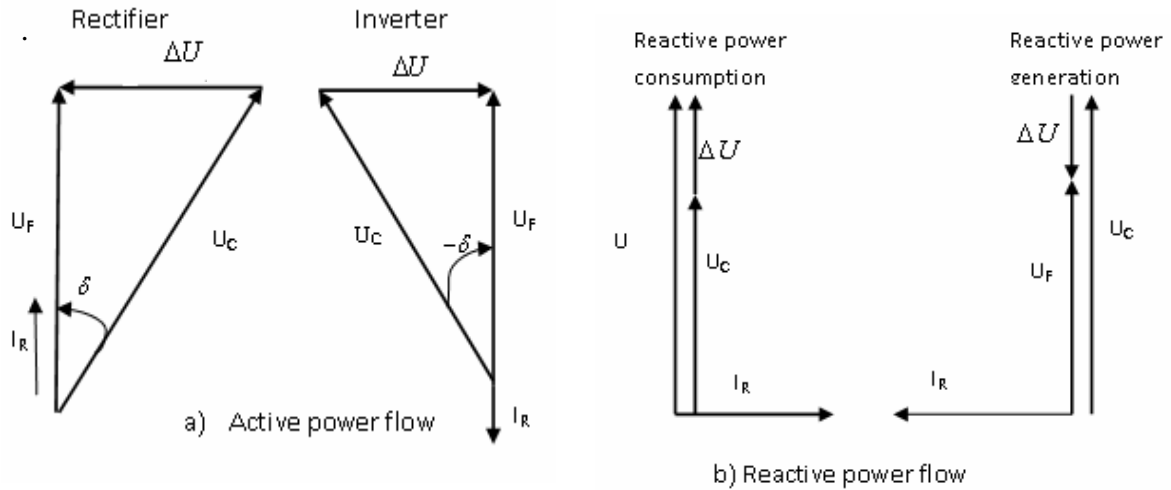


Figure 2.7: Active and reactive power flow control of VSC-HVDC

The complete control of magnitude of the voltage from the converter helps to determine the injection or absorption of reactive power. When  $U_F$  (AC system voltage) go down below converter set reference voltage  $U_C$ ,  $Q$  gets negative meaning reactive power to be supplied from the converter. On the other hand when  $U_F$  go beyond  $U_C$ ,  $Q$  gets positive, meaning reactive power absorption from the AC network so as to lower the voltage. This is the way the control of AC voltage limits takes place. Figure 2.7b illustrates this principle of operation.

Through the application of pulse width modulation it is possible to generate voltage of any magnitude and phase. Thus, active and reactive powers can be controlled independently. Moreover, the converters at either end of the link can be considered as a controlled synchronous machine capable of generating voltage of any magnitude and phase angle given by:

$$V_c(t) = 0.5V_{DC}M \sin(\omega t + \delta) \quad (2.9)$$

## 2.7 Pulse Width Modulation (PWM)

Pulse Width Modulation (PWM) is a modulation technique that generates variable-width pulses to represent the amplitude of an analog input signal.

In PWM switching scheme a comparison between a fundamental frequency modulating signal and a fixed frequency carrier signal is used to generate firing pulse for VSC converter switching. This comparison produces pulse signals of different width. A desired amplitude and phase angle of output voltage from VSC can be generated by varying the magnitude and phase angle of the modulating signal.

Basic purpose of PWM technique is to reduce inverter output harmonic level, to increase voltage magnitude and to reduce switching losses [33].

The PWM technique can be realized in variety of ways. Among these sinusoidal PWM, space vector PWM, optimized PWM, and sinusoidal PWM with third harmonics elimination are the most common.

The PWM technique chosen on DIgSILENT power factory for this work is sinusoidal PWM. In sinusoidal PWM scheme converter firing pulse signals are generated by comparing a fundamental frequency sinusoidal wave form with a triangular carrier signal as shown in figure 2.8. The relative level of the two waves is used to control the switching of devices in each phase leg of the inverter. The frequency of the triangular carrier signal determines the switching frequency of the converters.

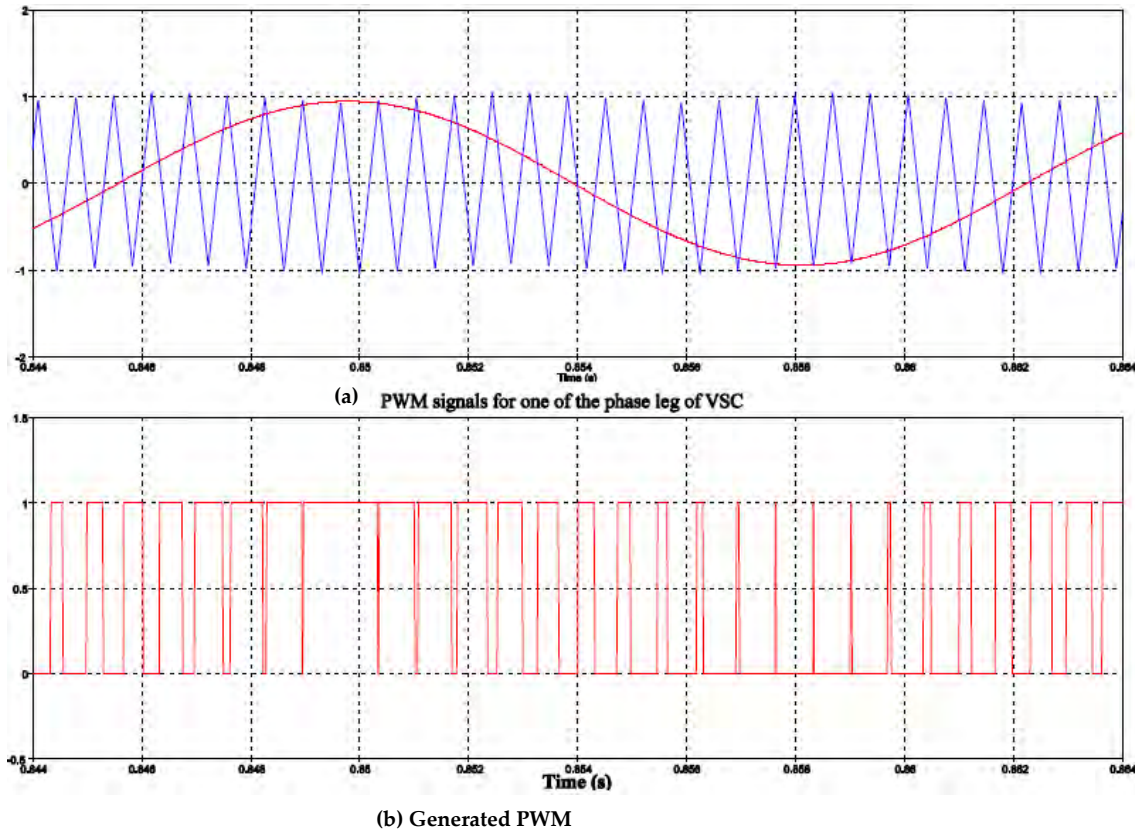


Figure 2.8: Sinusoidal PWM based on triangular carrier signal [32]

## 2.8 Capability Curve of VSC-HVDC

From the basic trigonometric identity we do have the following relation.

$$\sin^2 \delta + \cos^2 \delta = 1 \quad (2.10)$$

Expressing the sine and cosine of the phase angle difference in terms of powers and voltages in equation (2.7) and equation (2.8) and substituting to equation (2.10) will lead us to:

$$P^2 + \left( Q - \frac{U_F^2}{X_{reactor}} \right)^2 = \left( \frac{U_F \cdot U_C}{X_{reactor}} \right)^2 \quad (2.11)$$

This is a circle equation of radius  $\frac{U_F \cdot U_C}{X_{reactor}}$  and center at  $(0, \frac{U_F^2}{X_{reactor}})$ , which is a capability curve of voltage source converter. Capability curve is PQ-diagram defining the valid operating points of given equipment. Equation 2.11 shows the possibility of a four quadrant operation in

PQ-plane. Fig 2.9 below is a capability curve of VSC-HVDC drawn the origin shifted to this center for ease of discussion.

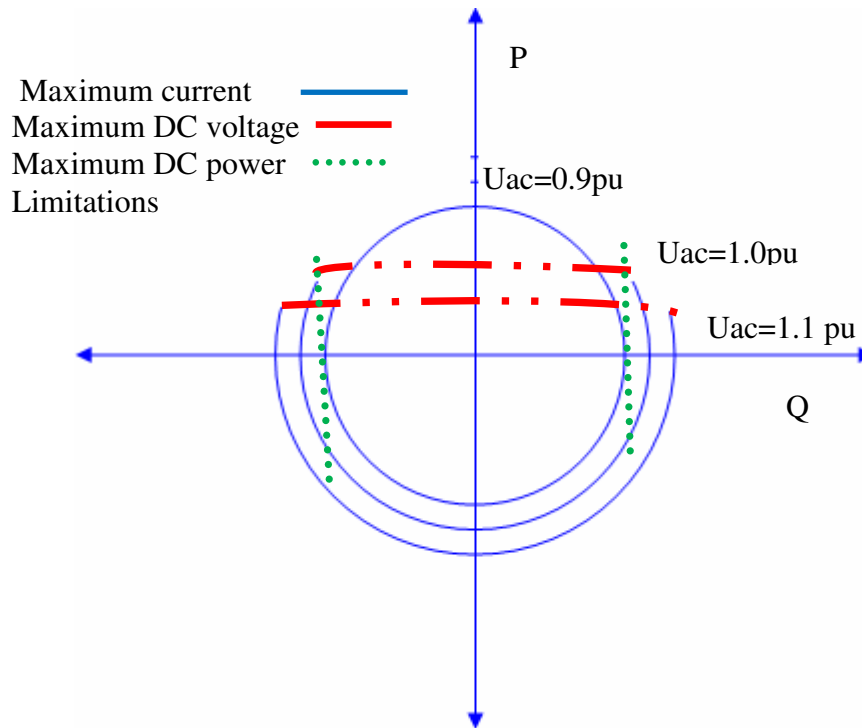


Figure 2.9: Capability curve of VSC-HVDC

With regard to VSC-HVDC three main factors limit the capability curve. The first is the maximum current through the IGBTs. This results the maximum MVA circle in the curve. The second limit is maximum DC voltage level. This determines the maximum reactive power arc in the plane. The last factor is maximum DC power. This determines the maximum active power transferred through the link.

## 2.9 Economics of VSC-HVDC Transmission

The investment cost of VSC-HVDC transmission installation is a combination of cost of various components within it. Converter station costs are found to be high as compared to AC substations. On the other hand the transmission lines in VSC-HVDC bring a significant cost reduction as compared to AC transmission lines. The average cost of different transmission technologies including VSC-HVDC is shown in table 2.1 below.

Table 2.1: Average investment cost of transmission system technologies [40]

<b>HVAC and HVDC transmission line</b>	<b>Cost</b>	<b>Unit</b>
HVAC over head single line circuit	200-500	kEUR/km
HVAC over head double circuit line	300-700	kEUR/km
HVDC over head bipolar line	200-400	kEUR/km
HVDC XLPE under ground cable	1000-2500	kEUR/km
<b>HVDC converter stations and FACTS</b>		
Traditional HVDC converter	40-60	kEUR/MVA
VSC-HVDC converter	50-70	kEUR/MVA
UPFC	50-90	kEUR/MVA

Here it is important to note that VSC-HVDC economics depend on a combination of various factors and on a particular system requirement. Therefore to make a complete cost analysis it is important to consider different conditions such as transmission schemes (bipolar, monopolar), system power loss reduction/cost, DC transmission medium to be used (cable or over head line), future power electronics cost trends and other factors. In addition the enhancement of transmission capacity by VSC-HVDC and the consequent reduction in number of new AC line installations should be taken in to consideration. Some works show that VSC-HVDC can be economically competitive to HVAC [36, 40].

## CHAPTER 3

### CONTROL OF VSC-HVDC SYSTEM

#### 3.1 Introduction

The control system is an important part of VSC-HVDC transmission system. It is this control system that monitors the transfer of scheduled active power across the DC link and maintains acceptable system voltage through reactive power control. The control tasks insure reactive power support to the surrounding AC system which increases power transfer capability of the system at normal operation and maintains system stability during disturbances.

The control tasks done with regard to active power include power flow direction reversal and scheduled power transfers. Active power flow direction reversal in VSC-HVDC is done by changing the polarity of the DC current unlike the classical HVDC which employ reversal of DC voltage polarity [30]. On the other hand, reactive power is controlled by controlling the magnitude of the output voltage from the converter.

In order to achieve the objective of power flow control different types of control strategies have been proposed. The direct power control and the vector current control strategies are the two most known.

In direct power control the active power is controlled by controlling the phase-angle shift between the converter voltage and the AC system voltages while the reactive power is controlled by varying the converter output voltage magnitude with respect to system demand. Because of disadvantages like variable switching frequency and necessity of fast conversion and computation, the use of direct power control is not very common [26].

On the other hand the vector control strategy has excellent dynamic performance and inherent protection against over-currents [21, 32]. Due to this the vector current control scheme is most widely utilized. In vector current control strategy the input currents to the rectifier and the output currents from the inverter are measured and compared with the reference current values and the error signal is fed to the controllers to produce switching signal to the converters.

Vector control strategy is discussed in various literatures [21, 22, 26, 28, 32]. The control system for the VSC-HVDC link model in this thesis is developed based on vector control strategy taking the practices of these works.

### 3.2 Current Vector Control

This control scheme is named current vector control in that the control strategy is implemented on the vectors of currents as represented in a dq-rotating reference frame. In vector control strategy the three phase quantities are first transformed to quantities in a two coordinate  $(\alpha, \beta)$  stationary system and then further transformed to quantities in a dq-rotational reference frame. This makes the transformed quantities appear as constant magnitude vectors (DC- vectors), since the reference frame is rotating at system frequency. The magnitude of the vectors is equal to the peak values of the quantities in abc-reference frame. This transformation gives the advantage of analyzing DC quantities which is easier than analyzing AC equivalents. More over the comparison of the DC quantities result static errors. These static errors from the comparison of quantities can easily be eliminated by applying simple PI controllers [26, 27]. This is one important feature of the vector control strategy.

The other important property of vector control strategy is decoupled control ability that makes possible independent control of active and reactive powers. The decoupling of quantities allows the implementation of a cascaded control strategy which has improved dynamic performance. Cascaded control strategy in VSC-HVDC is a two level control system. It consists of outer controllers and the inner current controllers. The outer controllers include the active power controller, reactive power controller, frequency controller and the DC-voltage controller. The cascaded control scheme is shown below.



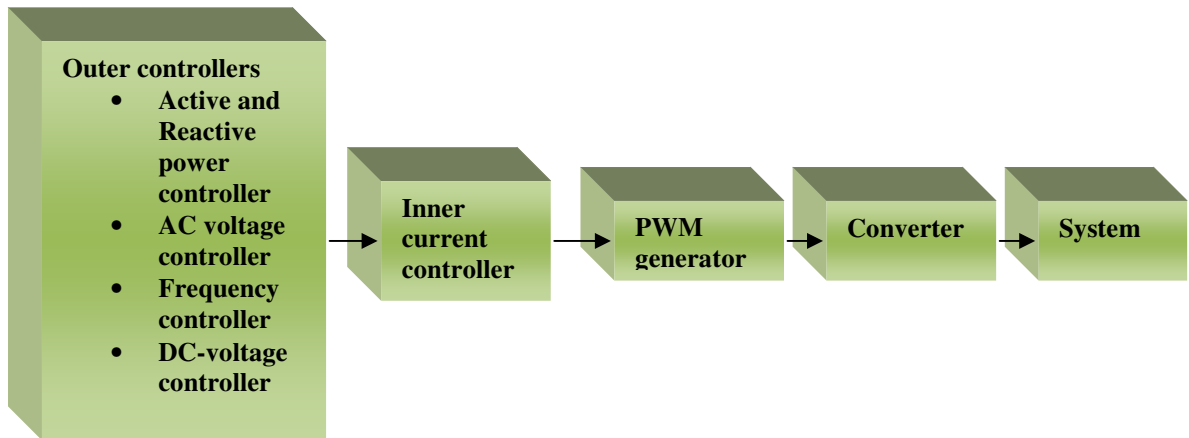


Figure 3.1: Control block diagram depicting how the errors are generated and how the outer controllers feed the inners

All the outer controllers are not used at the same time. One of the converters is required to control the DC voltage and the other to control the active power transfer. The selection of the remaining controllers depends on the application required.

### 3.3 VSC-HVDC Mathematical Modeling

The vector control strategy for VSC-HVDC starts from the mathematical modeling of VSC-HVDC system in dq-reference frame.

The voltage source converter can be represented by a controlled voltage source for the AC side as in figure 3.2 (a) and a current source for the DC side as in figure 3.2 (b). Therefore, we can represent the converter and grid interaction by the following equivalent circuit.

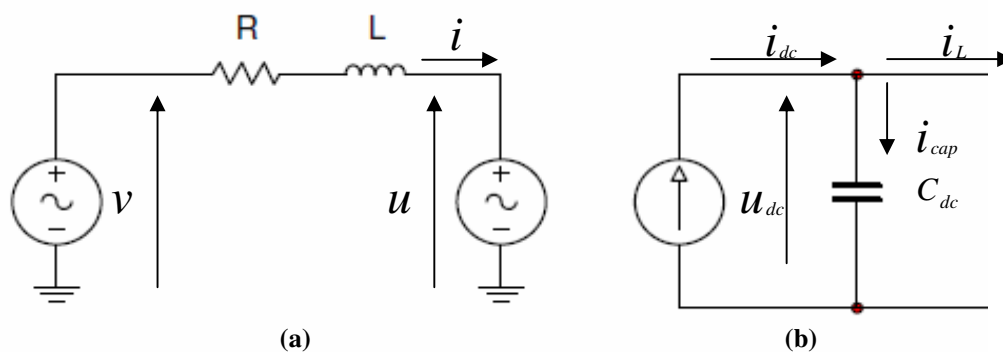


Figure 3.2: Equivalent circuit of VSC station

Applying Kirchhoff's voltage law across the reactor and the resistor the following equation holds true.

$$L \frac{di_{abc}}{dt} = v_{abc} - u_{abc} - Ri_{abc} \quad (3.1)$$

Where  $v_{abc}$  - Grid AC voltage in abc reference frame

$u_{abc}$  - Converter AC side output voltage in abc reference frame

$i_{abc}$  - AC current through the reactor in abc reference frame

$R$  - Reactor resistance

$L$  - Reactor inductance

Then applying the coordinate transformation technique known as Clark transformation the time varying three phase quantities are transformed to vectors in a two coordinate  $(\alpha, \beta)$  system.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \cos \frac{2\pi}{3} & \cos \frac{4\pi}{3} \\ 0 & \sin \frac{2\pi}{3} & \sin \frac{4\pi}{3} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (3.2)$$

This Clark transformation gives the advantage of dimension order reduction. Hence,

$$L \frac{di_{\alpha\beta}}{dt} = v_{\alpha\beta} - u_{\alpha\beta} - Ri_{\alpha\beta} \quad (3.3)$$

By using transformation angle from the system phase measurement at the PLL the electrical quantities are further transformed from the  $(\alpha, \beta)$  stationary coordinate system quantities to a rotational dq-reference frame equivalent quantities by applying the following park transformation.

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (3.4)$$

Hence, equation (3.3) transformed to:

$$L \frac{di_{dq}}{dt} = v_{dq} - u_{dq} - (R + j\omega L)i_{dq} \quad (3.5)$$

The term  $j\omega Li_{dq}$  is a speed voltage quantity introduced due to the rotation of the reference system and represents the time derivative of the synchronous rotating frame.  $\omega$  is the frequency at which the AC system operates. This speed voltage term shows that the rotation of the reference frame introduces cross coupling between the quantities of the two axes. Separating equation (3.5) into respective components gives the following.

$$\begin{aligned} L \frac{di_d}{dt} &= v_d - u_d - Ri_d + j\omega Li_q \\ L \frac{di_q}{dt} &= v_q - u_q - Ri_q - j\omega Li_d \end{aligned} \quad (3.6)$$

These equations show the relationship between the converter voltages and input currents in dq-reference frame.

On the other hand the DC side of the converter, applying Kirchhoff's current law at the node on the DC side in figure 3.2 is expressed by:

$$C_{dc} \frac{du_{dc}}{dt} = i_{dc} - i_L \quad (3.7)$$

Where  $i_{dc}$  – Converter output DC current

$i_L$ - DC current through DC link

$C_{dc}$ - DC capacitor capacitance

Thus equations (3.6) and (3.7) complete the mathematical modeling of VSC-HVDC.

At this point it is necessary to deal about the power relations in the dq-reference frame so as to arrive the objective of controlling active and reactive power by using dq-quantities.

The instantaneous power of a three phase system is the sum of the instantaneous powers produced by each phase. Hence:

$$p(t) = v_a(t)i_a(t) + v_b(t)i_b(t) + v_c(t)i_c(t) \quad (3.8)$$

Expressing currents and voltages in two phase  $(\alpha, \beta)$  stationary system gives the following power equation.

$$p(t) = \frac{3}{2}(v_\alpha i_\alpha + v_\beta i_\beta) + 3v_0 i_0 \quad (3.9)$$

The active power is independent of the coordinate system. Hence, it can be expressed in the dq-reference frame as:

$$p(t) = \frac{3}{2}(v_d i_d + v_q i_q) + 3v_0 i_0 \quad (3.10)$$

In a balanced condition the 0 components are equal to zero. Hence p will have the form.

$$p(t) = \frac{3}{2}(v_d i_d + v_q i_q) \quad (3.11)$$

The reactive power on the other hand can be calculated from the apparent power as:

$$s(t) = \frac{3}{2}ui^* = p(t) + jq(t) \quad (3.12)$$

The imaginary part of this equation represents the reactive power. Hence,

$$q(t) = \text{Im}\left(\frac{3}{2}ui^*\right) = \frac{3}{2}(v_q i_d - v_d i_q) \quad (3.13)$$

Synchronizing the d axis voltage with system voltage leads the following important relation.

$$v_d = v \quad \text{and} \quad v_q = 0 \quad (3.14)$$

Then, the power equations become:

$$\begin{aligned}
 P &= \frac{3}{2} v_d i_d \\
 q &= -\frac{3}{2} v_d i_q
 \end{aligned}
 \tag{3.15}$$

Equation (3.15) indicates that active power is dependent on the d-axis current while reactive power is dependent on q-axis current. Hence, active and reactive powers are decoupled and independent control is possible by independently controlling  $i_d$  and  $i_q$ .

On the other hand the power equation for the DC side is:

$$P_{dc} = v_{dc} i_{dc} \tag{3.16}$$

### 3.4 The Inner Current Control Loop

The current controller loop is the inner part of the cascaded control strategy. It needs to be very fast as compared to the outer controllers so as to achieve control system stability. It is supplied current reference values from the outer controllers and dq transformed currents from transducers. The inner current control loop has the following general set up.

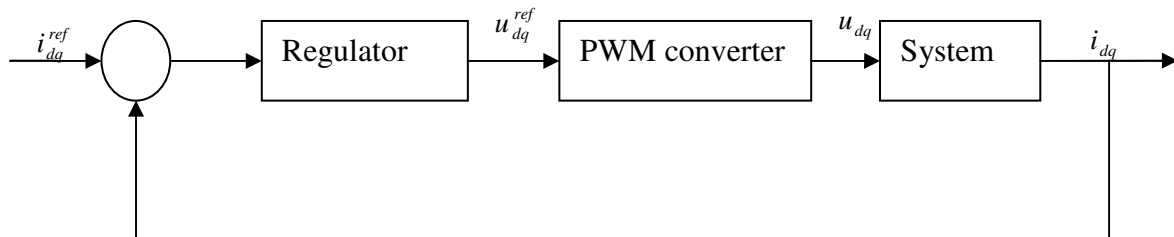


Figure 3.3: The inner current control loop set up

The inner current control loop consists of two PI regulators each for the d and q axis currents. These controllers transform the error current from the comparison to a voltage signal which is used by PWM generator for switching the converter.

#### 3.4.1 PI regulator

PI stands for proportional and integral controller. Due to DC vectors produced by dq-transformation a PI controller is sufficient to reduce the steady state error signal to zero.

The PI regulator is represented by the following equation:

$$K_p \left( 1 + \frac{1}{sT_i} \right) \quad (3.17)$$

Where  $K_p$  is the proportional gain while  $T_i$  is the integral time constant.

The regulator produces the voltage order to the PWM converter. Hence from the inner current control loop in figure 3.3 the output of the regulator is.

$$(i_{dq}^{ref}(s) - i_{dq})(K_p(1 + \frac{1}{sT_i})) = u_{dq}^{ref}(s) \quad (3.18)$$

### 3.4.2 PWM converter

The converter is approximated by a first order equation. It produces output voltage which is the converter side voltage as shown in Figure 3.2.

$$u_{dq}^{ref} \left( \frac{1}{(1 + T_a s)} \right) = u_{dq} \quad (3.19)$$

Where  $T_a = T_{switch} / 2$

Hence this approximation shows that the converter is an ideal power transformer with time delay  $T_a$ . In PWM the switching frequency is expected to be much larger than the system frequency. In our design case converter switching frequency of 5000Hz is chosen. Which gives  $T_a = 0.0001$  s.

### 3.4.3 System transfer equation

From equation (3.6) it is evident that the dq representation of AC side of the converter system contains a cross coupling term  $j\omega L i_{dq}$ . From the control point of view this term is considered as a disturbance for each axis.

In order to eliminate the cross coupling (disturbances), compensation terms  $v_d$  and  $\omega Li_q$  are fed forward on the  $d$ -axis controller while  $v_q$  and  $\omega Li_d$  are fed forward on the  $q$ -axis controller [34].

With the compensation terms used for decoupling, the converter input from the controller is now:

$$\begin{aligned} u_d^{ref} &= -(i_d^{ref} - i_d)(K_p(1 + \frac{1}{sT_i})) + \omega Li_q + v_d \\ u_q^{ref} &= -(i_q^{ref} - i_q)(K_p(1 + \frac{1}{sT_i})) - \omega Li_d + v_q \end{aligned} \quad (3.20)$$

Hence the converter output is:

$$\begin{aligned} \left( -(i_d^{ref}(s) - i_d)(K_p(1 + \frac{1}{sT_i})) + j\omega Li_q + v_d \right) \left( \frac{1}{(1 + T_a s)} \right) &= u_d(s) \\ \left( -(i_q^{ref}(s) - i_q)(K_p(1 + \frac{1}{sT_i})) - j\omega Li_d + v_q \right) \left( \frac{1}{(1 + T_a s)} \right) &= u_q(s) \end{aligned} \quad (3.21)$$

Since the converter is assumed as ideal transformer which has only a time delay impact on its input. Hence we can assume that the input of the converter is the same as the output except time delay.

Substituting equation (3.6) to equation (3.21) results the following in time domain.

$$\begin{aligned} u_d &= L \frac{di_d}{dt} + Ri_d \\ u_q &= L \frac{di_q}{dt} + Ri_q \end{aligned} \quad (3.22)$$

As it is evident from equation (3.22) the cross coupling terms are eliminated and hence it is possible to have independent control of the  $d$  and  $q$  component currents.

Laplace transformation of equation (3.22) leads as to:

$$i_{dq}(s) = \frac{1}{R + Ls} u_{dq}(s) \quad (3.23)$$

Therefore the system transfer equation will become:

$$G(s) = \frac{1}{R} \frac{1}{1 + \tau s} \quad (3.24)$$

$\tau$  is the reactor time constant defined by:

$$\tau = \frac{L}{R} \quad (3.25)$$

Equation (3.22) shows that the two equations are independent of one another and the system is of first order.

The complete system with the compensation terms is shown by the following block diagram.

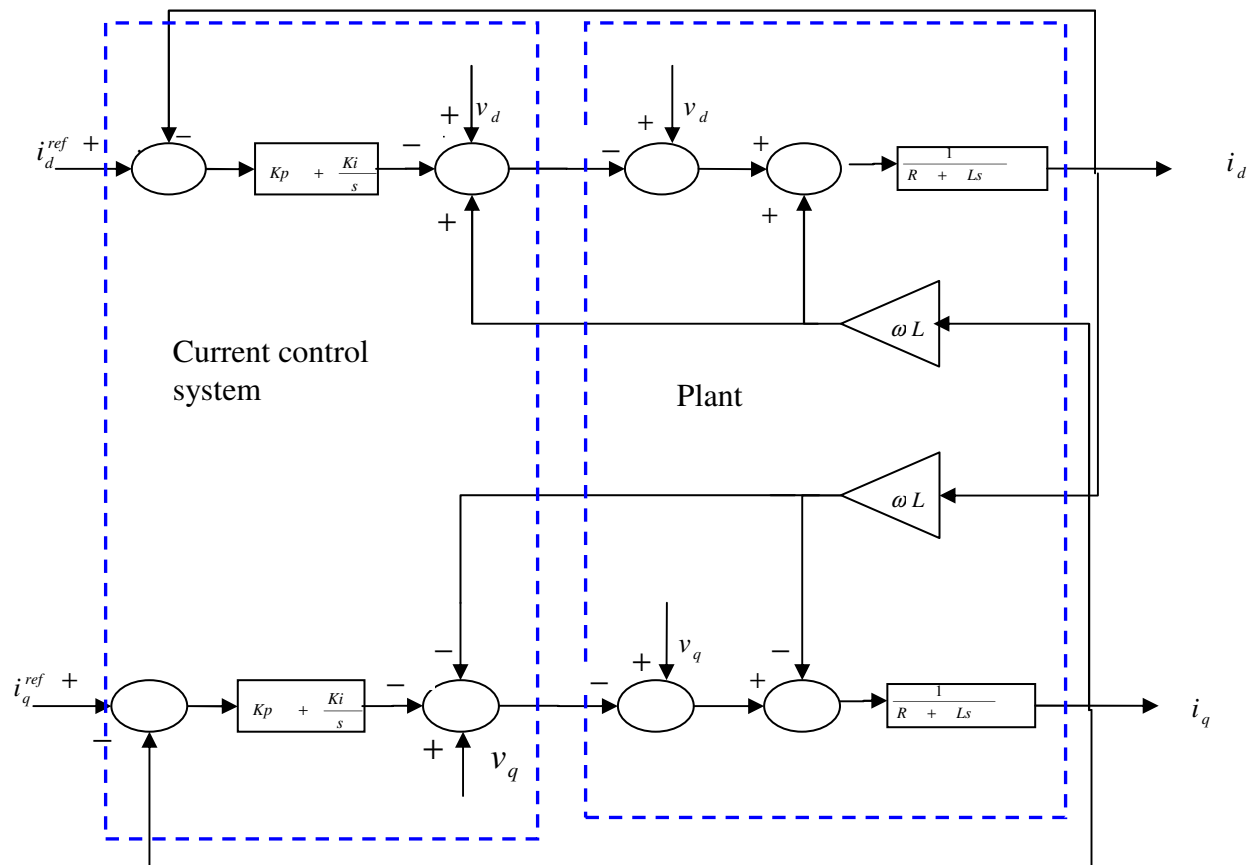


Figure 3.4: The inner current control loops with the compensation terms



After simplification including the converter, the current control loop will be represented by the following reduced form.

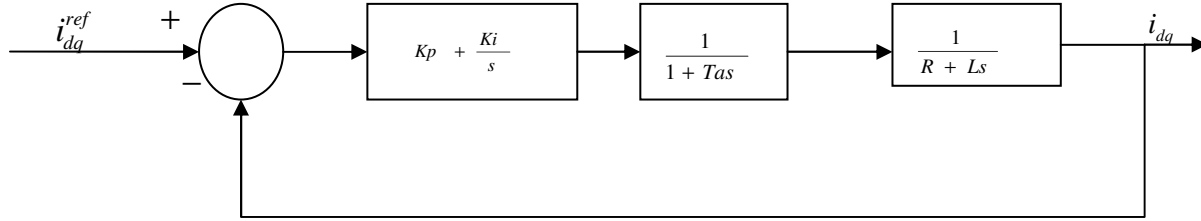


Figure 3.5: Reduced form of the inner current control loop

### 3.4.4 Tuning the current controller

Controller tuning can be accomplished using different techniques. The aim of tuning is to get fast response of the system and maximize plant output.

The tuning of the controllers for VSC here is based on the principle adopted for the basic electrical drives [35]. Accordingly, the speed of the controllers increases towards the inner loop. The inner loop is tuned according to the optimum modulus criterion. This method is implemented when the controlled system has one dominant time constant and the other minor time constant. The dominant pole is canceled by the controller zero to arrive at a standard transfer function. Then the absolute value (modulus) of this transfer function is equated to 1 from unity gain requirement to obtain the remaining parameters. It is chosen due to its simplicity and fast response at tracking the reference value.

The tuning of current controller by modulus optimum criteria can be obtained from the open loop transfer function of the current controller figure 3.5.

$$G_{ol}(s) = K_p \left( \frac{1 + sT_i}{sT_i} \right) \left( \frac{1}{1 + sT_a} \right) \left( \frac{1}{R + sL} \right) \quad (3.26)$$

Here the approach is to place the zero of the controller over the dominant pole of the system. Hence,  $T_i$  is equal to the reactor time constant  $\tau$ . Substituting the reactor values in section 2.5.3  $L=12.9\text{mH}$ ,  $R=0.20253\ \Omega$ :

$$T_i = \tau = \frac{L}{R} = 0.063694 \quad (3.27)$$

As a result pole zero cancellation take place. The zero of the controller cancels the dominant pole. This yields a second order close loop transfer function of the form:

$$G_{cl} = \frac{\frac{K_p/R}{sT_i(1+sT_a) + \frac{K_p/R}}{\frac{K_p/R}{R}}} = \frac{\frac{K_p/R}{R}}{s^2T_iT_a + sT_i + \frac{K_p/R}{R}} = \frac{K_p}{T_iT_aR} \left( \frac{1}{s^2 + \frac{s}{T_a} + \frac{K_p}{RT_iT_a}} \right) \quad (3.28)$$

$\xi$ , the damping constant of the second order equation is required to have the value 0.707 for the system to have optimum over shoot and rise time [28].

Hence, from equation (3.28) we can get,

$$\omega_n = \sqrt{\frac{K_p}{T_iT_aR}} \quad (3.29)$$

Then from this we can compute  $\xi$  as:

$$\xi = \frac{1}{2} \sqrt{\frac{T_iR}{K_pT_a}} \quad (3.30)$$

Solving for  $K_p$  and substituting the values:

$$K_p = \frac{T_iR}{4\xi^2T_a} = 64.52 \quad (3.31)$$

Hence our closed loop transfer function becomes:

$$G_{cl} = \frac{50.21 \times 10^6}{s^2 + 10^4 s + 50.21 \times 10^6} \quad (3.32)$$

Using matlab the following step response is obtained with specifications: Rise time  $t_r = 0.3 \times 10^{-3} s$ , settling time  $t_s = 0.842 \times 10^{-3} s$ , maximum over shoot  $M_p = 4.38\%$  peak time  $t_p = 0.629 \times 10^{-3} s$  and peak amplitude 1.04.

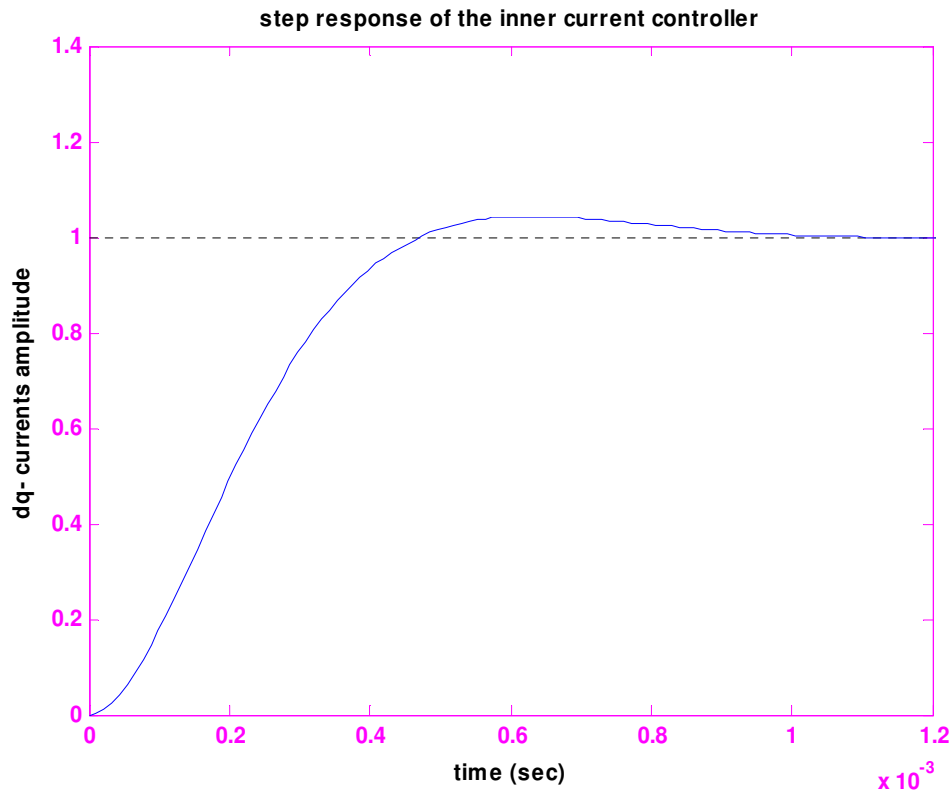


Figure 3.6: Step response of the inner current control loop with the designed current controller

This result shows that the system response is very fast with the controller designed by modulus optimum tuning technique.

### 3.5 Outer Controllers

The outer controllers perform a specific task. This includes active and reactive power control tasks, DC voltage control tasks and the frequency controlling tasks. In all these controllers

integrators can be used to eliminate steady state errors [22]. They act on input signal from measured value and a set reference signal and they produce the reference d and q currents which are going to be used as input signal for the inner current controllers.

### 3.5.1 PQ-controllers

The PQ-controllers are basically PI controllers. The main aim of PQ- control is to regulate the active and reactive power exchange between the converter and the grid.

Active and reactive powers are calculated from the grid and compared with the reference values and the error signal is made to pass through PI regulator. The PI controllers create the reference d and q currents which are going to be fed to the current controllers.

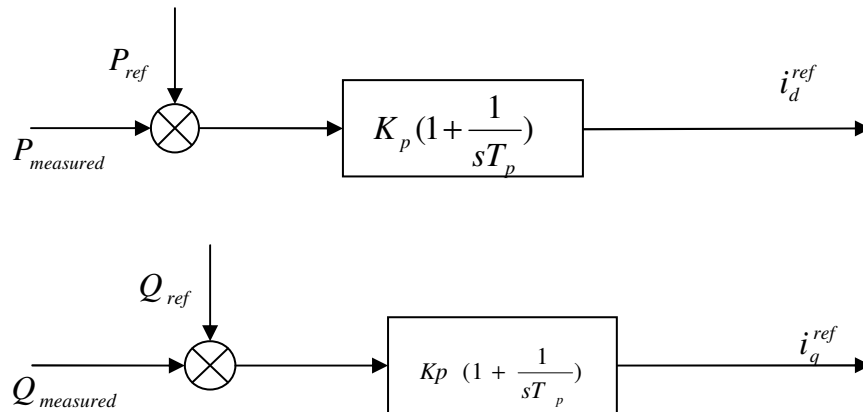


Figure 3.7: The PQ-controllers

There is not a general rule for tuning the PQ-controllers [21]. Hence the tuning in this work is done through trial and error on DIgSILENT until best responses are achieved. Accordingly,  $K_p = 10$  and  $T_i = 0.1$  are chosen for these controllers.

### 3.5.2 DC-voltage controller

DC voltage control is important for controlling the power exchange between the converters. The DC voltage control aimed at keeping the DC voltage at a defined value using the converter current as a control variable.

Assuming the converter to be lossless the active power that enters the converter is equal to the active power that leaves the converter.

Then equating the active power equation in equation (3.15) and the DC power equation (3.16) leads to:

$$\frac{3}{2} v_d i_d = v_{dc} i_{dc} \quad (3.33)$$

From equation (3.7) we can solve for  $i_{dc}$  as:

$$i_{dc} = i_L + C_{dc} \frac{dU_{dc}}{dt} \quad (3.34)$$

Substituting equation (3.34) to equation (3.33) gives the relation between the dc voltage and the d-axis current as:

$$\frac{3}{2} v_d i_d = v_{dc} \left( i_L + C_{dc} \frac{dU_{dc}}{dt} \right) \quad (3.35)$$

Laplace transformation and solving for  $U_{dc}$  leads us to the following important result.

$$U_{dc} = \frac{1}{Cs} \left( \frac{3}{2} \frac{v_d i_d}{v_{dc}} - i_L \right) \quad (3.36)$$

To make more illustrative lets depict the relationship using block diagram.

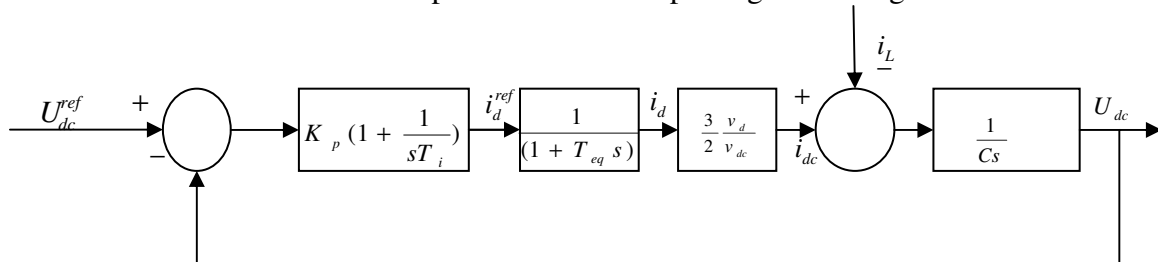


Figure 3.8: Block diagram representation of the DC voltage control loop

Here in order to avoid the effect of the disturbance from  $i_L$ , compensation term, which have the value  $\frac{2}{3} \frac{v_{dc}}{v_d} i_L$  can be added before the converter. The inner current loop is approximated by first order equation.

### 3.5.3 Tuning the DC voltage controller

Tuning of the DC controller is done through symmetrical optimum tuning. When the open loop transfer function has zero at the origin modulus optimum tuning cannot be implemented [28]. Since the open loop transfer function of the DC voltage controller loop has a pole at the origin as shown in Figure 3.8, here symmetrical optimum tuning is employed for designing the controller parameters.

For the voltage controller the parameters tuned by symmetrical optimum technique are calculated as follows.

The proportional time constant is [26, 27]:

$$T_i = a^2 T_{eq} \quad (3.37)$$

$a$  - is the symmetrical distance between  $1/T_i$  to cross over frequency and  $1/T_{eq}$  and cross over frequency [26, 27]. The recommended value of  $a$  is between 2 and 4.

The equivalent time delay due to the current control loop is calculated as:

$$T_{eq} = 2T_a = 0.0002 \quad (3.38)$$

Hence the proportional time constant taking  $a=3$  is  $T_i = 0.0018\text{sec}$ .

According to symmetrical optimum tuning technique the proportional gain is calculated as follows using the values  $V_{dc}=81.7\text{kV}$ ,  $C=53.933\ \mu\text{F}$ ,  $V_d=V=45\text{kV}$ .

$$k_p = \frac{2}{3} \frac{v_{dc} C}{V_d a T_{eq}} = 0.109 \quad (3.39)$$

The over all closed loop transfer function from figure 3.8 becomes:

$$G_{cl} = \frac{KT_i s + K}{T_i T_{eq} C s^3 + T_i C s^2 + KT_i s + K} \quad (3.40)$$

Where,  $K = \frac{3}{2} \frac{K_p v_d}{v_{dc}}$

Calculating the above values G will have the following form:

$$G_{cl} = \frac{5.301 \times 10^{-5} s + 0.02945}{1.942 \times 10^{-11} s^3 + 9.71 \times 10^{-8} s^2 + 5.301 \times 10^{-5} s + 0.02945} \quad (3.41)$$

The following step response is obtained using Matlab with Rise time 0.00156 s, peaking time 0.0043 s, peak amplitude 1.36, and settling time 0.0132 s is achieved.

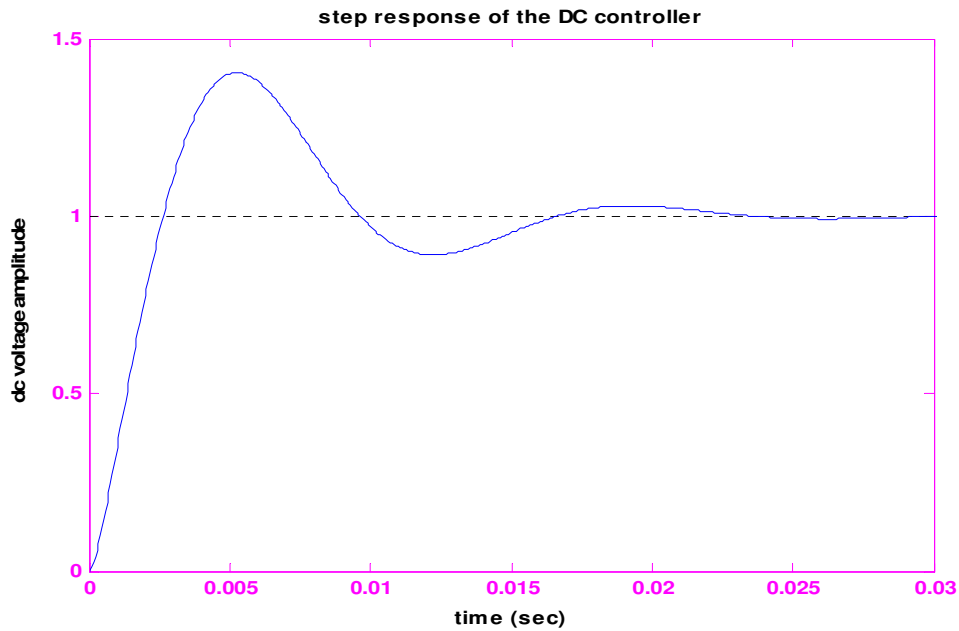


Figure 3.9: Step response of the designed DC voltage control loop.

The time response to step excitation shows that the system response is about five times slower than that of inner current controller and has higher overshoot. This slower response is necessary condition for the cascaded control system stability.

In Summary, in this chapter a mathematical model of VSC-HVDC is developed. Then a faster inner current controllers and outer DC controller as well as PQ-controllers are designed for the control of VSC-HVDC link. The parameters for inner current controllers is  $k_p=64.52$  and  $T_i=0.063694$ , for the DC controllers  $k_p=0.109$  and  $T_i=0.0018$ , for both P and Q controllers  $k_p=10$  and  $T_i=0.1$  is obtained. With this the control system design for our VSC-HVDC link is completed. In the next chapter the performance of the designed controllers will be evaluated as implemented on DlgSILENT power factory.

## CHAPTER 4

### SIMULATION STUDIES

In this chapter the performance of the designed VSC-HVDC controllers at a control system implemented on DIgSILENT, is evaluated by initiating disturbances. Next, the VSC-HVDC link with its complete control system is integrated to the North Western EEPCo system model and the system dynamic performance improvement for various disturbances introduced at different locations is discussed. Finally the AC-DC system operation at different loading conditions is evaluated.

#### 4.1 Testing the Control System

Testing the performance of the control system proves its effectiveness upon operation within the AC system. The designed controllers in chapter-3 coordinated in the control strategy described below are tasted using monopolar VSC-HVDC transmission system model shown below in figure 4.1. The associated data of the VSC-HVDC link are provided in table 4.1.

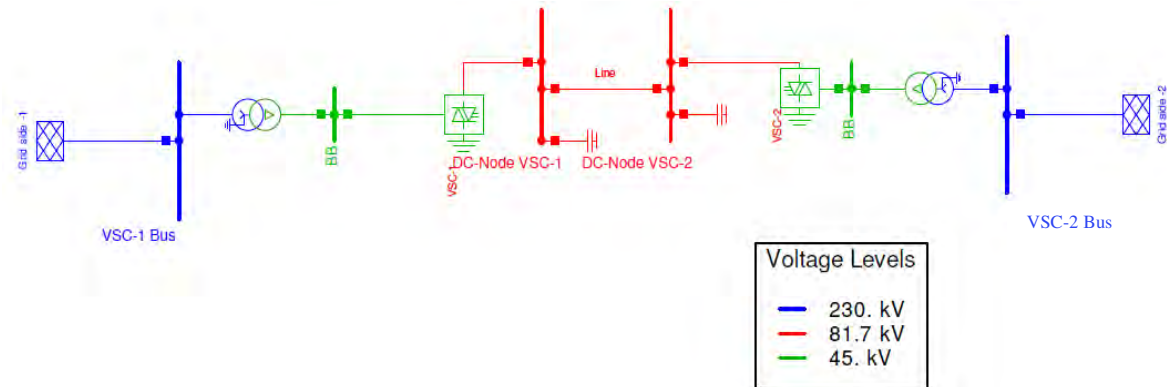


Figure 4.1: The controller test system

The grid sides are represented by external networks. Grid side-1 represents EEPCo grid at Mota side while grid side-2 represents Debre Markos side. The external networks are provided with parameters of short circuit power, short circuit current and R/X ratio taken from the actual EEPCo grid to create an operational resemblance with the operation in the grid.



Here, since the consideration is on the RMS quantities, it is not found necessary to deal with the low pass filters and the associated harmonics. RMS simulation deals with only the fundamental frequency component quantities.

Table 4.1: Test system Parameters

Component	Value
Transformer (230kV/45kV) rating	100 MVA
Transformer equivalent inductance	12.9 mH
Transformer equivalent resistance	0.20253 $\Omega$
DC link capacitor	53.933 $\mu$ F
DC transmission line resistance	0.2 $\Omega$ /km
DC transmission line length	111km
External Network -1 (Mota side)	Short circuit power $S_k''=10,000$ MVA
	R/X= 0.041
External Network-2 (Debre Markos side)	Short circuit power $S_k''= 2000$ MVA
	R/X=0.21

The DC link in this study is required to provide reactive power support at either ends. Hence reactive power control is implemented at both ends. One of the converters is required to control the DC voltage then the other converter should control the active power. As a result, the control strategy chosen is that the VSC-1 controls reactive power and the DC-link voltage and VSC-2 controls active power and reactive power.

The complete control system set up for each side converter is shown at Appendix-B and the initialization codes developed and block status checks for each converter block is shown in Appendix-C.

The requirements expected from the control system are:

- Capability of controlling active power flow in either direction.
- The reactive power control at either ends must be carried out independent of each other.
- Independent control of active and reactive powers.

The control system test helps to insure effectiveness of the control system in achieving these objectives under normal and disturbed conditions.

#### **4.1.1 Active power flow direction reversal**

The purpose of this simulation is to show the effectiveness of the control system with regard to the variation of active power. Tasks done on active power by transmission system operator (TSO) at converter stations are scheduled amount power transfer and reversal of power flow direction. Here below the performance of the VSC-HVDC control system under power flow direction reversals is evaluated.

In this test case, the active power reference at the PQ-controller is reversed and increased from -1 pu to 1pu at 0.3s and at 0.7s the active power reference is again reversed from 1 pu to -1 pu. This orders a complete reversal of active power flow direction through the DC link. The simulation result shows; active power flows at the two grid sides showed direction reversal following the order as depicted in figure 4.2 (a).

The change in the reactive powers at the two ends is insignificant except some transients. This is shown in figure 4.2 (b). Hence, we can say that the control of active power flow is independent of reactive power.

Another important result is observed in figure 4.2 (c) regarding the converter bus voltages. Some voltage variation is observed on VSC-2 bus voltage. This variation is reasonable due to the fact that the occurrence of the disturbance is near this bus. But still the change is insignificant. On the other hand no variation is observed on VSC-1 bus voltage. This proves the fact that the change on bus voltages is dependent on reactive power changes but not on active power changes.

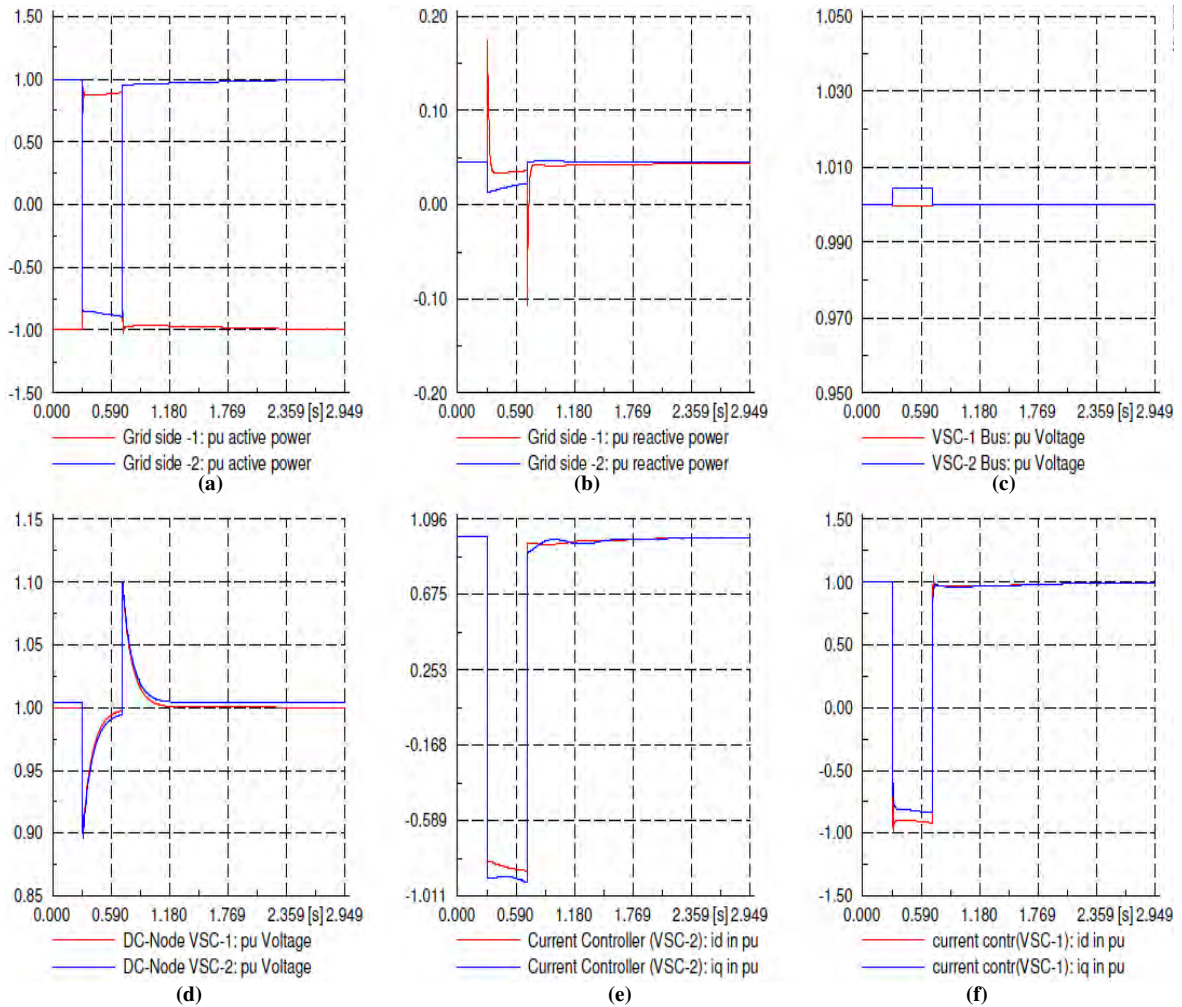


Figure 4.2: Transients at active power reversal

As seen from figure 4.2 (d), except during the transients, the DC link bus voltages are at the desired value of 1pu. The DC voltage transients show fast tracking of pre-disturbance value, proving the effectiveness of DC voltage controller. On the other hand, the d and q axis currents at the current controllers in figure 4.2 (e) and figure 4.2 (f) show variations from their initial values to achieve power reversals and maintain reactive power at the set value.

From these results we can conclude that active power reversal is effective and the designed controllers and control system are robust upon power reversals.

### 4.1.2 Reactive power control

Reactive power control is an important task that is done frequently within the transmission system. The system voltage is dependent on the reactive power provision within the system. Hence in order to ensure system voltage stability there should be effective control mechanism of reactive power. The reactive power control can also be used to damp out system power oscillations that arise following disturbances. Here below the control system performance is evaluated in reactive power control task.

In this test case, initially the reference value of reactive power is at zero. This is in an effort so as to achieve 1pu value of voltages at the converter buses. At 0.3 s the reference value of the reactive power is set to -1 pu. Then at 0.7s it is reversed and set again to 0.

The simulation result in figure 4.3 (b) shows that the reactive power at grid side-2 changes tracking the reference value but at grid side-1 it remains unchanged. This shows reactive power control at each converter is independent of one another. This is one of the requirements from the VSC-HVDC operation. The converter bus voltage at VSC-2 shows a step change from its pre-disturbance value as shown in figure 4.3 (c). When the reactive power returns to its pre-disturbance value, VSC-2 bus voltage returns to its nominal value of 1pu. This shows the dependency of bus voltage on the reactive power injected or absorbed to/from it. Bus voltage at VSC-1 bus shows no change due to the fact that the reactive power at this side showed no change. Hence, during contingencies TSO can monitor system voltage by adjusting the reference reactive power set value until desired system voltage is achieved.

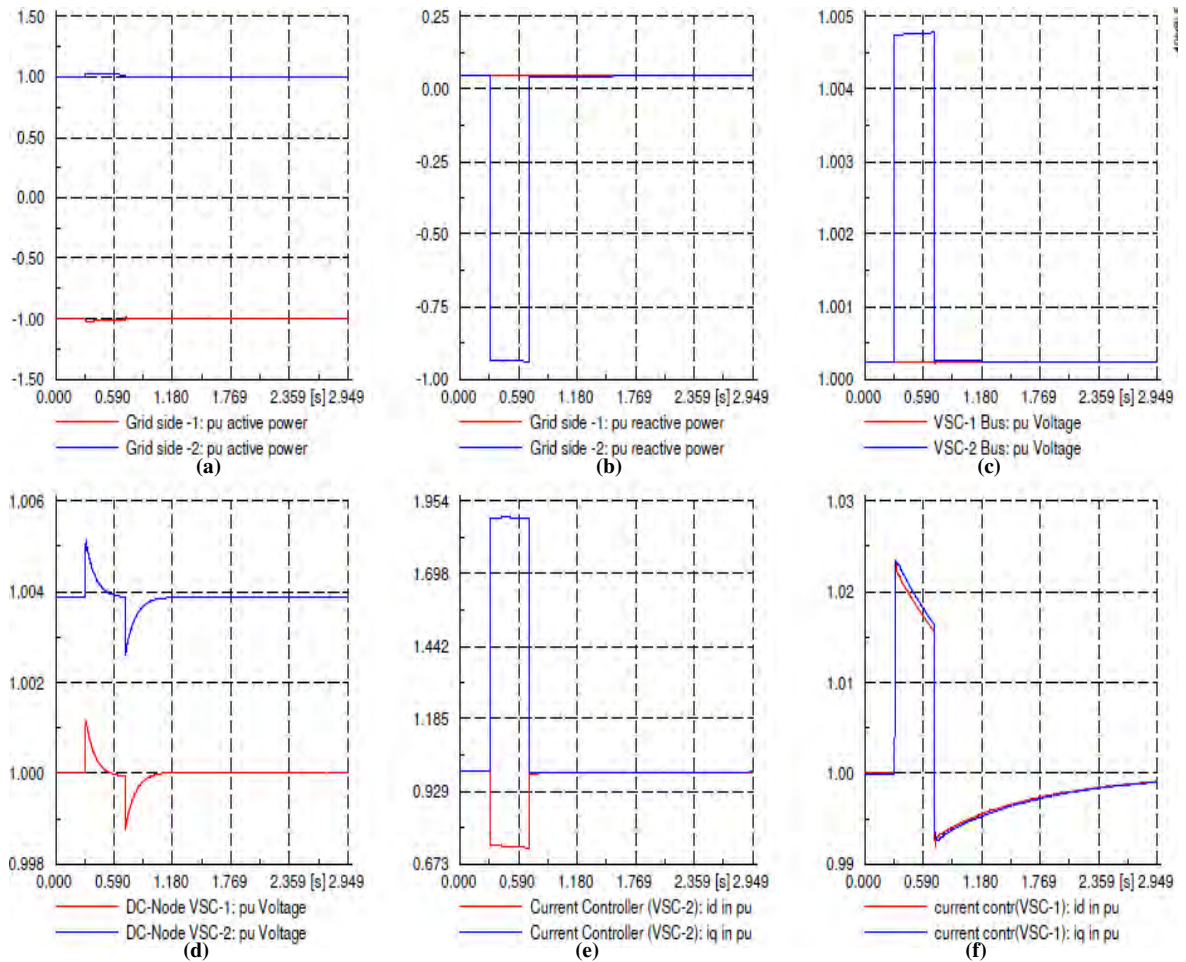


Figure 4.3: Responses for the step change of reference reactive power.

On the other hand, the active powers at the two grid sides remain unchanged as shown in figure 4.3 (a). This is what is expected from VSC-HVDC application, i.e. independent control of active and reactive power.

### 4.1.3 DC voltage step responses

Some times it may be necessary for TSO to transfer power across the DC link at a given DC voltage value so as to achieve some form of influence in the grid. This can be done through changing the DC voltage reference value. Here, below reference value of the DC voltage is changed from initial value and the performance of the control system is evaluated.

In this case, at 0.3 s the dc reference value,  $V_{dc\_ref}$  is increased from 1 pu value to a value 1.5 pu and then at 1s the value is again reduced to the value 1pu.

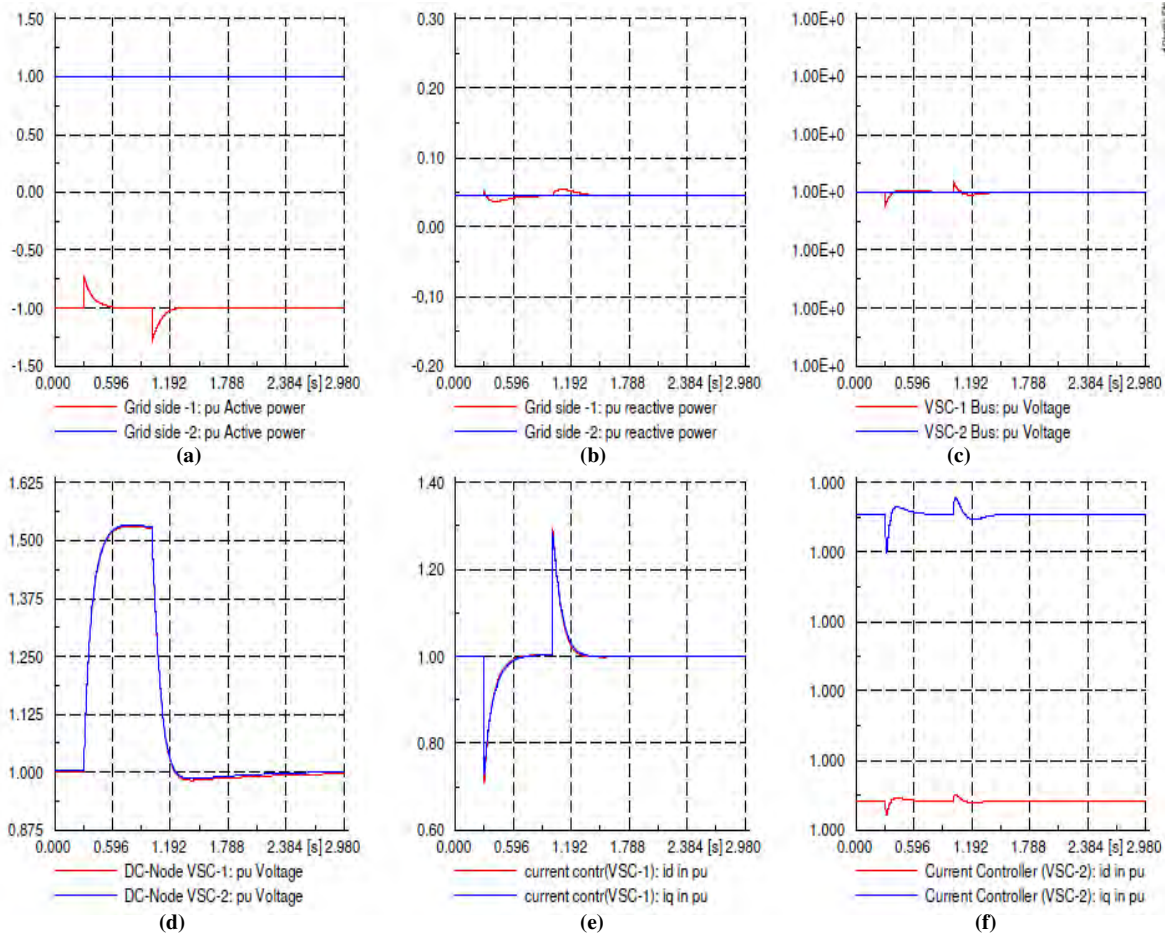


Figure 4.4: Transients at step change in  $V_{dc\_ref}$

The DC bus voltages show changes from 1 pu to 1.5 pu tracking the reference value as shown in figure 4.4 (d). The active power at grid side-1, in figure 4.4 (a), shows only transient peaks. This shows that the same power is being transferred at a different DC voltage value. Only the current controller on VSC-1 side showed some changes that quickly track the pre disturbance value as in figure 4.4 (e). Other changes to converter bus voltage and reactive powers are insignificant.

These simulations show that the designed control system achieved stability after dc voltage reference step changes and the requirement from the control system mentioned earlier is satisfied.

#### 4.1.4 Three phase to ground fault at VSC-1 Bus and VSC-2 Bus

Faults are the most common form of disturbances in power systems. Therefore, it is necessary to test the performance of the designed controllers upon the occurrence and the clearance of faults. The three-phase to ground faults are the most common type of faults in power grids.

In this test case, 3-phase to ground fault having fault impedance magnitude of  $0+j0$  is activated at the VSC-1 bus at 0.2s and cleared at 0.5s. The controllers maintained stability during the fault occurrence and achieved the desired system condition after fault clearance.

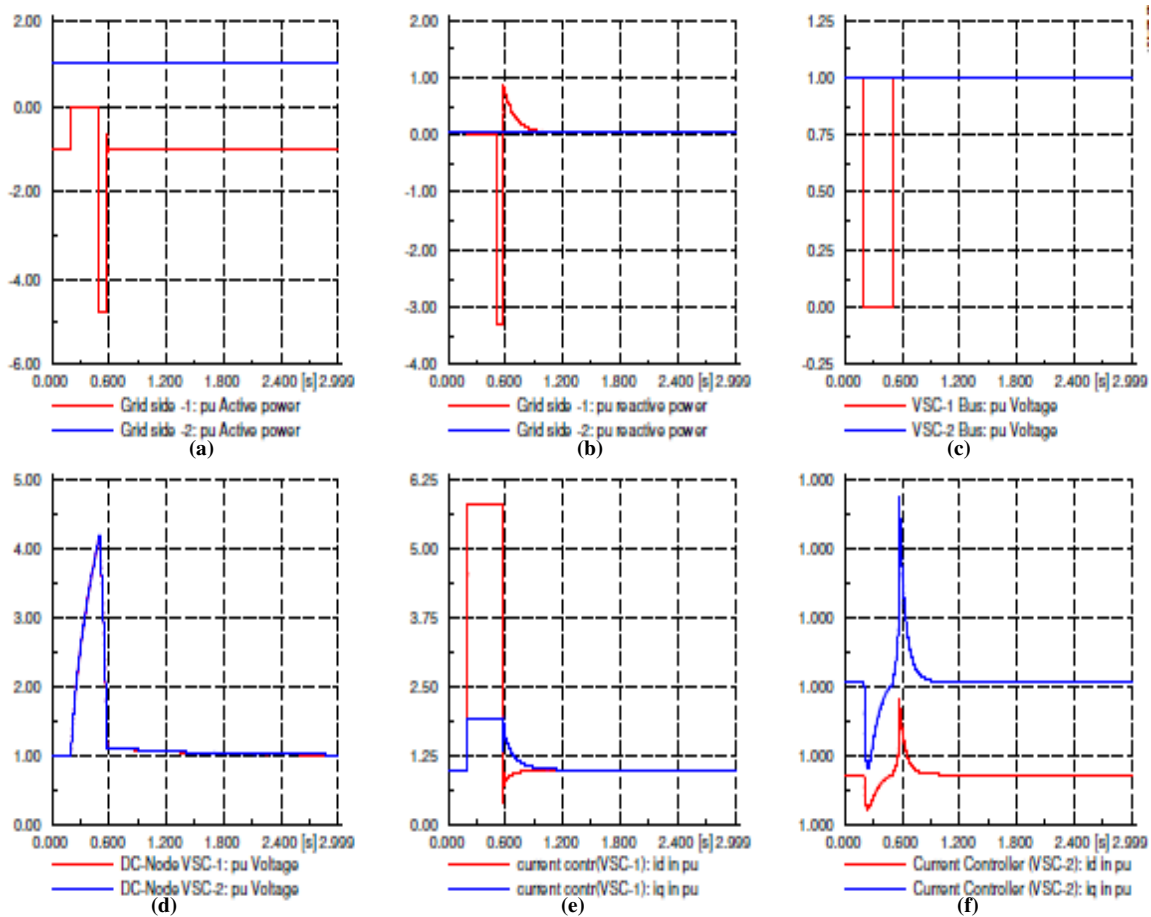


Figure 4.5: Transient response of the system for 3-phase to ground fault at VSC-1 bus

In grid side-1, as shown in figure 4.5 (a), active power is reduced to zero for the duration of the fault while grid side-2 active power is maintained at its pre-disturbance value. This indicates the delivery of active power to the DC bus capacitors which results in no power flows to grid side-1. But still grid side-2 active power flow is unchanged. This delivery of active power to the DC capacitors makes the DC bus voltages to show steep increase at the occurrence of the fault as in figure 4.5 (d). But when the fault is cleared the DC-bus voltages returned to their pre-disturbance values.

In figure 4.5 (b) the reactive power at grid side-1 shows a transient peak only at fault clearance time. But soon the required value of 0 MVar is restored. At the fault occurrence the Q-controller maintained required value of 0 MVar. This shows the Q-controller at VSC-1 achieved the desired task of maintaining reactive power at 0 MVar.

On the contrary, the converter bus voltage at VSC-1 side, as shown in figure 4.5 (c), is reduced to ground potential 0 pu even if the reactive power of this side is at 0 MVar. This shows the fact that ground faults at bus bars result ground potential 0 pu regardless of the compensation to the bus bar due to infinite charge accumulation of the earth. On the other hand, the converter bus voltage at VSC-2 remains at its pre-disturbance value. This is due to the grid reactive power support from VSC-2. Figure 4.5 (e) and (f) show transients are significant at VSC-1 side current controller dq-currents while at VSC-2 side current controller dq-current changes are undetectable, still at their pre disturbance value, 1pu. This is due to the fact that the occurrence of the disturbance is at VSC-2 side.

For the fault occurrence at VSC-2 bus, active power flow from Grid side-2 drops to zero as shown in figure 4.6 (a). This results in no active power flow through the DC link. Normally the flow of active power is from VSC-2 to VSC-1.

On the other hand, VSC-2 bus voltage dropped to ground potential 0 pu at the fault occurrence. But VSC-1 bus voltage shows no value change because VSC-1 is acting as a STATCOM providing this grid side with the desired reactive power. This is due to the fact that VSC converter at zero active power transfer acts as a STATCOM. This is shown in figure 4.6 (c).



In this fault case, figure 4.6 (d), the DC bus voltages show transients at disturbances but soon the transients show fast tracking of the pre-disturbance values after fault occurrence as well as after fault clearance. This shows that the DC voltage controller response is fast and hence, satisfactory.

The inner current controller dq-currents show value changes so as to achieve the desired active and reactive power control tasks.

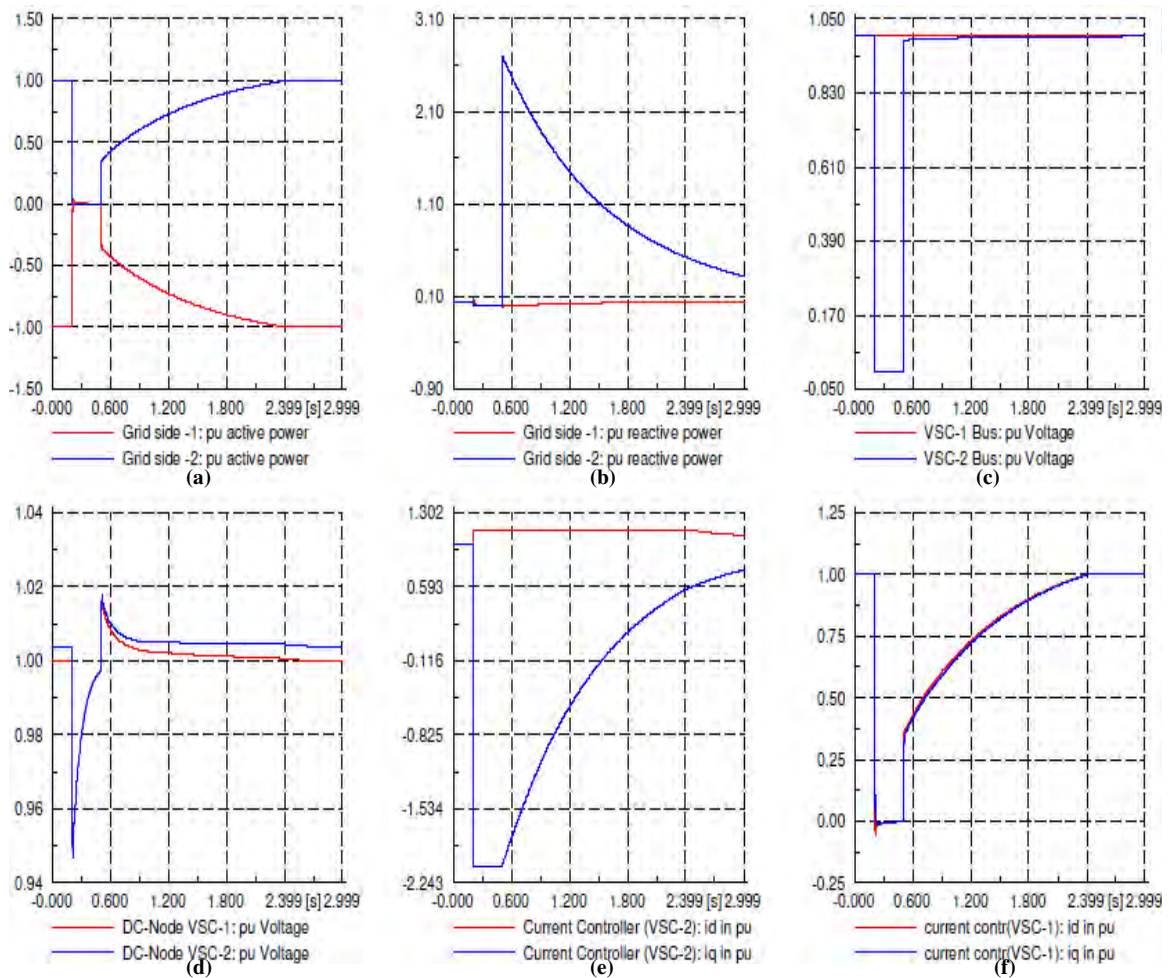


Figure 4.6: Transient response of the system for 3-phase to ground fault at VSC-2 bus

## 4.2 VSC-HVDC Integration to North-Western EEPCo System

The EEPCo system has two main parts: the interconnected system (ICS) accounting about 98% electric power supply coverage and the self contained system (SCS) accounting the remaining coverage.

The North Western and Northern EEPCo system is an important area of the ICS. It is this area that takes huge share of the future EEPCO's power generation. This part of EEPCo system covers the area From Dejen up to Northern most areas as Far as Endasellasi and Wokro. This part encompasses 4 huge power plants. Total load of the area currently, is about 182 MW active power and 131.508 MVar reactive power. The transmission system uses 66 kV, 132 kV, 230 kV and 400 kV transmission voltages.

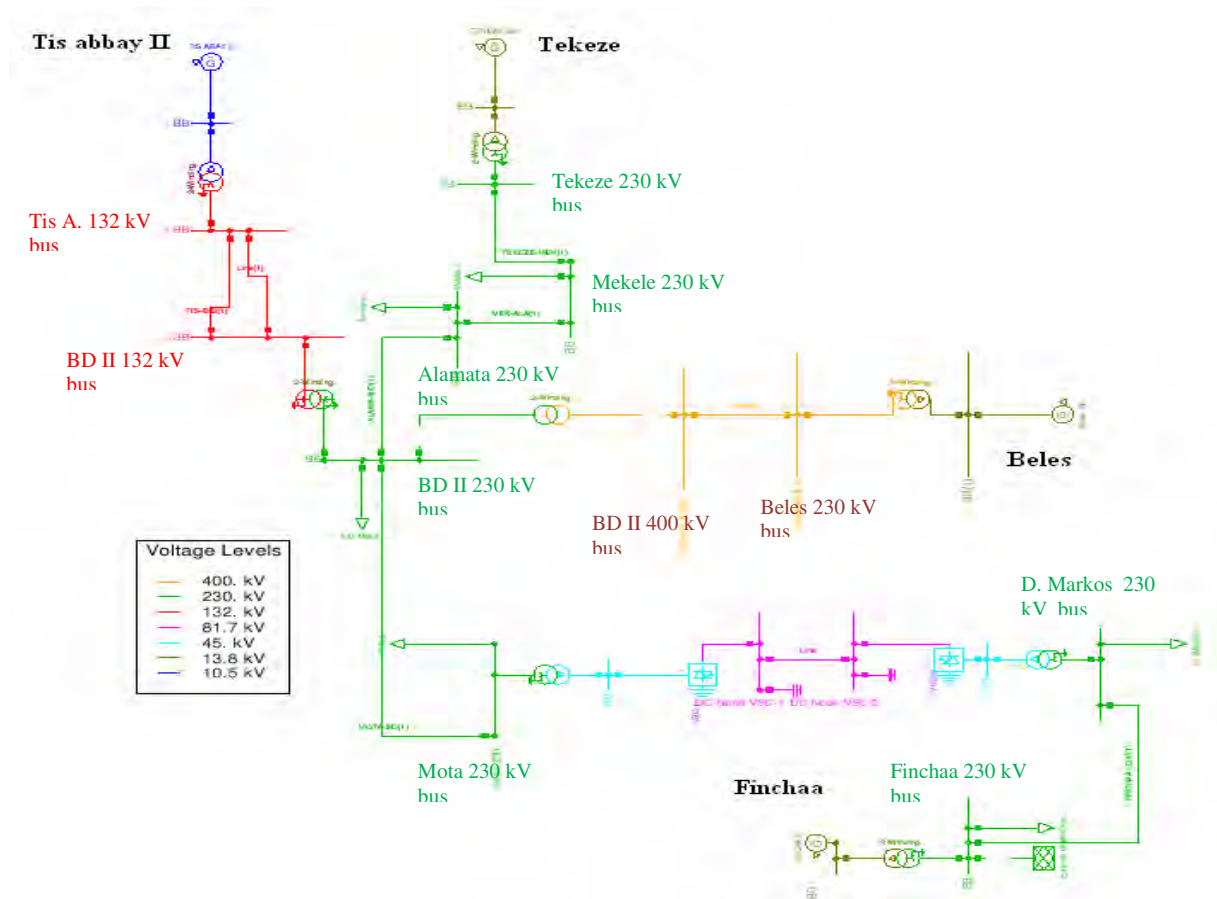


Figure 4.7: DIGSILENT model of the North-Western and Northern EEPCo system with VSC-HVDC

In the above figure, the north western EEPSCO power system is modeled on the DIgSILENT software. The network reduction is done based on the practices from [2, 15]. The network parameters are given in appendix A.

### 4.3 Simulation Results

The VSC-HVDC link is located between Mota and Debre Markos replacing the existing AC line. The power being transmitted through the AC line is, currently, 40 MW on the average.

Different incidents are activated and simulation results are shown with the designed VSC-HVDC link and with the existing AC transmission system (without VSC-HVDC).

The strategy here focuses on investigating the improvement on pre-disturbance as well as post-disturbance voltage profiles. The post disturbance bus voltage values determine the stability of power systems after fault occurrence [4, 5, 39]. Improved post disturbance voltages results in improved system stability after disturbances. The parameter under investigation is bus voltage pu magnitude. The discussion is made on some selected buses. Next the result on the remaining buses is shown.

The time domain simulation results below compare the bus voltage magnitudes at three phase to ground faults before VSC-HVDC integration (i.e. at AC transmission) and with VSC-HVDC transmission integration, at various disturbance incidences.

All the simulations start at reference time -0.1s. This helps to visualize the behavior of the simulation at the real simulation starting time 0s and adds clarity. Here the investigated contingency is the common three phase to ground fault. Three phase to ground fault of fault magnitude  $0+j0\Omega$  and fault duration 2.5 cycles which is equal to 0.5s is used. First let us discuss the effect of clearance time on post disturbance voltage profile and stability.

### 4.3.1 The effect of clearance time on the post disturbance voltage profile

Fault clearance times have impacts on the post disturbance voltage profiles. Here Tekeze 230 kV bus is chosen to show the effect of clearance times on EEPCo's system post disturbance voltage profile.

Three-phase to ground fault is initiated at Bahir Dar II 230 kV bus bar at 0.5 s of the simulation time. The voltage readings taken at 3.952 s gave 0.970 pu for clearance at 0.7s, 0.950 pu for clearance at 1s and 0.920 pu for clearance at 1.1s. This shows that as fault clearance time increases pu post disturbance voltages declines. Further increase of clearance times will lead to worse voltage profiles and system instability due to the increased duration of the disturbance.

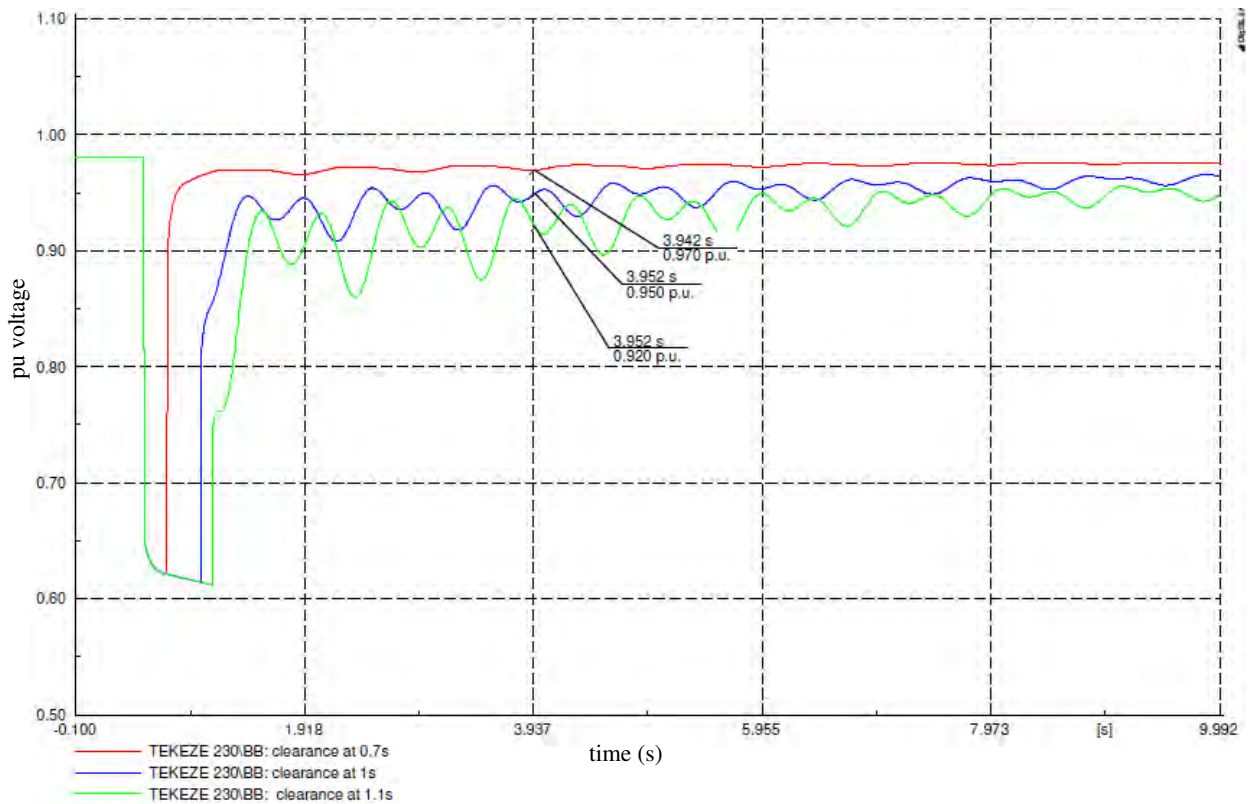


Figure 4.8: The effect of clearance time on post disturbance voltage profiles

Critical clearing time is fault clearance time beyond which the system enters to instability. Here in this test case further increasing the clearance time beyond 1.1s lead the system to lose

its stability. From this investigation from fault initiation time 0.5s to fault clearance time 1s is selected as optimum fault duration for the following simulations.

### 4.3.2 Post disturbance voltage profile and rotor angle stability with VSC-HVDC integration

Power system stability problems are interrelated. Voltage stability problems may manifest themselves as rotor angle instability and vice versa [4]. Thus improving one of the instability problems may improve a wide range of instability problems depending on the control actions made.

Here the focus is given to investigate the improvements at the pre disturbance as well as post disturbance bus voltage magnitudes. Mota 230 kV bus voltage profile is chosen for discussing the results.

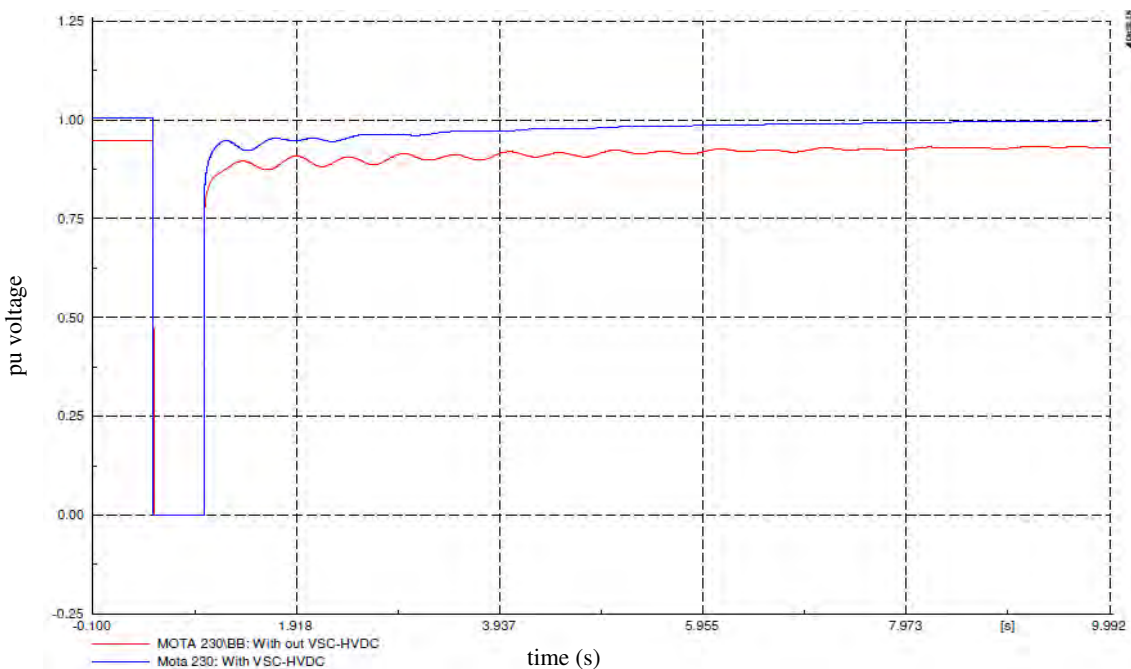


Figure 4.9: Voltage profile improvement at Mota 230 kV bus

The diagram shows pre disturbance voltage profile is improved. Before the integration of VSC-HVDC the pre disturbance voltage value (red line) is 0.93 pu below the acceptable limit of 0.95 but introducing VSC-HVDC shifts the value to 1 pu. Higher voltage is favorable at

reducing system power loss and improving system stability at steady state. At simulation time 0.5s 3-phase to ground fault is activated at this bus. Immediately the voltage of this bus bar falls to 0. This 0 value means the bus is at ground potential during the occurrence of the fault. The fault stayed for 2.5 cycles and cleared at 1s. After the fault clearance the voltage achieved at 1.2s is 0.88 pu before employing VSC-HVDC transmission but with VSC-HVDC integration the per unit voltage is improved to the value 0.95 pu. This is a significant improvement on the post disturbance voltage profile. At 8s the system restores its pre-disturbance voltage value with VSC-HVDC. However, without VSC-HVDC integration the system attains the pre disturbance value at 8.7s. This shows that a faster restoration of system condition is achieved by the proposed design solution. This is an indication that system robustness against transient events is improved.

The other important result obtained is that the bus voltages on the opposite side of the faulted area, i.e Fincha-230 kV bus and Debre Markos-230 kV bus, remain unaffected during the fault when VSC-HVDC is used, as shown in figure 4.10 below.

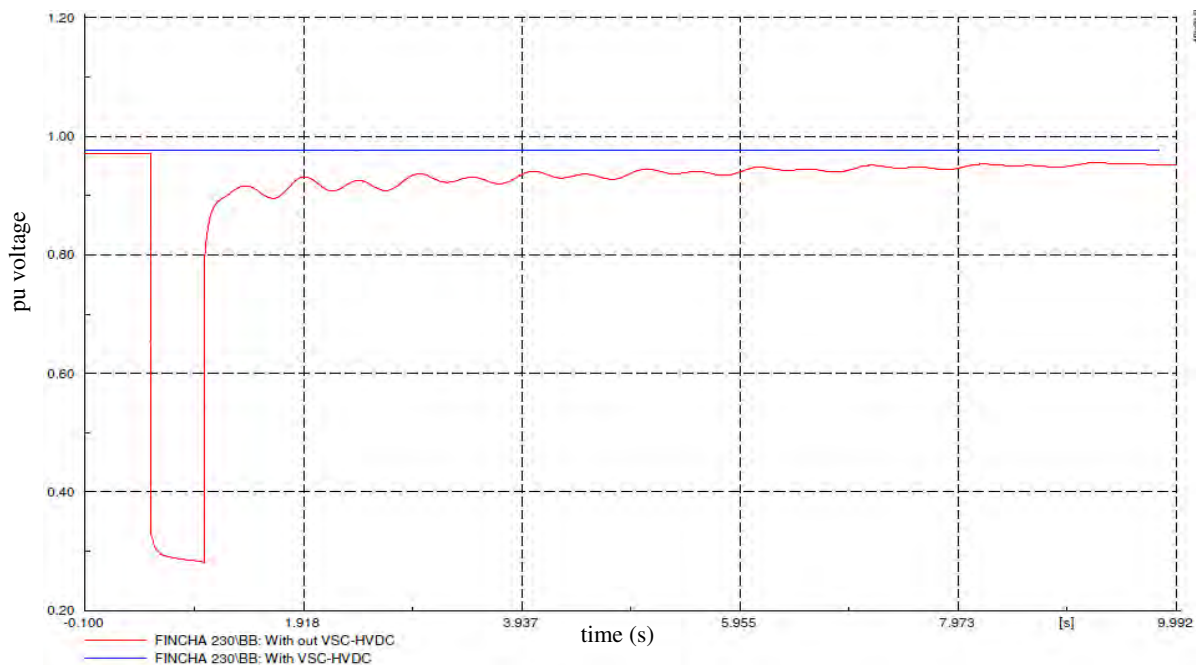
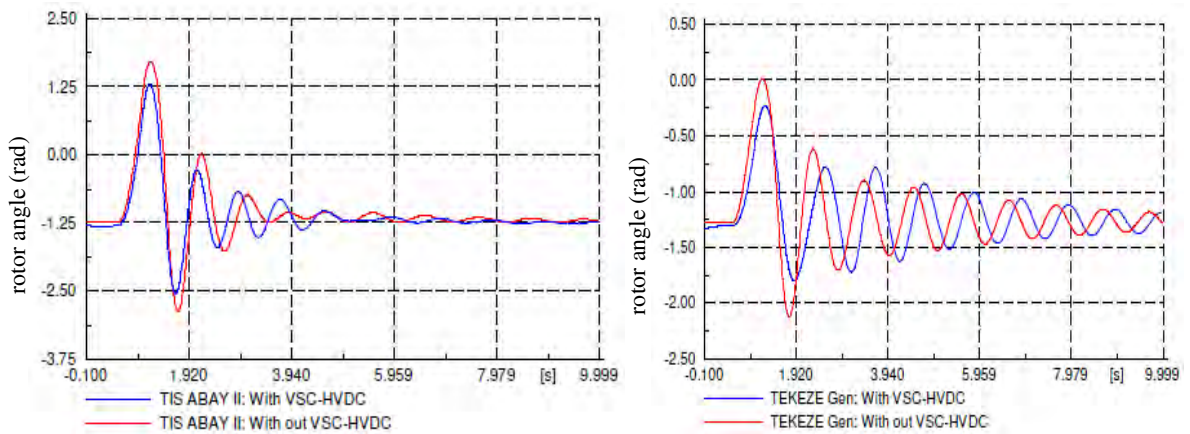


Figure 4.10: Bus voltage dynamics of Debre Markos 230 kV

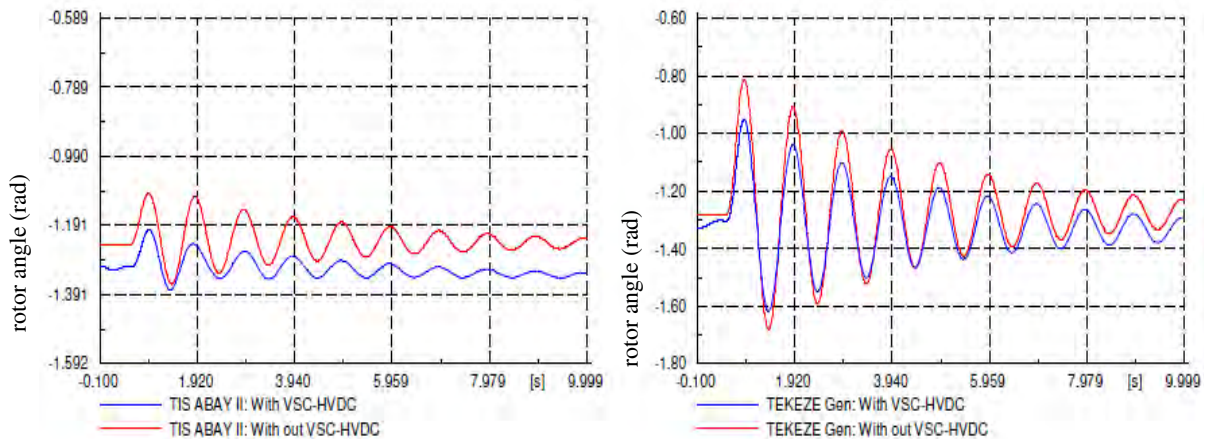
This shows that the HVDC link is acting as a fire wall for preventing instability spread and here station independent reactive power control is utilized to maintain these bus voltages near

desired value of 1pu. Debre Markos 230kV bus is located at the other end of the VSC-HVDC link from the faulted point. The VSC-HVDC link prevented the instability not to be transmitted to this end. The converter at Debre Markos side effectively monitored the voltage in the area and maintains it at desired value of 1 pu during and after the occurrence of the fault. The occurrence of the fault has no impact on this side. Thus here instability spread prevention is effectively achieved.

Another important result obtained is with regard to rotor angle oscillation. The rotor angle oscillation of Tis abay II generator and Tekeze generator are shown below in figure 4.11 with Beles generator as reference machine.



a) Fault at Bahir Dar II 230 kV bus



b) Fault at Mekele 230 kV bus

Figure 4.11: Tis abay II and Tekeze generator rotor angle oscillations

These rotor angle oscillation illustrations depict in all cases first swing angle stability is improved with VSC-HVDC. This is the stability of the first swing of the rotor. More over with out VSC-HVDC the generators experience larger and longer oscillations. But when VSC-HVDC is integrated the oscillations are damped and their life span some what shortened.

This rotor angle stability achievement accounts to the active power control task of the P-controller at the VSC-HVDC link.

This result shows that it is also possible to bring rotor angle stability by integrating VSC-HVDC to the EEPCCo system.

### **4.3.3 Post disturbance bus voltage profile of the over all system**

In the previous section, the improvement achieved is discussed using selected buses. The improvements are not restricted to these buses and the faults that are being managed are not only at Mota 230 kV. Here below faults at different locations are initiated and the improvement over all the bus bars is illustrated from figure 4.12 to figure 4.15. In all cases, the three-phase to ground faults with fault impedance magnitude  $0+j0$  are initiated at 0.5s and cleared after 2.5 cycles (in 50 Hz system) at 1 s.



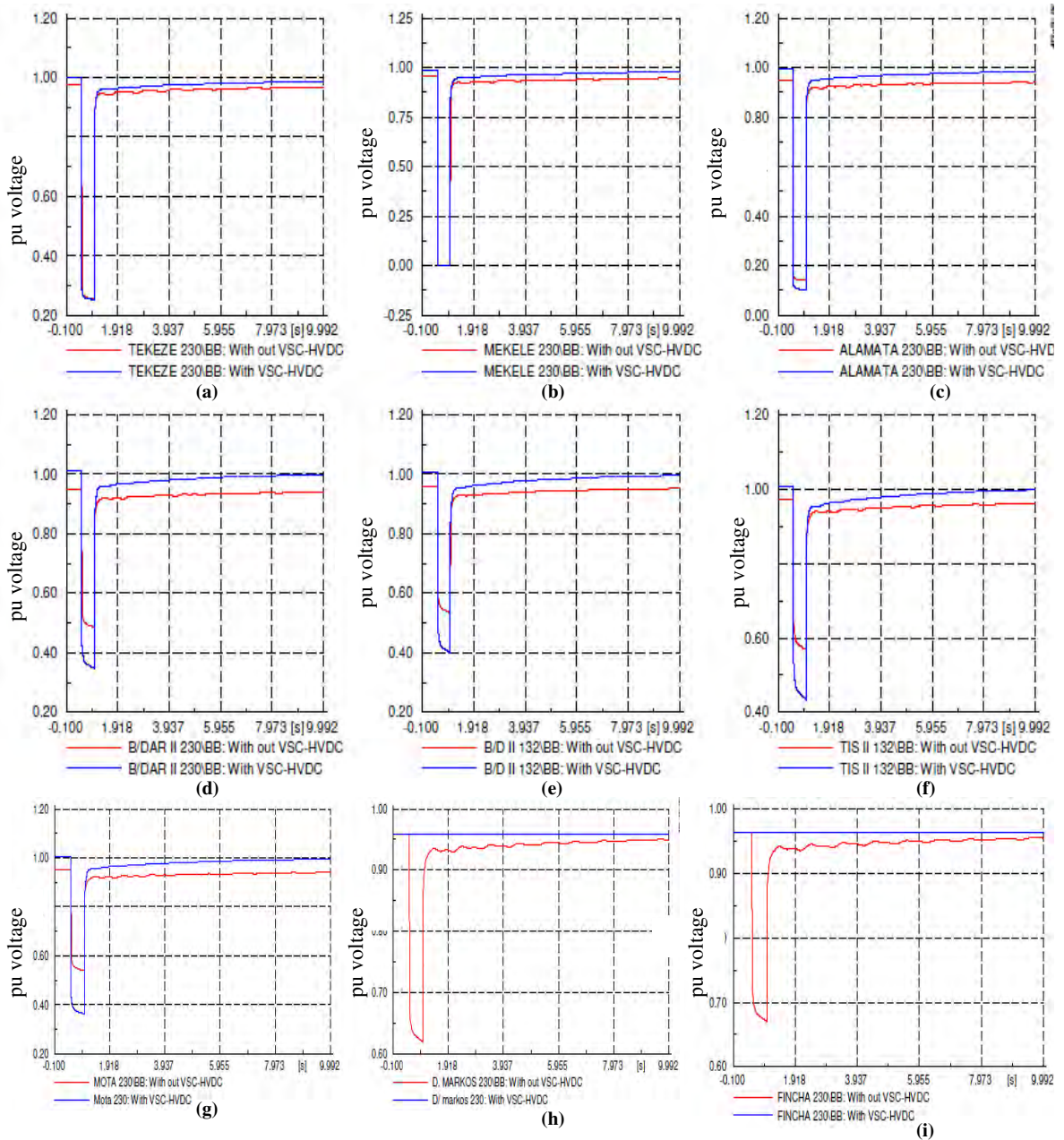


Figure 4.12: Bus voltage dynamics with and with out VSC-HVDC for a fault at Mekele 230kV bus.

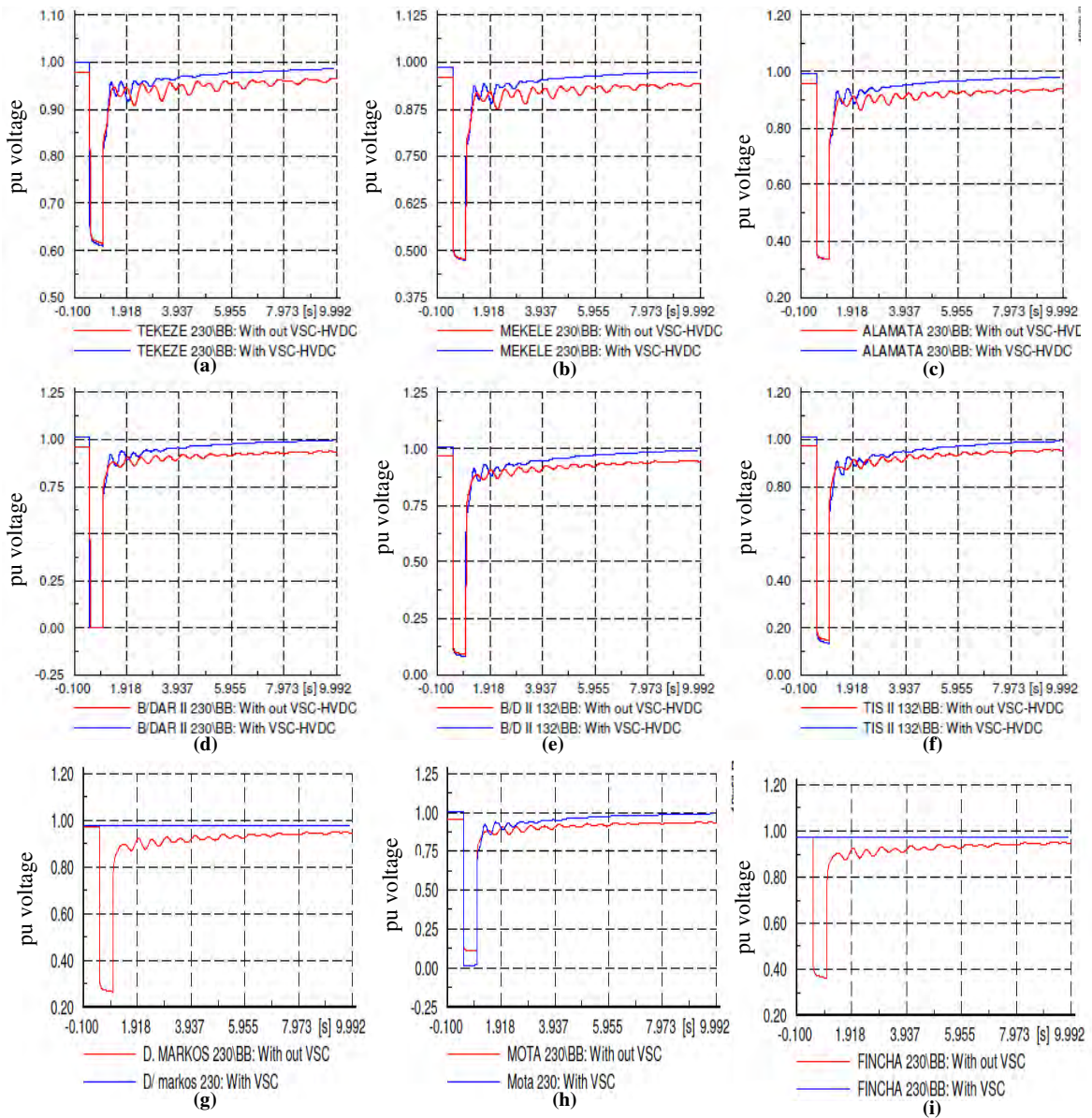


Figure 4.13: Bus voltage dynamics with and with out VSC-HVDC for a fault at Bahir Dar II 230kV bus.

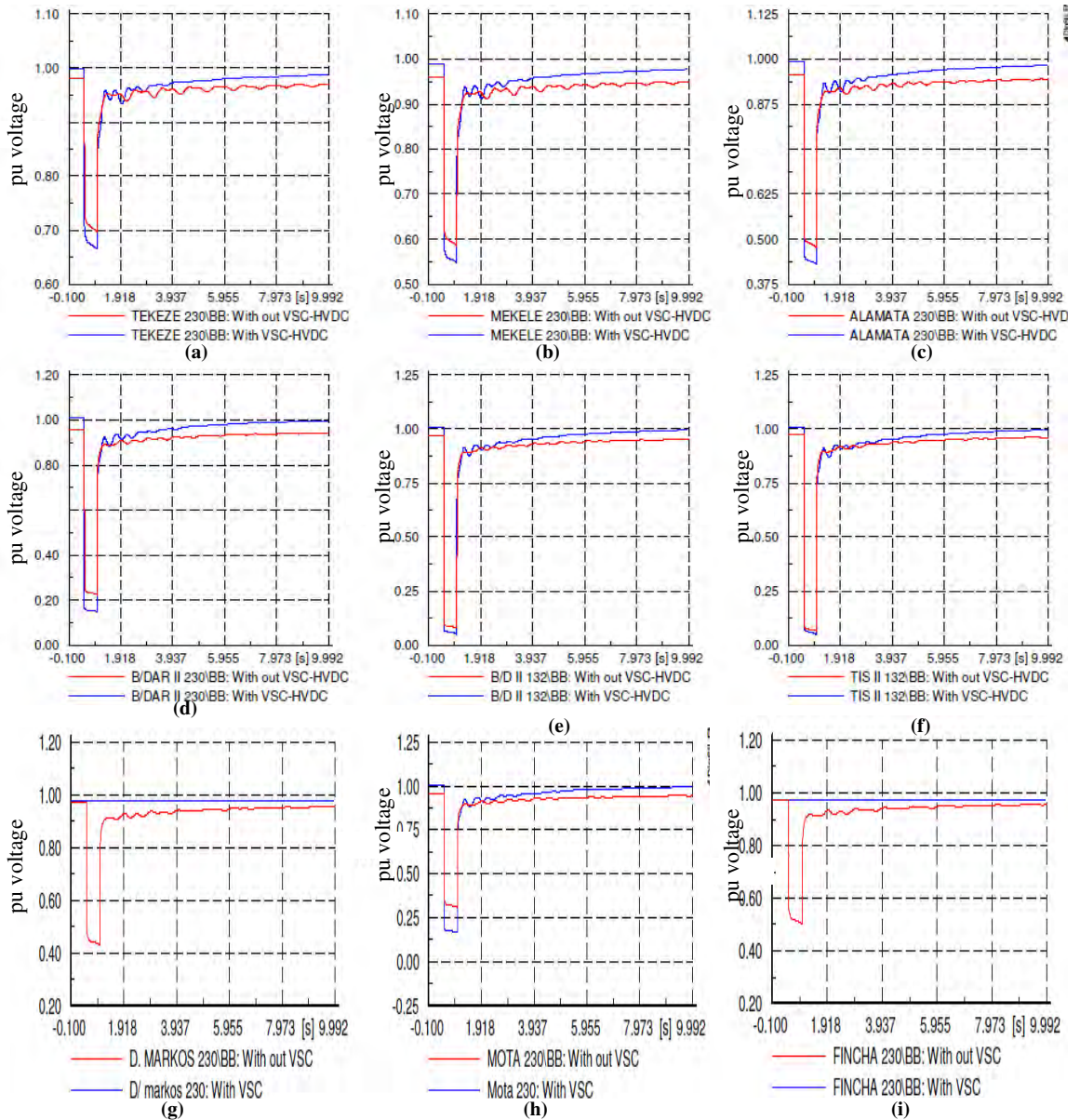


Figure 4.14: Bus voltage dynamics with and with out VSC-HVDC for a fault at one of the double line from Tis Abay II to Bahir Dar II.

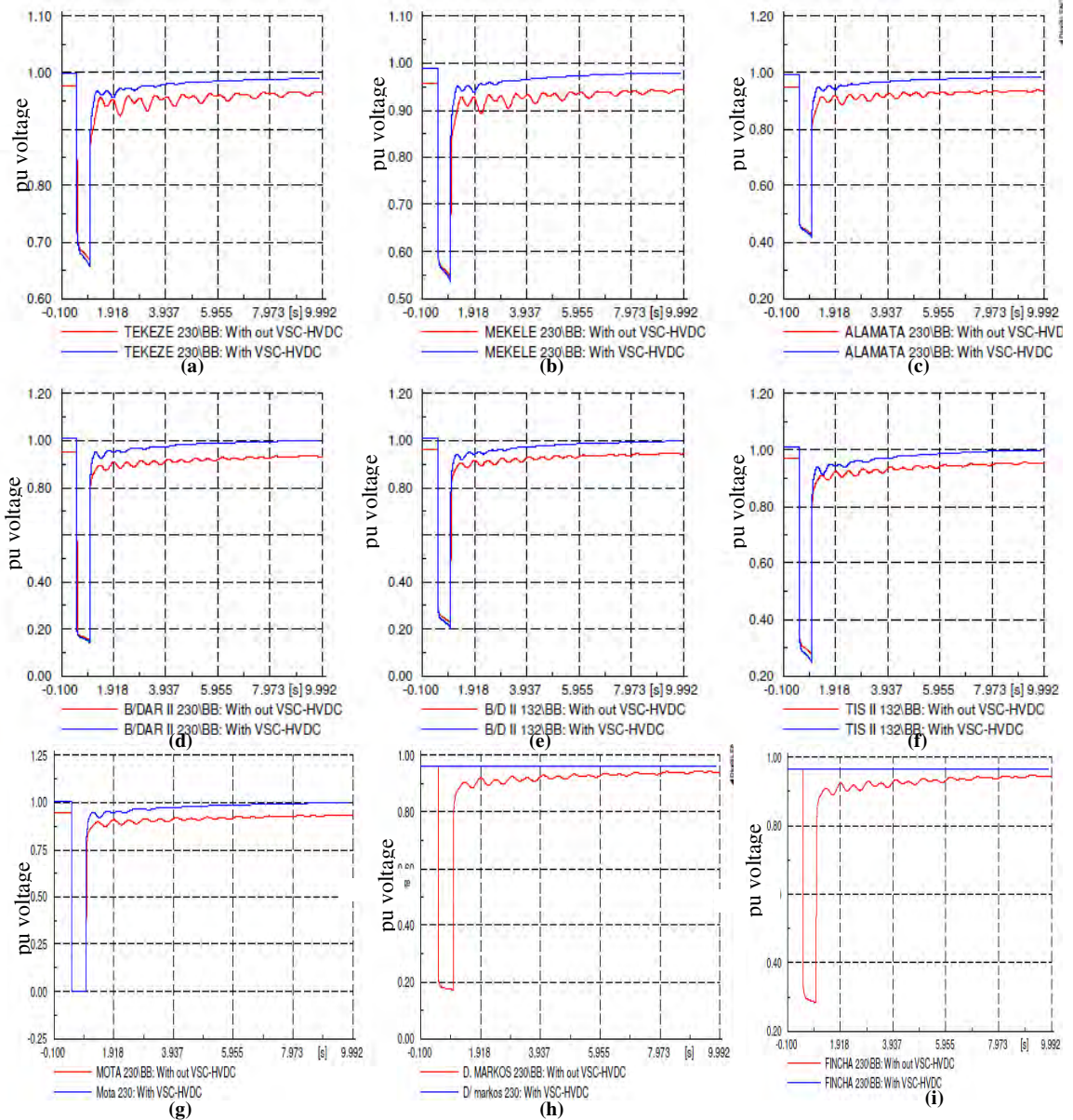


Figure 4.15: Bus voltage dynamics with and with out VSC-HVDC for a fault at Mota 230kV bus

These simulation results show that the pre disturbance as well as the post disturbance pu value of bus bar voltages is improved upon integrating the proposed VSC-HVDC link. More over they reveal that more sounding improvement is obtained at bus bars that are near the inserted VSC-HVDC link. The VSC-HVDC link also prevented the instability not to be transmitted to the other end.

#### 4.3.4 AC-DC grid operation at half load and average load

The above simulation cases are made at peak load condition where the consumer needs much energy. This high energy demand makes the system voltage profile to decline. The proposed method showed effectiveness at serious grid condition of peak load. But it is also necessary to deal about the operation of the AC-DC grid during low power demands and associated tasks done at reactive power planning during this low load conditions. The following illustration compares the voltage profiles of the AC-DC grid at half load, average load and peak load conditions. The fault is activated at Mota 230 kV bus and Bahir Dar II 132 kV bus is selected for discussion.

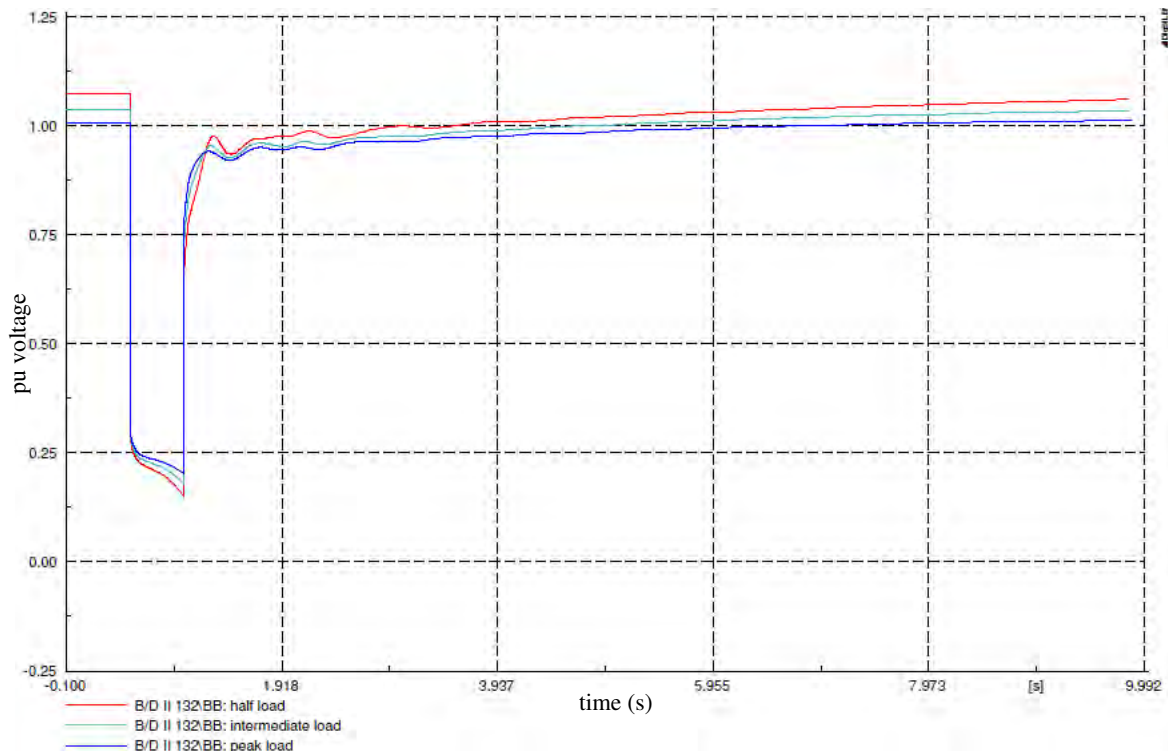


Figure 4.16 Bahir Dar II 132 kV bus voltage profile at different system load.

In this figure at half load 1.042 pu, at average (intermediate) load 1.016 pu and at peak load 1.015 pu bus voltage magnitude is obtained. During half load condition the system pre-disturbance voltage profile increase above the peak load bus voltage value. Most of the pre disturbance bus voltage profiles of other buses are near 1.05 pu which is the upper boundary of the N-0 contingency criteria. The N-0 contingency criterion is satisfied for bus voltages between 0.95 pu- 1.05 pu. Higher voltages beyond this limit usually cause trippings by over

voltage circuit breakers at substations. More over they cause power system equipment malfunctioning.

The high voltage profiles at low system loads are required to come to the safe region towards 1 pu. This is done through changing the reactive power set point at Mota side VSC station. Accordingly the reactive power reference value at Mota side VSC is set at -10 MVar and -20 MVar, respectively during half load condition. This brings the reduction of bus voltage profiles from their uncompensated half load values as shown below in figure 4.17.

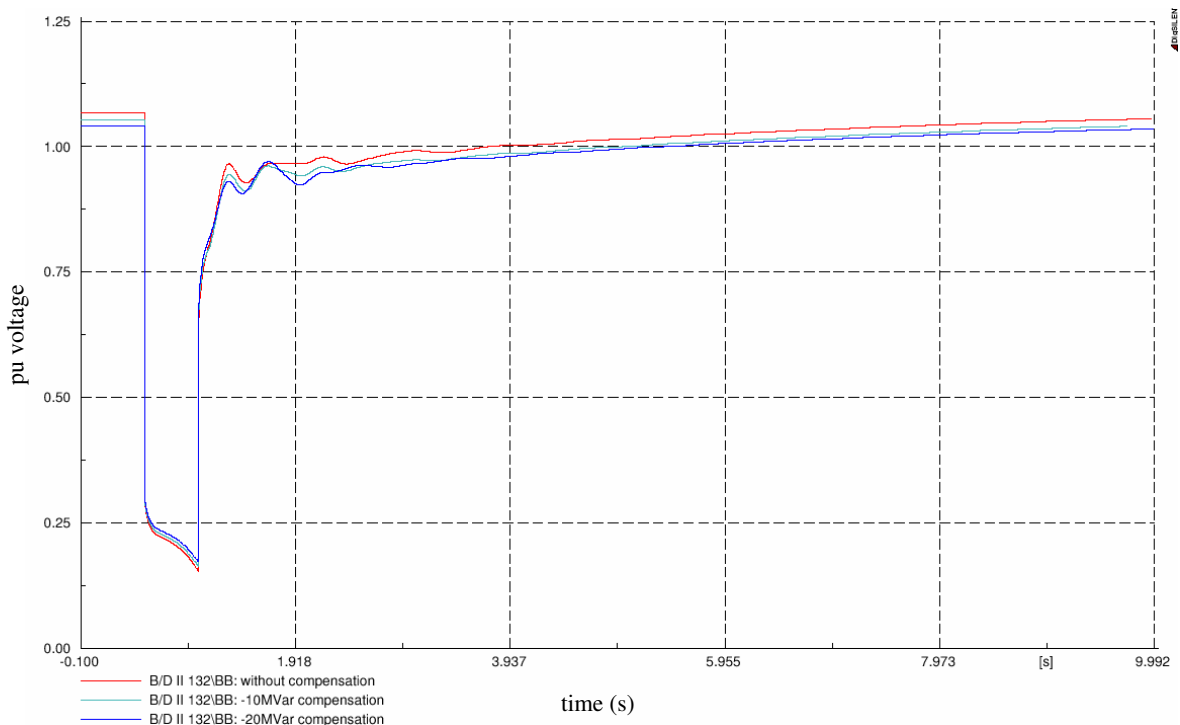


Figure 4.17 Bus voltage profile control through reactive power compensation

At half load with out compensation the bus voltage value at Bahirdar II 132 kV bus is 1.042 pu. To lower the system voltage level in two steps -10 MVar and -20 MVar reactive power is injected to the system (i.e. reactive power absorption). Finally bus voltage values 1.037 pu for -10 MVar compensation and 1.021 pu for -20 MVar compensation is achieved. This shows the possibility of maintaining desirable system bus voltage by controlling the reactive power set point at converter stations.

Coming to the post disturbance pu voltage values, reactive power compensated cases showed better post disturbance voltage profiles as shown above. Similar result is obtained for other buses. Here below Mekele 230 kV and Tis Abay II 132 kV bus voltages are shown below.

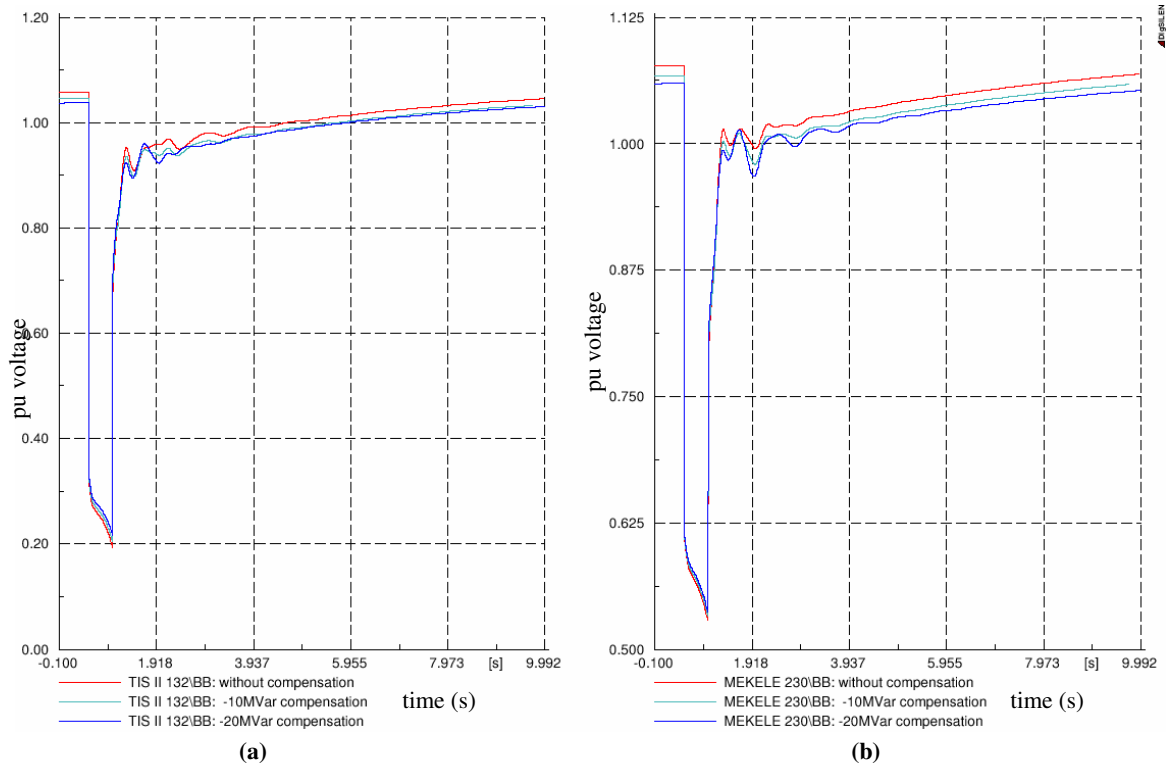


Figure 4.18 Tis abay II 132kV and Mekele 230 kV bus voltage profiles upon reactive power compensation

## CHAPTER 5

### CONCLUSIONS, RECOMMENDATIONS AND SUGGESTIONS FOR FUTURE WORK

Through the work done on this thesis the following conclusions are drawn.

#### 5.1 Conclusions

From the controller tests we can conclude the following:

- Bidirectional power flow and independent active and reactive power control is achieved by the designed controllers and control system.
- The designed control system is stable against the common disturbances that occur in the power system which include transmission system operator interventions and faults.

From the simulation results and the analysis made upon integrating VSC-HVDC link to North-Western EEPCo system the following important conclusions are drawn:

- Post disturbance pu bus bar voltage magnitudes, which determine the stability of a power system after contingency, are improved from below 0.9 pu to above 0.95 pu.
- Fast, i.e within 7 seconds, restoration of pre disturbance bus voltage value after fault clearance is achieved with VSC-HVDC transmission integration. With out VSC-HVDC most buses take above 9 seconds to regain pre disturbance voltage value.
- Similarly pre disturbance pu voltage magnitude is improved from below 0.95 to around 1 pu. Higher voltage magnitudes around 1 pu mean lower system power loss. This shows that integrating VSC-HVDC help at reducing EEPCo system significant power losses at steady state operation.
- Rotor angle oscillation of generators is damped after introducing VSC-HVDC to the system. This is due to the active power controlling task of the P-controller.



- Low load higher bus voltage profiles that go beyond the upper N-0 contingency criteria limit are monitored through reactive power control from the converter stations.

Generally, this work shows that the EEPCo system dynamic performance can be enhanced upon utilizing HVDC transmission based on VSC.

## **5.2 Recommendation**

Based on the result of this thesis work, it is strongly recommended that EEPCo has to consider the integration of VSC-HVDC transmission to its upcoming large power system to maintain the system stability thereby improving over all system power transfer capability and reduce huge power losses in the system.

## **5.3 Suggestions for Future Works**

- Optimization of VSC-HVDC transmission costs considering converter topologies, DC transmission medium costs, DC-transmission schemes, and future power electronics cost trends to make the option economically attractive.
- Technically, assessment of the power transfer capability improvement at the upcoming EEPCo transmission system, brought by integrating VSC-HVDC system, can be studied. This helps to make energy-cost analysis which will be added in the cost analysis.

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## APPENDICES

### Appendix A: Northern and North-Western EEP Co model system data

Table A.1: Transmission line data

Transmission Line	Length (km)	R (ohm/km)	X (ohm/km)	C (nF/km)	Diameter (mm)
Fincha-Debre markos	71.36	0.0597	0.4113	8.9	570.2
Debre markos-Mota	111.8	0.0597	0.4113	8.9	570.2
Mota-Bahirdar II	81.1	0.0597	0.4113	8.9	570.2
Tisabay II-Bahirdar II	28.96	0.1836	0.4228	8.7	180.7
Bahirdar II-Alamata	348	0.0918	0.3193	11.4	180.7
Alamata-Mekele	140.7	0.0918	0.3193	11.4	180.7
Mekele-Tekeze	103	0.0739	0.4142	8.9	394.0

Table A.2: load data

Load Center	Active power (MW)	Reactive power (MVar)
Mekele	44.02	31.7893
Alamata	3.528	3.6162
Bahirdar	30.68	20.617
Mota	0.88	0.59135
Markos	6.3	2.42219
Finchaa	7.1545	4.8285

Table A.3: Generator data from ARIVA [37] with some assumptions

Parameters	Finchaa	Tis Abbay	Beles (approximated)	Tekeze (approximated)
Ta (s)	6.39	6.0	6.19	5.59
Tg (s)	0.23	0.175	0.2	0.18
ra (pu)	0.0022	0.0045	0.032	0.025
Xas (pu)	0.1	0.1512	0.13	0.1
xd'' (pu)	0.13	0.26	0.19	0.2
xd' (pu)	0.23	0.42	0.25	0.3
xq'' (pu)	0.207	0.26	0.23	0.35
xq' (pu)	0.4	0.6	0.6	0.3
Td'' (s)	0.03	0.05	1.	0.04
Td' (s)	1.0	1	1.06	1.0
Tq'' (s)	0.02	0.05	0.06	0.03
Tq' (s)	0.9	0.9	1.0	0.9

Table A.4: Governor Data of the generators from ARIVA [37] with some assumptions

Parameters	Finchaa	Tis Abbay	Tekeze (approximated)	Beles (approximated)
R	0.05	0.05	0.04	0.05
R	0.70	0.50	0.50	0.6
Tr	12.0	5.00	8.408	12
Tf	0.02	0.05	0.05	0.03
Tg	0.10	0.20	0.50	0.5
Tw	2.40	1.00	0.496	2.5
At	2.50	2.50	1.15	2.5
Pturb	0.00	0.00	0.00	0.0
Dturb	0.30	0.30	0.30	0.30
Qnl	0.08	0.08	0.08	0.08
Gmin	0.00	0.00	0.00	0.0
Qnl	0.50	0.50	0.50	0.6
Velm	0.04	0.20	0.20	0.04
Gmax	1.00	1.00	1.00	1.00

## Appendix B: DiGSILENT implementation of the controllers

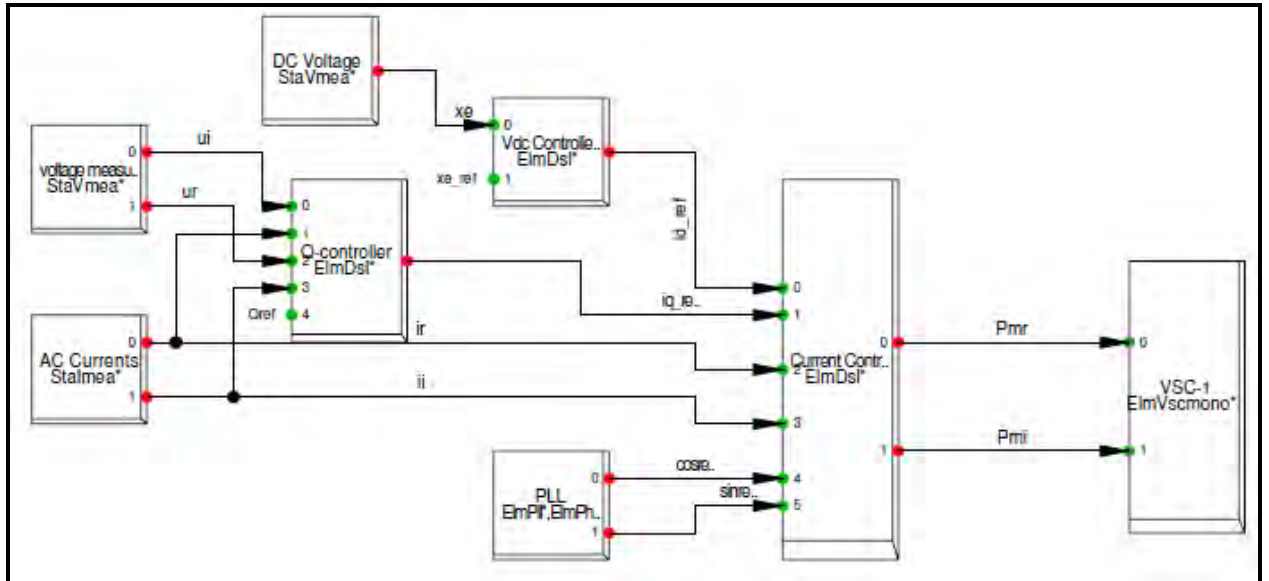


Figure B.1: Control system set up of VSC-1

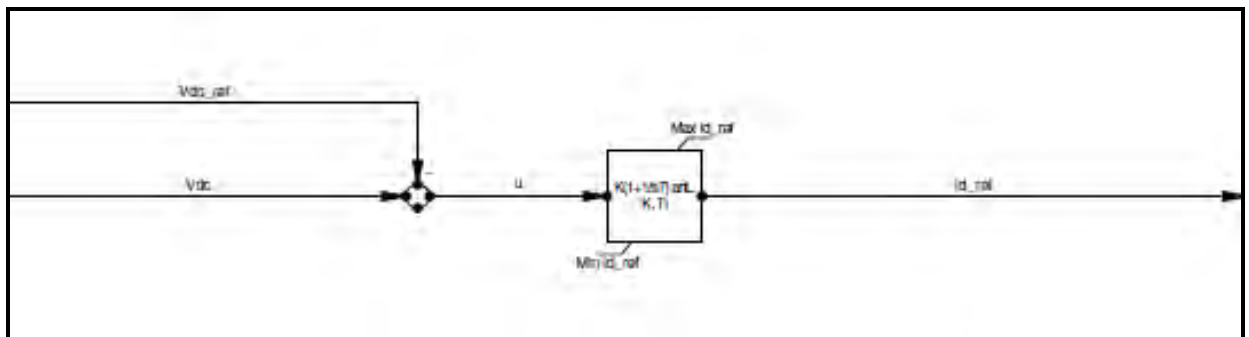


Figure B.2: The voltage controller



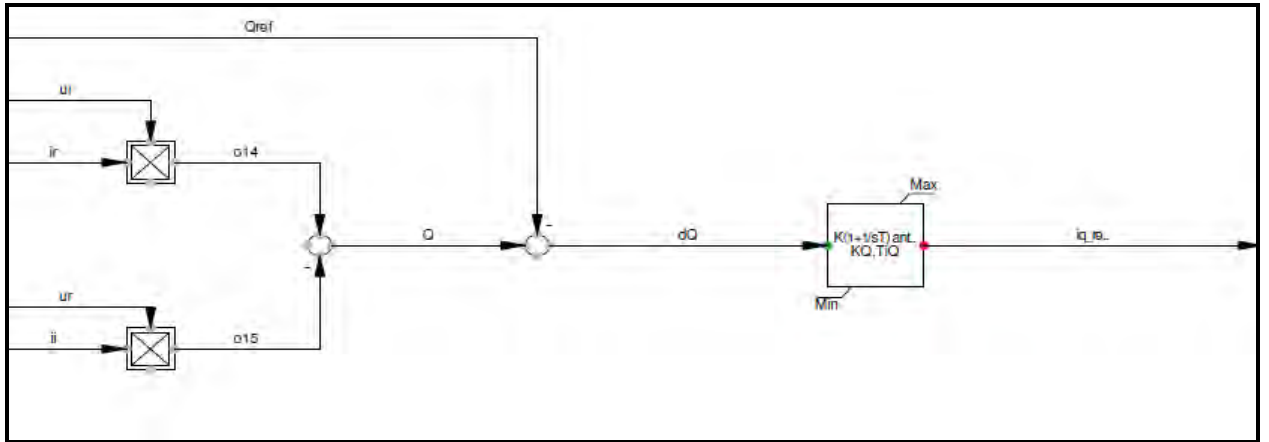


Figure B.3: Q-controller

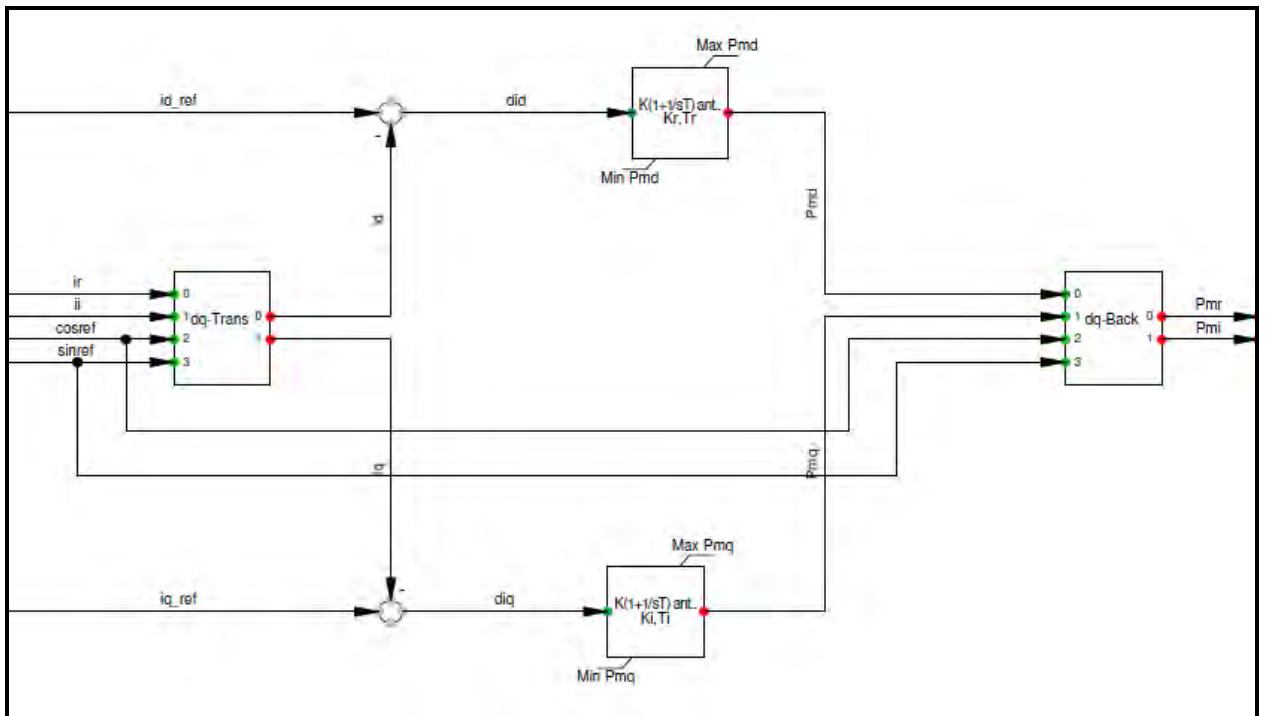


Figure B.4: The inner dq-current controllers

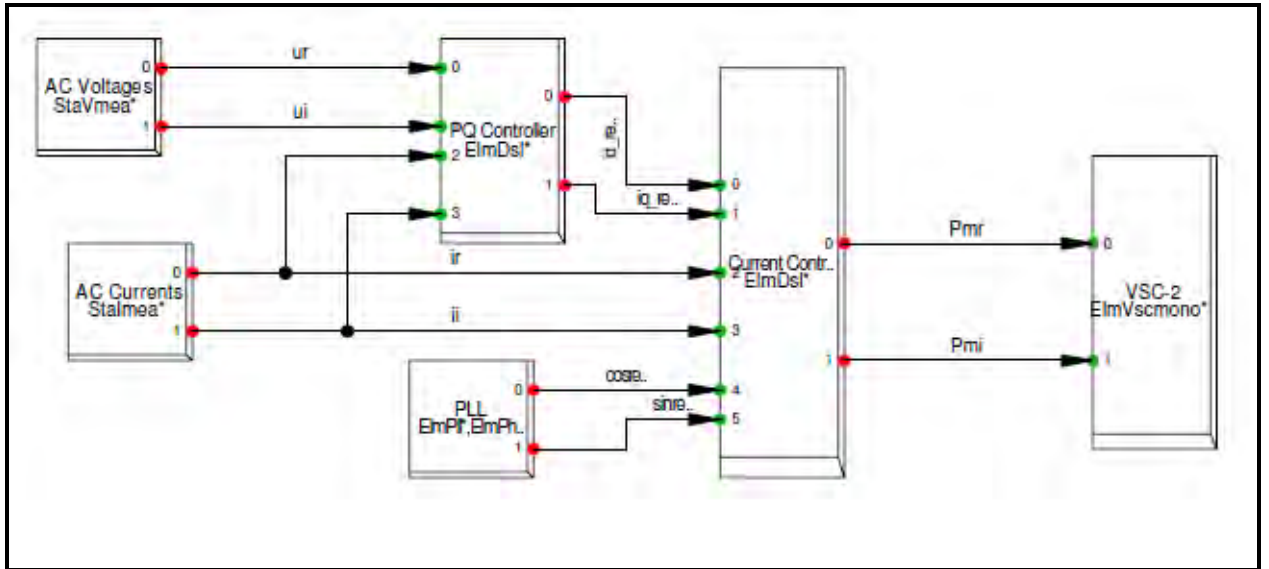


Figure B.5: VSC-2 control system set up

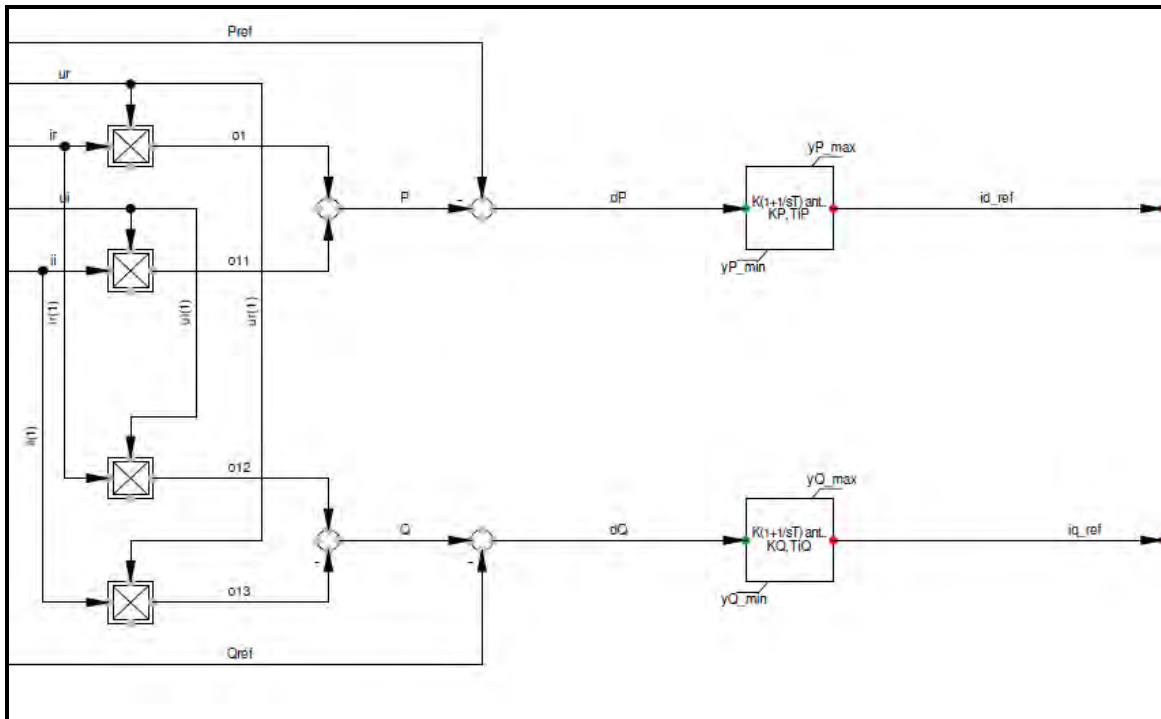


Figure B.6: The PQ-controller

## Appendix C: Controller equations, initial condition codes and block status checks on DIgSILENT

### C.1 Q controller at VSC-1 codes

DIgSI/info - Equations of '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Q-controller.Bl

```
!
-----
model iq_ref = 'Q-controller'(Qref,ui,ir,ur,ii;xiQ;KQ,TiQ,Min,Max;b0,b1,dev,yunb,Q,dQ,o14,o15)
  iq_ref = '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models\con_PQ.BlkDef\Used Macr
  o14 = ir*ui
  o15 = ii*ur
  dQ = Q-Qref
  Q = -o15+o14
  inc(xiQ)=iq_ref*TiQ/KQ
  inc(Qref)=Q
```

DIgSI/info - Check initial conditions of '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\
DIgSI/info - Variable may be used in output(), fault(),event()

set derivations to zero:  
xiQ.=0 => 0=dev

existing initial conditions:  
inc(Qref) =Q  
inc(xiQ) =iq\_ref\*TiQ/KQ

existing definitions/assignments:  
iq\_ref =lim()  
b0 =KQ  
b1 =KQ/TiQ  
dev =dQ  
yunb =b1\*xiQ+b0\*dQ  
Q =-o15+o14  
dQ =Q-Qref  
o14 =ir\*ui  
o15 =ii\*ur

DIgSI/info - Check '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Q-controller.BlkDef':  
DIgSI/info - Variable may be used in output(), fault(),event()  
DIgSI/info - Block is ok.

## C.2 DC voltage controller codes

DIgSI/info - Equations of '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Mo

```
! _____  
model id_ref = 'Vdc controller'(Vdc_ref,Vdc;x1;K,Ti,Min id_ref,Max id_ref;b0,b1,dev,yunb,dVdc)  
  id_ref = '\Demo.IntUser\UPFC.IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models  
  dVdc = Vdc-Vdc_ref  
  inc(Vdc_ref)=Vdc  
  inc(x1)=id_ref*Ti/K
```

DIgSI/info - Check initial conditions of '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\  
DIgSI/info - Variable may be used in output(),fault(),event()

```
set derivations to zero:  
  x1.=0 => 0=dev
```

```
existing initial conditions:  
  inc(Vdc_ref) =Vdc  
  inc(x1) =id_ref*Ti/K
```

```
existing definitions/assignments:  
  id_ref =lim()  
  b0 =K  
  b1 =K/Ti  
  dev =dVdc  
  yunb =b1*x1+b0*dVdc  
  dVdc =Vdc-Vdc_ref
```

DIgSI/info - Check '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.In  
DIgSI/info - Variable may be used in output(),fault(),event()  
DIgSI/info - Block is ok.

### C.3 Inner current controller codes

DIgSI/info - Equations of '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\curre\_con VSC-1

```
! _____
model Pmr,Pmi = 'curre_con VSC-1'(id_ref,ir,ii,cosref,sinref,iq_ref;xid,x1,xiq,x4;Tm,Kr,Tr,Ki,Ti,Min Pmd,Min Pmq,Max Pmd,Max Pmq;a1
id,iq = '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models\current_con_VSC-1.BlkDe
ud = '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models\current_con_VSC-1.BlkDef\U
Pmd = '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models\current_con_VSC-1.BlkDef\
Pmr,Pmi = '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models\current_con_VSC-1.Blk
uq = '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models\current_con_VSC-1.BlkDef\U
Pmq = '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\Models\current_con_VSC-1.BlkDef\
did = id_ref-id
diq = iq_ref-iq
      inc(x1)=Pmd*Tr/Kr
inc(x4)=Pmq*Ti/Ki
inc(id_ref)=id
inc(iq_ref)=iq
inc(xid)=did
inc(xiq)=diq

inc(Pmd)=Pmr*cosref+Pmi*sinref
inc(Pmq)=-Pmr*sinref+Pmi*cosref
```

DIgSI/info - Check initial conditions of '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\  
DIgSI/info - Variable may be used in output(), fault(), event()  
DIgSI/info - Variable may be used in output(), fault(), event()

```
set derivations to zero:
xid.=0 => 0=-a1*xid+did
x1.=0 => 0=dev1
xiq.=0 => 0=-a2*xiq+diq
x4.=0 => 0=dev
```

```
existing initial conditions:
inc(id_ref) =id
inc(iq_ref) =iq
inc(xid) =did
inc(x1) =Pmd*Tr/Kr
inc(xiq) =diq
inc(x4) =Pmq*Ti/Ki
inc(Pmd) =Pmr*cosref+Pmi*sinref
inc(Pmq) =-Pmr*sinref+Pmi*cosref
```

existing definitions/assignments:

```
Pmr =Pmd*cosref-Pmq*sinref  
Pmi =Pmd*sinref+Pmq*cosref  
a1 =1/Tm  
b1 =1/Tm  
b4 =Kr  
b5 =Kr/Tr  
dev1 =ud  
yunb1 =b5*x1+b4*ud  
a2 =1/Tm  
b2 =1/Tm
```

```
b0 =Ki  
b3 =Ki/Ti  
dev =uq  
yunb =b3*x4+b0*uq  
Pmd =lim()  
Pmq =lim()  
did =id_ref-id  
diq =iq_ref-iq  
id =ir*cosref+ii*sinref  
iq =-ir*sinref+ii*cosref  
ud =b1*xid  
uq =b2*xiq
```

```
DIgSI/info - Check '\\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfolder\curre_con VSC-1.BlkDef  
DIgSI/info - Variable may be used in output(), fault(), event()  
DIgSI/info - Variable may be used in output(), fault(), event()  
DIgSI/info - Block is ok.
```

### C.3 PQ- controller codes

DIgSI/info - Equations of '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Mo

```
! -----
model id_ref, iq_ref = 'PQ controller' (Pref, ur, ir, ui, ii, Qref; xiP, xiQ; KP, TiP, KQ, TiQ, id_ref_min, iq_re
id_ref = '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfold
iq_ref = '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.IntPrjfold
o1 = ir*ur
o11 = ii*ui
o12 = ir*ui
o13 = ii*ur
P = o11+o1
Q = -o13+o12
dP = -P+Pref
dQ = Q-Qref
inc(xiP)=id_ref*TiP/KP
inc(xiQ)=iq_ref*TiQ/KQ

inc(Pref)=P
inc(Qref)=Q
```

DIgSI/info - Check initial conditions of '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\  
DIgSI/info - Variable may be used in output(), fault(), event()  
DIgSI/info - Variable may be used in output(), fault(), event()

set derivations to zero:

```
xiP.=0 => 0=dev
xiQ.=0 => 0=dev1
```

existing initial conditions:

```
inc(Pref) =P
inc(Qref) =Q
inc(xiP) =id_ref*TiP/KP
inc(xiQ) =iq_ref*TiQ/KQ
```

existing definitions/assignments:

```
id_ref =lim()
iq_ref =lim()
b0 =KP
b1 =KP/TiP
dev =dP
yunb =b1*xiP+b0*dP
b2 =KQ
b3 =KQ/TiQ
dev1 =dQ
yunb1 =b3*xiQ+b2*dQ
P =o11+o1
Q =-o13+o12
dP =-P+Pref
dQ =Q-Qref
o1 =ir*ur
o11 =ii*ui
o12 =ir*ui
o13 =ii*ur
```

DIgSI/info - Check '\Ahadu.IntUser\VSC final(9).IntPrj\Library.IntPrjfolder\User Defined Models.In  
DIgSI/info - Variable may be used in output(), fault(), event()  
DIgSI/info - Variable may be used in output(), fault(), event()  
DIgSI/info - Block is ok.

## Appendix D: Matlab code for step response plot of the designed current controller and DC voltage controller

```
% Programmer: Ahadu
% Date : March 14, 2011
% Objective : Calculating Transient

%response parameters of the %designed
current controller

Ti=0.063694; % Integral time constant
Kp=64.52 ; % Proportional constant
R=0.20253 ; % Reactor resistance in ohm
Ta=0.0001 ; % Converter delay in sec

num=[Kp/(Ti*Ta*R)];
den=[1 1/Ta Kp/(Ti*Ta*R)];
G=tf(num,den);
step(G);
ylabel ('dq- currents amplitude');
xlabel ('time');
title ('step response of the inner current controller');
```



```

% Programmer:           Ahadu
% Date      :           March 14, 2011
% Objective   :           Calculating Transient step
                           %response parameters of the
                           %designed current controller

Ti=0.0018;              % Integral time constant
Teq=0.0002;            % equivalent time delay of %the
                       inner current control loop

Kp=0.109   ;           % Proportional constant
Vd= 45;                % AC System voltage in kV
Vdc=81.7;              % DC voltage in kV
C=53.933e-6;          % DC capacitor value in Farad

K=(3*Kp*Vd)/(2*Vdc)

num=[K*Ti K ];
den=[Ti*Teq*C Ti*C K*Ti K];

G=tf (num,den);

Step (G);

ylabel ('dc voltage amplitude');
xlabel ('time');

title ('step response of the DC controller');

```

## DECLARATION

I declare here that this thesis entitled “**Investigation of VSC-HVDC System for Dynamic Performance Improvement of EEPCO High Voltage Grid**” is the result of my own research work except as cited in the references. The thesis has not been accepted for any degree and is not concurrently a submitted candidature of any other degree.

Signature : .....

Name : Ahadu Hilawie

Place : Addis Ababa

Date : June 2011

This is to certify that the above declaration made by the candidate is correct to the best of my knowledge.

Signature : .....

Name : Dr.-Ing Getachew Biru

Place : Addis Ababa

Date : June 2011