



Addis Ababa University

Addis Ababa Institute of Technology

School of Electrical and Computer Engineering

Configurable Analog Circuit Synthesis and Implementation kit: PCB based Approach

A thesis submitted to School of Electrical and Computer Engineering as partial fulfillment

of

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By: Abisa Girma

Advisor: Dr. Getachew Alemu

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DECLARATION

I, Abisa Girma, declare that this thesis is my original work. The findings presented in this paper are not found in any other previous research works.

Abisa Girma

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Abstract

The implementation of newly designed analog circuits in most cases is a merger of known analog circuit blocks. The testing of these analog circuits have challenges like schematic to prototype part discrepancy, being cumbersome, fragility and component value variation. Field Programmable Analog Array (FPAA), could be considered analog counterparts FPGA, have been used for the design and development analog circuits. FPAAs combine CAD tool with rapid prototyping of analog circuits. FPAAs are monolithic programmable and generic analog circuit building tools.

In this paper a configurable PCB based analog circuit builder kit is to be designed and built as a possible rugged alternative to FPAAs. The need for this alternative is put forward to utilize the advantages of FPAAs in a more rugged and accessible analog circuit building. This kit contains real analog circuit components with configurable interconnecting switches on a single board. The building and validation testing of such a kit is performed in this research. It can handle more power and larger components. It contains on board power supplies and component banks. This kit could be instrumental in the education/training of analog circuit design both in academia and industry.

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Acronyms

PCB-Printed Circuit Board

FPAA- Field Programmable Analog Array

CAB-configurable Analog Block

FPGA- Field Programmable Gate Array

SPICE-Simulation Program with Integrated Circuit Emphasis

ICs- Integrated Circuits

QFN- Quad Flat pack No lead

EPAD- Electronically Programmable Analog Devices

LDO -Low Drop Out regulator

ACPA-analog cross point array

CACB- configurable circuit builder

Chapter 1

1.1. Background

Analog circuits are still in demand despite digital circuit domination. “The world, as we all know, is analog” . Almost every measurable physical quantity can be represented in an analogues of time varying electrical or other type of signal.

The information in measured physical quantities is mapped to electrical signal physical quantities like voltage, current frequency, phase and others. The analogues representation followed manipulation, adjustments and changing of physical quantities in terms of electrical signal quantities involves analog circuits.

Analog circuit conception, design and development requires a formidable know how and skillset. The design and development requires more experiments using real components. There are many aspects of analog circuit design endeavor that simple simulation could not address. Therefore, experimenting is critical for analog circuit design. Analog circuit have been built and tested using various implementation techniques. Circuit ball construction, perforated soldered board building, solder less bread boarding prototyping and PCB implementation are some of the well-known and used circuit building techniques.

The configurable circuit building realm is more advanced and commercialized in digital circuit design than analog circuit. FPGA, PLD, CPLDs and other reprogrammable and configurable digital circuit building platforms have been and are common. Analog Configurable platforms FPAAs and EPADs could be analog counter parts of FPGAs and PLDs. FPAAs are made of configuration memory units, configurable analog blocks (CAB) and a network. FPAAs are mainly used in the design of analog and mixed signal integrated circuit designs.

PCB based configurable analog circuit builder could be viable alternative for the study or design of analog circuits. Generic switches, multiplexors and cross point array ICs could be used to realize a configurable network and component banks. Assortments of real circuit component could be used to make the component banks.

1.2. Over View of Current Technology

1.2.1. Analog circuits

The world is an analog place. The realm of analog signal processing lets electronic circuits to work with the physical world. Analog circuit building blocks play important and big roles in electrical and electronics engineering. The most common analog circuit blocks in resistor networks, filters, oscillators, amplifiers, comparators phase locked loops, current mirrors, voltage references and analog and digital converters, voltage regulators and others. Their usage is ongoing and they will be in demand in the future [2].

The fundamental of analog circuit design, synthesis, analysis and building is being taught and trained. The analog circuit realm is an intricate interconnection of engineering and science and vocational disciplines. Electrical engineering circuit related disciplines like analog filters, oscillators, power electronics, instrumentation and others interact with device fabrication and science. The analog circuit design engineering, device physics and device fabrication disciplines are embodied by the vocations of thick film circuit building ,PCB(printed circuit boards) design fabrication ,PCBA(PCB assembly)

The construction of any circuit is a gathering of circuit component pins to specific number of nodes. Labeled circuits are build using certain number of nodes. Components are placed between nodes. Nodes use in analysis to study voltage and current characteristics. Measurement of parameters is done on or with nodes. Components pins that are connected to a node are equipotential. The effort of building any circuit involves interconnection of circuit component pins to nodes. The interconnection of nodes can also be achieved using switches, multiplexers and switch arrays. Cross bar networks are common networking methods that dates back to the day of development of telephone switching systems. Advancement of switch arrays and cross point arrays allows to make a configurable matrix like interconnection network according to[2]

1.2.2. Field Programmable Gate Arrays

The FPAA is a monolithic amalgamation of different of analog building blocks. There are also configurable networks used for conveying signals between analog building blocks. The presence of memory elements allowed users to achieve function and structure of analog circuit build according to [1].

FPAA is a monolithic collection analog building blocks with configurable interconnecting a network and memory units [3].

Configurable Analog Blocks (CABs)

[1]Configurable Analog Blocks (CABs) are the basic units of FPAA. They are interconnected using and a routing network. They also directly connected with configuration memory .the configuration memory units in turn are routed to be connected with CAD interface. These elements are made of operational amplifiers switched capacitors components

1.2.3. Printed Circuit Boards

Printed circuit board are circuit implementation using a thin metal lamination routes on insulation composite material. The PCB is extensively being used for circuit building throughout since and technology. PCBs are very diverse and rugged form of circuit building up date. The technology has been exploited commercially in extensive manner with in the last 60 years according to[5] . At the beginning of 19th century different approaches were taken to a printable circuit interconnection. Silver, graphite and other conductive material were deposited on cloth, composites and other materials to form circuits. The first idea of using copper coated clad and selective etching proposed by Dr. Paul Eisler. This gave way to rapid mass manufacturing method of PCB. The main principle of fabrication behind PCBs to this day is selective etching of copper coated clad [5].

PCB is produced in series of masking, drilling and etching processes. The starting material is the metal coated clad material. The clad material could be produced predominantly from copper. The copper is deposited on to a non-conductive sheet using forced plating or electrolytic deposition. The non-conductive clad part is produced from range of material type. That could range from cotton reinforced composite board to woven fiber glass and epoxy. The copper clad is mostly bought as standard raw material for PCB fabrication. The metal deposited clads classified in terms of metal type, metal thickness, non-conductive sheet thickness and material type.

The production of PCB starts from preparation of fabrication file. The fabrication files are produced from PCB layout software packages. The most common way of producing PCB fabrication files is in terms of layers. The main type of fabrication file is named gerber files. This is a collection of simple images of PCB layers.

PCB is realized by successively etching using photo lithographic methods. The copper clad is drilled on CNC for through hole component mount, chassis mounting and via holes. Then copper coating on the PCB clad is etched after masking the routes with etch resistant film. The completed further goes to photolithographic masking for solder masking. Solder pads are then coated with immersion or hot air knife techniques with metals like silver, tin and gold.

1.2.4. Over view of configurable analog circuit builder (CACB)

The configurable analog circuit builder (CACB) designed is inspired by crossbar network formation for analog circuit building [1]. The network formed is a cross bar interleaving with analog switch at each cross point. The cross point switches are digitally addressable.

The CACB architecture is selected in consideration of main network, component banks, and digital control signal, on board processor and computer interface. A computer interface circuit is connected to main on board processor. The on board processor is connected to analog cross point array (ACPA) ICs and analog multiplexors via port expansion ICs. The power supply voltage regular circuits provide to all digital and analog ICs on board.

The CACB is implemented on Printed Circuit Board. The cross bar network takes center stage while component banks surround its peripherals. Analog switch and multiplexor control digital signals and signal port expansion circuits are placed on outer peripherals of the CACB board. In consideration of placement of components, signal type and route complexity four layer PCB is selected. The design of PCB follows the convention of first zoning of board then placements components and eventually routing of interconnection. There are also other detail tasks like formation of component footprint, design rule checking, and sourcing and files generation.

Analog circuit built on a schematic capture software is saved to generate SPICE based net listing. The generated net listing is processed to a configuration data using custom computer side program designed for this research. The configuration data is passed to CACB's on board processor via serial port. The on board processor send switching data to cross point arrays and component bank analog multiplexors.

The CACB board is built stage by stage and tested for functionality. The performance of the CACB is conducted to support the main argument of this thesis. This CACB could be a viable alternative for analog circuit building using bread boarding, ball circuiting or FPAA implementation.

CACB could be faster to build, versatile, cheaper, accurate and better power handler. This is verified using performance testing using a simple nominal resistive circuit network.

1.3. Literature Review

Analog Integrated Circuit Design and Testing Using the Field Programmable Analog Array Technology [7]

This paper presents a design and testing of an analog circuit using FPPAs. It introduces to FPAA based on switched capacitor then presents a specific FPAA namely AN221E04. An analog phase comparison circuit design, implementation and testing was performed using AN221E04. Finally the results were compared with simulation.

The need for FPAAs

Integrated circuits are becoming ever complicate and dense. The design processes for these ICs is getting tedious and more time taking. Therefore analog, digital and mixed design are approached using deferent abstraction levels. Programmable circuits added more capability towards the design of even more complex circuits. The design of Integrated circuit outside manufacturing was made possible due programmable circuits.

PLDs contributed to custom design digital ICs which eventually led to FPGAs. In comparison the FPAAs lag behind both in commercialization and utilization. As example the Anadigm FPAA became available commercially.

The FPAA explanation in this reference paper is based on a CAB implemented using switched capacitor. Switch capacitor equivalent resistors are used around an Opamp to make a single CAB. The sampling frequency ($f=1/T$) determines the equivalent resistance value of switched capacitor.

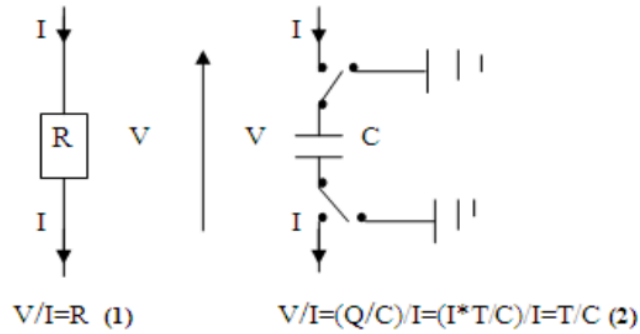


Figure 1: Switched Capacitor used as resistor [7]

Intricate and safety critical ICs undergo various types tests to insure reliability. In addition to that self-diagnostics and redundant circuits are included to add “limp home” capabilities. One such circuit is built and tested using Anadigm FPAA in this paper.

Functional Switching Matrix for Automatic Analog Circuit Synthesis [8]

This article discusses about the development process automated or semi-automated analog circuit synthesis. The approach taken is first to formulate circuits component, number of pins and switch matrices and suggest circuit topology that reduces number attempts to make a circuit. Analog circuit realization using switch matrix is chosen. The number of components and the number for their pins can form a matrix of all possible connection. This matrix is mapped to a space division of non blocking switch matrix array. Further the utilization of unused rows is also suggested.

1.4. Statements of Problem

The common analog circuit building techniques like bread boarding, circuit ball building, and PCB prototyping have been used for long time. These methods have short comings like

- Cumbersomeness: building systems of circuits could result in huge amount of wire work and instruments
- Fragility of constriction: circuits could be easily malfunction due to loose connections and movement of parts
- Debugging difficulty: tracing and rectifying anomalies in circuits could be difficult
- Need to have all parts at place- availability of various parts is requirement for continuous development and design work.

The above shortcomings could result in longer design time, limited design scope and costly design. This in turn limits access to analog circuit design, building and test capabilities.

Configurable analog building techniques could overcome the above mentioned shortcomings. FPAA could be a good alternative for analog designs but they also come with their own shortcomings. They are

- hard to acquire,
- mostly made to operate in low powers
- made by different companies with different CAD tools(computer side software)

This thesis work tries to find and demonstrate an alternative analog circuit building kits that have the configuration capabilities of FPAAs and ruggedness of mainstream analog building techniques.

1.5. General Objective

The objective of this thesis is explore a viable alternative configurable analog circuit builder using PCB based implementation. It involves conceptualizing, designing, building and testing of an analog circuit builder.

1.6. Specific Objective

The specific objectives of this thesis are summarized below

1. Explore elements of a configurable circuit builder: to study configurable networks, analog circuits and analog switching elements and state of the art configurable analog circuit building methods.
2. Conceptualize analog circuit builder: to build a concept feasible CACB architecture considering scope, viability and availability of parts.
3. Design elements of CACB: to develop CACB elements like PC side program, Circuit board and embedded program.
4. To build a prototype for CACB: to build working PCBA with functional testing
5. Test: to check the functionality and efficacy of CACB and analog circuits using soldered perforated board

1.7. Relevance of this thesis work

This thesis could be useful in its quest to find a rapid configurable analog circuit building alternative using PCB as platform. A PCB based kit that can build a variety of circuits with digital interface could be useful in electronics laboratories in both industry and academia. A more rugged

and practical circuit builder kits could be developed using this study as a starting point. The hardware implementation in this thesis could also be used in analog signal (i.e. video, sensor signal, waveforms) routing, multiplexing and mixing.

1.8. Methodology

- The problem related analog circuit building was listed out. Then literature is reviewed to study and understand state of the art configurable circuit builders.
- A conceptual for an alternative configurable analog circuit builder is drawn
- The detailed selection and implementation hardware and software design was done
- A prototype for CACB was tested for functionality and efficacy

1.9. Outline of thesis

Thesis is organized in seven chapters. The first chapter presents the problem statement, objective and relevance of this work. In the second chapter an over view to analog circuit building, FPAAs, PCBs is presented. In addition works related FPAA based configurable circuits and cross bar networks are review. The third chapter presents concept for architecture and construction of CACB kit. The fourth chapter deals assumptions and step by step design of CACB kit. Chapter 5 and 6 deals with efficacy and/or functionality test and test results respectively. Chapter 7 is present recommendation and conclusions

Chapter 2: Configurable Analog Circuit Builder Conception and System Description

2.1 Field Programmable Gate Arrays

The FPAA is a monolithic amalgamation of different of analog building blocks. There are also configurable networks used for conveying signals between analog building blocks. The presence of memory elements allowed users to achieve function and structure of analog circuit build according to [1].

FPAA is a monolithic collection analog building blocks with configurable interconnecting a network and memory units [3].

Configurable Analog Blocks(CABs)

[1]Configurable Analog Blocks (CABs) are the basic units of FPAA. They are interconnected using and a routing network. They also directly connected with configuration memory .the configuration memory units in turn are routed to be connected with CAD interface. These elements are made of operational amplifiers switched capacitors components

2.3 General Concept development

A configurable circuit building tool regardless of digital, analog or mixed would contain a component space, network space and a CAD tool (PC side software)(Figure 2). These three parts work in tandem to achieve rapid, less error prone and configurable circuit building and testing. The CACB conception and design involves search and choice of suitable part for the three sections.

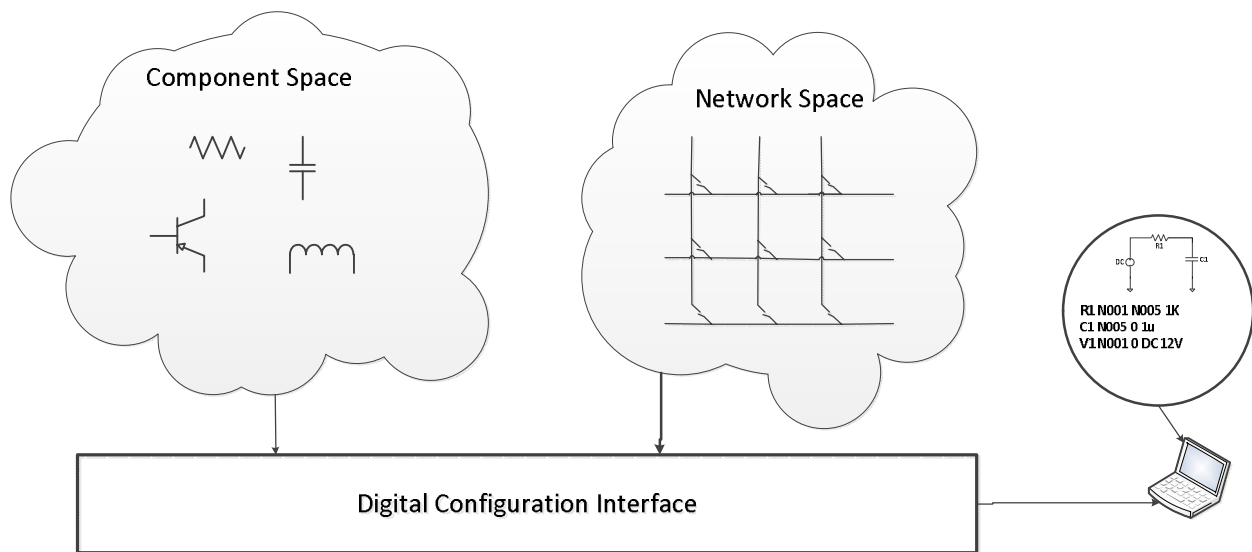


Figure 2 : CACB initial Concept diagram

2.1.1 Component Space

The component space refers to circuit component assortment, mapping and selection. The component choice for the CACB are

- a. Switched or simulated components: like in FPAAs resistor and other components' behavior could be achieved using switched capacitor methods. This involves formulation of circuits with switches, capacitors and pulse generators.
- b. Real components: using combination or multiplexing of component assortment

Inconsideration of simplicity of design and the ruggedness that real components bring to the implementation of CACB they are selected for this study.

2.1.2 Network Space

The network space refers to the interconnecting element of CACB. This network needed to form the nodes of CACB kit. It should be configurable (i.e. switchable) via digital control. This network could perform in space division or time division.

- a. Time division: refers to time slotted switching different of component pins. Time division involves switching of multiplexors and switches.
- b. Space division: refers to the interconnection different component pins by means of switch arrays and cross points using spatial channels.

The space division is chosen for implementation of CACB. It is simpler to implement and better mimics main stream analog circuit building techniques.

2.1.3 Digital Configuration interface

The digital interface stands between PC side software tool and network-component space. This part has function of

- i. Receiving and storing of encoded mapping for components and network
- ii. Addressing of network for configuration using analog cross point arrays
- iii. Addressing of components using analog multiplexors

The digital configuration interface would contain microcontrollers, serial to parallel converters and computer interface ICs.

2.1.4 PC Side configuration tool

In the realm of configurable circuit building the source of circuit interconnection (i.e. net list) is a schematics capture tool and simulation CAD tool. The most common and simplest form of net listing for circuit is achieved by using SPICE listing. A SPICE implemented listing can be easily interpreted to actual circuit.

The PC side configuration tool, in CACB context, is custom software that can interpret SPICE listing and process it to make configuration data. The configuration data is then sent to CACB board via serial communication.

2.4 Implementation Conception

The circuit building process is based on the fact that any circuit can be constructed by connecting different components to a designated nodes(Figure 3). Different kinds of analog circuits could be achieved by Connecting, disconnecting, adding and shifting of node connections.

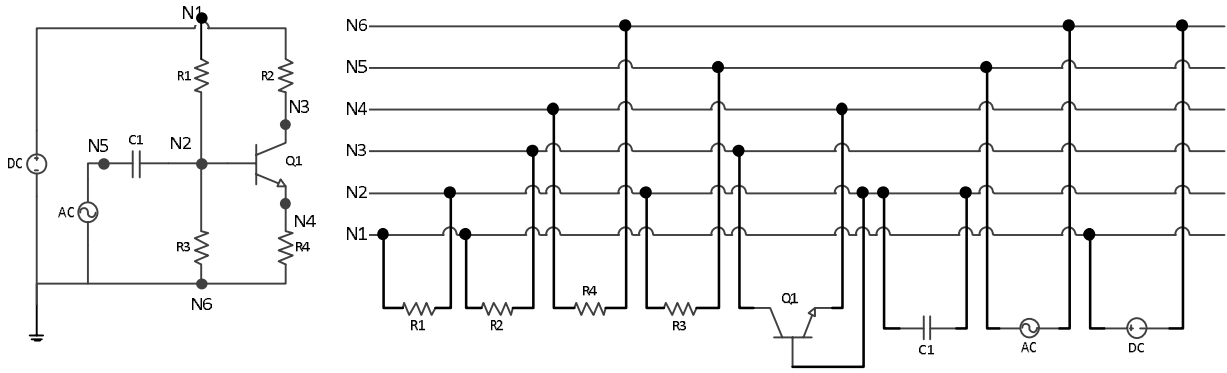


Figure 3: Simple voltage transistor amplifier circuit plotted in two topologies

a) basic schematics b) parallel node connection schematics

Switches could be used to realize node connections according to [3]. The selection of analog switch array is done according to the voltage swing levels that they allow, maximum switch resistance, and frequency band width, switch array count and digital control. The switch resistance and voltage swing allowance are have a considerable tread off while selecting a commercially available analog cross point switch array.

The components to connect to the node are selected from bank of possible components. These banks of components uses analog multiplexors. Analog multiplexors used have the lowest resistance with the least trade off with voltage swing.

A configurable Analog circuit builder that is intended to be realized in research contains two main parts(Figure 4). The part are the PC side (1) software and main circuit board (2). The PC side program reads analog circuit SPICE listing file and extracts circuit building parameters. The main circuit board implements the particular analog circuit using on board components and analog switches.

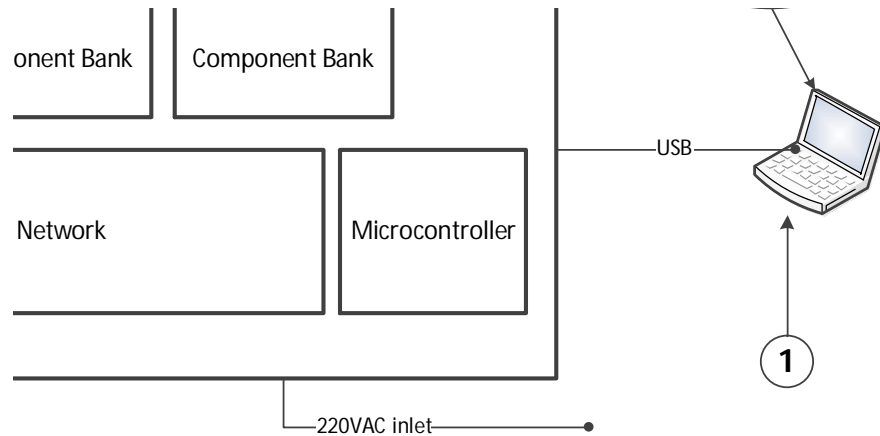
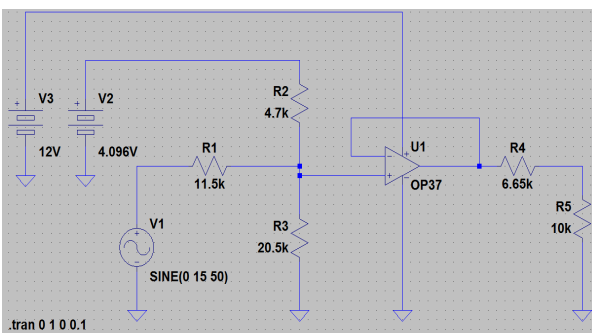


Figure 4: Configurable Analog circuit builder System

2.2.1 PC side program

This program is responsible for the extraction of circuit building parameters from SPICE listing file. Circuit building parameters include number of circuit nodes, kind of component, count of component, value of component, node connection of component. A typical SPICE listing would contain rows of data delimited by space (Figure 5).



```
V1 N004 0 SINE(0 15 50)
R1 N005 N004 11.5k
R2 N005 N002 4.7k
R3 0 N005 20.5k
V2 N002 0 4.096V
XU1 N005 N003 N001 0 N003 LT1037
V3 N001 0 12V
R4 N006 N003 6.65k
R5 0 N006 10k
.tran 0 1 0 0.1
.lib LTC.lib
.backanno
.end
```

Figure 5 PC side program description

This program is also responsible for data packaging and sending to circuit board. Some data processing is also be done in order facilitate circuit building. Data processing includes address mapping, component lookup and Analog cross Point array (ACPA) and Analog Multiplexor switching map.

2.2.2 Circuit board

This circuit board (Figure 6) is responsible for the actual building different analog circuit desired by the user. The desired analog circuit building parameters (i.e. processed parameters) are received from computer side via serial communication. The on board microprocessor would translate the parameters to digital switching pattern. These patterns are passed in digital I/O (input output) expander chips. The digital I/O expanders rearrange analog circuit interconnections by directly addressing digital interfaces of ACPA and analog multiplexers.

The circuit nodes are availed for measurement purposes on a on the left edge of the board.

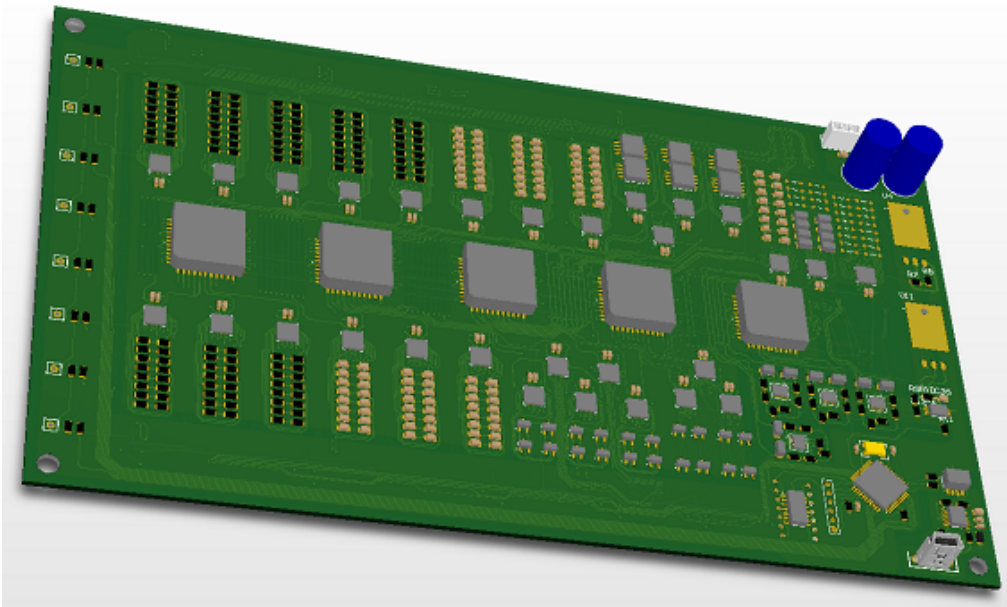


Figure 6 configurable Analog circuit builder circuit board

Chapter 3: Analog Circuit Builder Design Process

3.1 configurable Analog circuit builder initial assumptions and design approach

3.1.1 Analog circuit builder System Architecture

The system architecture refers to how a configurable analog circuit could be achieved on PCB. The decision to land on a single working system architecture some questions were raised.

What are kinds of analog circuit components are to be used?

The analog circuit builder system may contain some Passive components, transistors, diodes, operational amplifiers and others. There could also be opening for insertion of unique components like analog mixed signal ICs, sensors and other components.

What are the limits of analog circuit builder board?

The others important issue is up to how much voltage level and up to how much frequency bandwidth shall be implemented. In this implementation voltage levels assumed to include from -7.5V to 7.5V for dual supply operations and 0V to 15V for single supply operations. The frequency band width could be limited up to 500 KHz.

The analog circuit builder board is composed of analog switching elements and component banks. Analog switching elements include analog cross point arrays and analog multiplexers. The composition of analog circuits that are desired to be made using this circuit builder detected the analog switches kind and capability.

How can any component pin be connected to any kind of node?

Simple analog circuits doesn't involve too much node count. Eight nodes could cover a significant number and kinds of analog circuit builds. Therefore the connecting varies pins of circuit components to eight or less number of node could be enough to test the basic argument of this paper.

Analog cross points array are used for PBX Systems, Instrumentation, analog and digital Multiplexers and Video Switching Networks. Analog cross point arrays are logical choice implement circuit builder. 8 by 16 analog cross point can connect 16 possible component pins. The increase number of component pins connected to the eight nodes more analog cross points arrays

are used by sharing the eight columns. Five analog cross point arrays are used to make in order to make the eighty components pins connection to nodes.

How many components and kinds of components could suffice to cover the implementation of a descent number and kinds of analog circuits?

The components kinds and counts to be used is determined case by case. Resistors are the most commonly used components. They are versatile and can come in different size and kinds of packages. The most common and familiar series of resistor value is the E-series. The E-series follow discrete values of resistor value spaced exponentially. The most familiar series, E-12 series, contains 12 resistor where the values approximately correspond to exponent of 10 to 0.083. The exponent value is multiplied by integral resistor place value. The first value of E12 series follows a pattern of 1,1.2,1.5,1.8,2.2,2.7 while 10 to the power of 0.083 with integral values follows 1,1.16,1.4 . The E12 series with 7 tenth place multiplier would contains 84 resistors.

To use this resistor series with possible reputation of some common resistor values eight resistor banks can suffice for this analog circuit builder. There will be 8 resistors banks each containing 16 resistors.128 possible resistors are populated in this analog circuit builder board.

The capacitor values most commonly used are fewer than resistors. In this design there are 6 capacitor banks with 16 capacitor in each. The transistor and operational amplifier are fewer in type and in kind there for the on half of the 4to 1 analog multiplexor is used. On each transistor or Opamp bank 4 transistor/Opamp is placed.

3.2 Circuit board implementation

3.2.1 Computer interface

USB to UART communication port is used. The on board processor is connected to the UART side of interface while the USB is connected to computer side via mini-USB connector. This sub-circuit is implemented using a FTDI's FT230XS-R USB to UART converter (U19)(Figure 7). There is a USB isolation for TX and RX signals. This is done in order avoid shock hazard and unwanted common mode voltage stress. The isolation is achieved using an opto-coupler (ILD207T, U18). There is a TVS diode (D1) placed between FT230XSR USB to UART IC (U19) and USB connector (P3) for ESD protection.

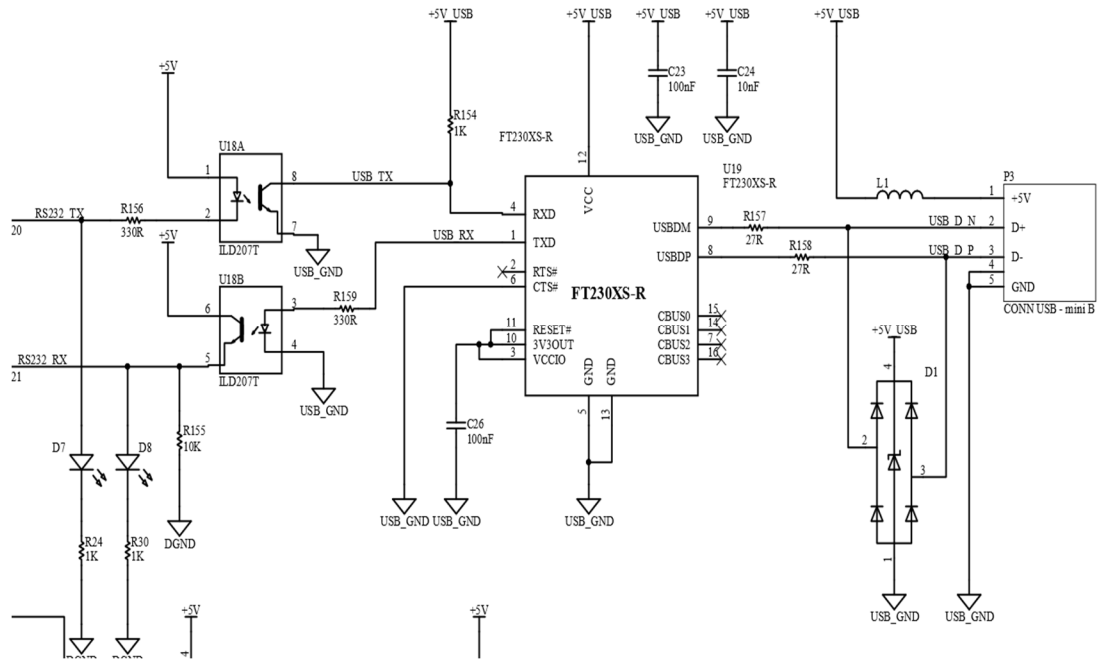


Figure 7: section schematics of computer interface sub-circuit

3.2.2 Processor

The analog circuit builder has a processor (PIC16F877, U30) (Figure 8) that receives component interconnection data and sends to digital selector circuit for analog switch array interconnection. The processor is connected to the digital selectors (i.e. Digital Port expander ICs) via SPI interface. It is also controls indicator LED light to show which of eight analog nodes are loaded.

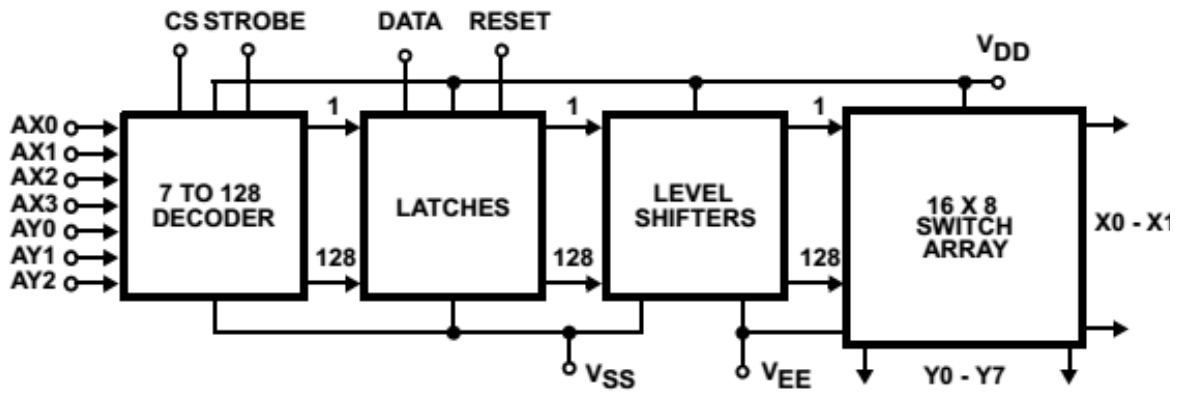


Figure 9: Single analog cross point array IC [taken from CD22M3494 datasheet]

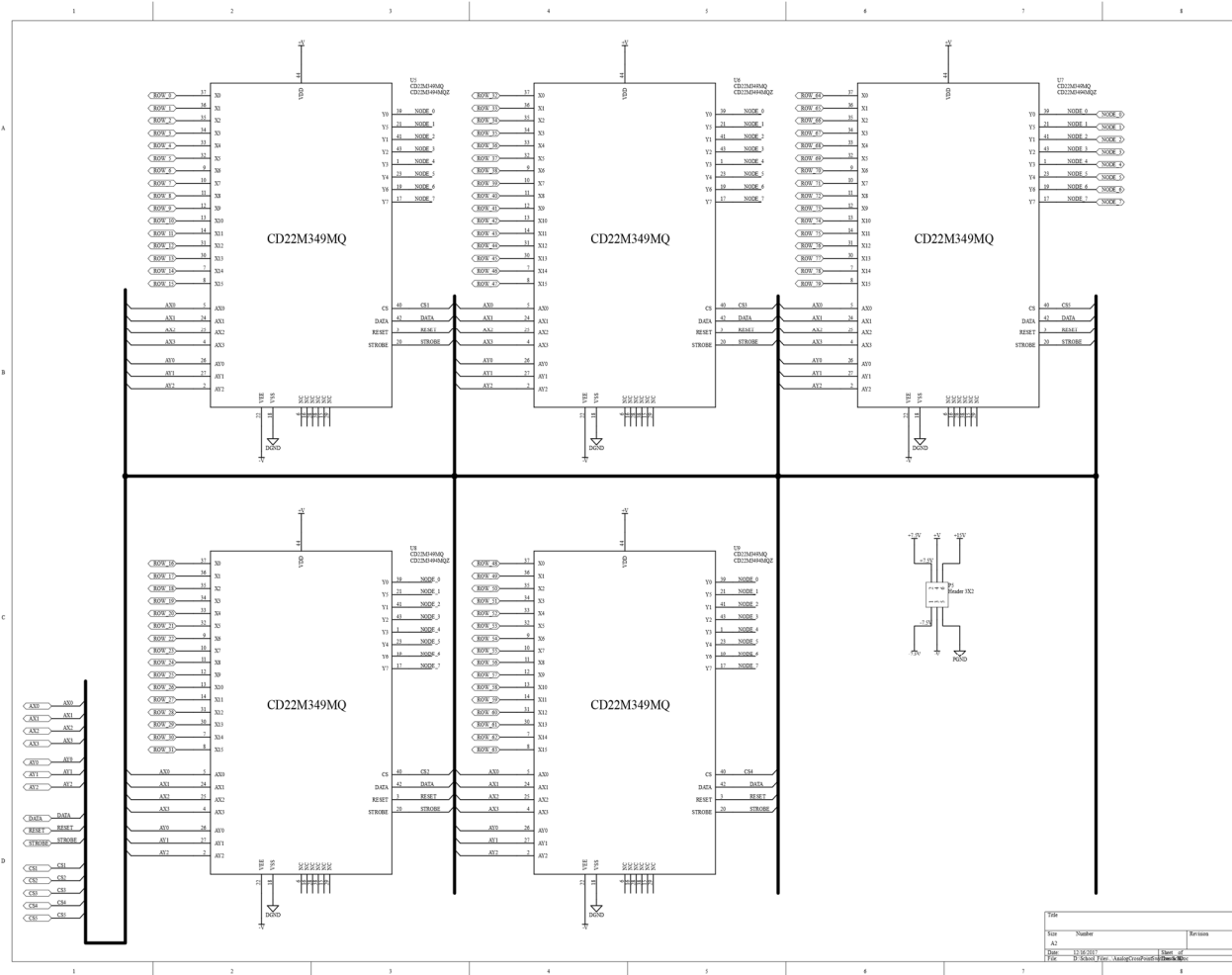


Figure 10 : Section schematics of Analog Switching network using five analog cross point array ICs (CD22m3494)

3.2.4 Component Banks

There are 12 resistors that can be availed at a time for the analog cross arrays. Each resistor is selected out of possible 16 resistors (4 by 4 array) using two 4to1 analog multiplexers(Figure 11). These multiplexers are have minimal resistance (nearly 1ohm) and are independently controlled.

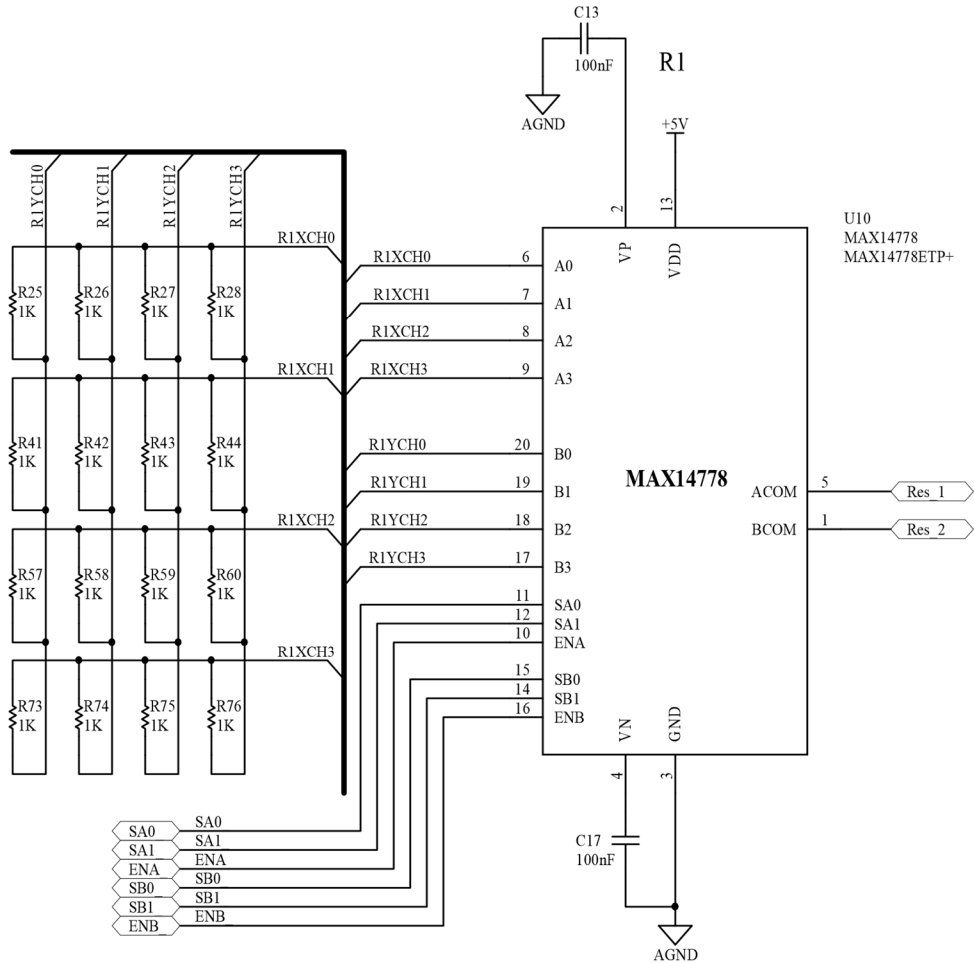


Figure 11: Resistor bank unit made of a dual 4 to1 analog multiplexor (MAX14778) and 16 resistors

There are 6 capacitors that can be availed at a time for the analog cross arrays. Each capacitor is selected out of 16 resistors (4 by 4 array) using two 4to1 analog multiplexers.

There are 3 transistor (Figure 12 a) s and 3 Opamp (Figure 12 b) that can be availed at a time for the analog cross arrays. Each Opamp or transistors are selected out of 4 transistors or Opamp (2 by 2 array) using three 4to1 analog multiplexers for each set.

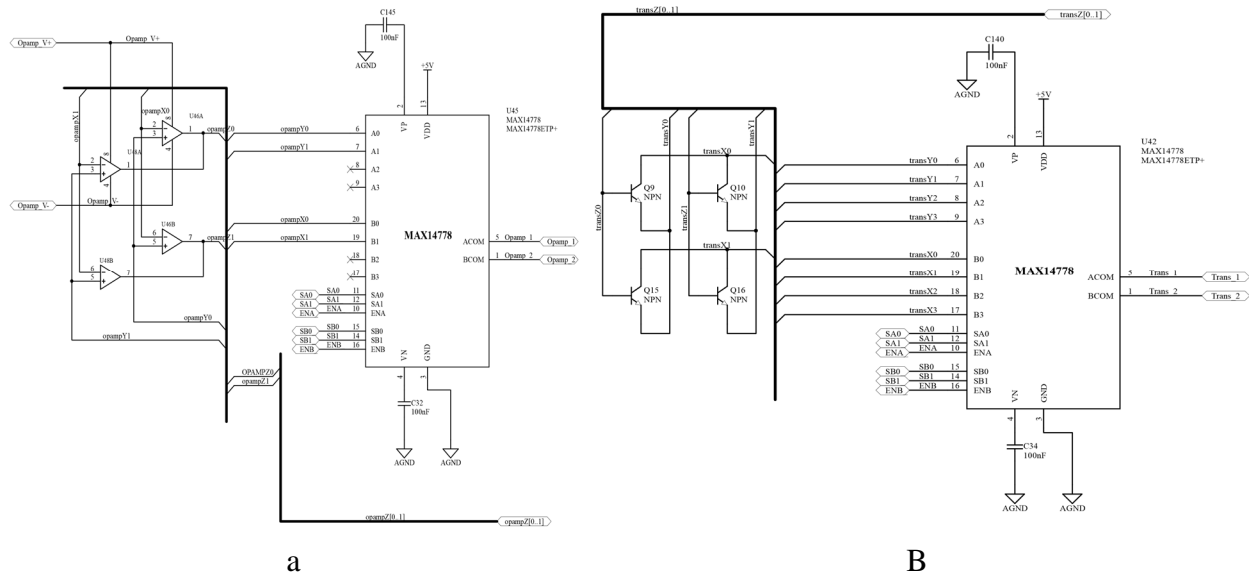


Figure 12: Operational amplifier and transistor component bank made from

a) 4 Opamp and MAX14778 b) 4 transistors and MAX14778

There are three miscellaneous components banks for two leg components that are individually selected out of 16 component through dual 4 to 1 analog multiplexors. There are three, 3 legged miscellaneous components, availed each selected out of 4 multiplexed components using 4 to 1 analog multiplexors.

3.2.5 Digital Selection sub-circuit

This configurable analog circuit builder used two kinds of analog switches (i.e. the analog cross point array (CD22m3494) and 4 to 1 analog multiplexor (MAX14778)). The analog cross point array contains data reset, strobe and chip select digital signal input pins. The dual 4 to 1 analog multiplexer contains four select pins and two enable pins. There are five analog cross point array ICs and twelve dual 4 to 1 analog multiplexors. This requires numerous digital signal lines coming from the on board processor. This is achieved using digital port expander ICs (MCP23S17) (Figure 13). These ICs receive data via 4 wire SPI and change it to sixteen bit parallel data lines. These data lines are connected to the both cross point arrays ICs and analog multiplexors. Each port expander have a hardware a three bit address pins.

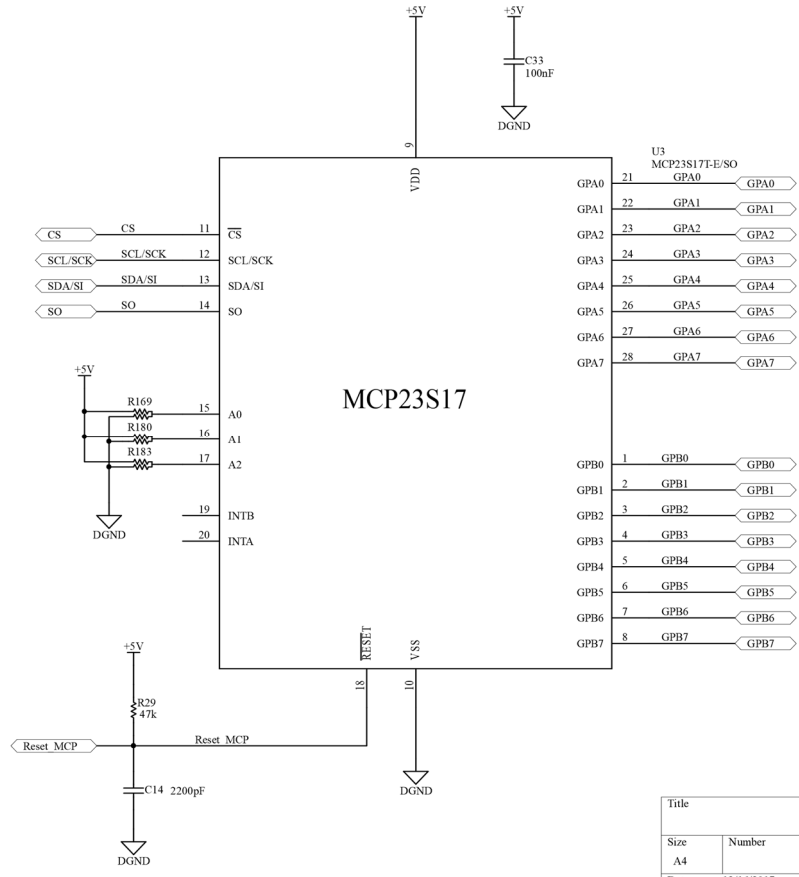
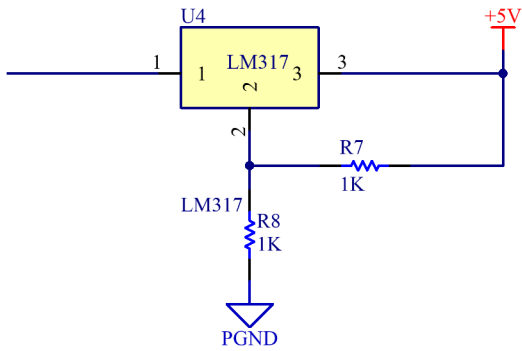


Figure 13: Part of Digital selector sub-circuit using port expander (MCP23S17)

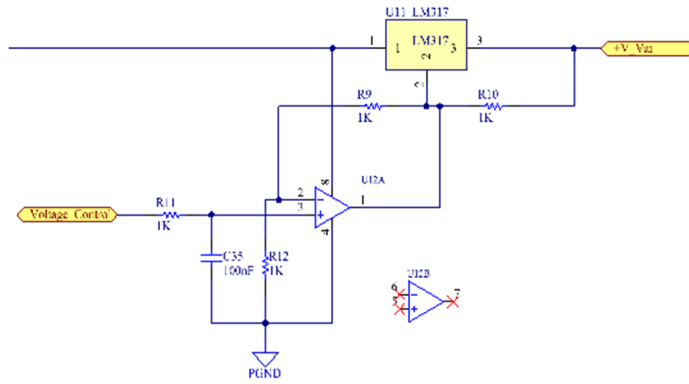
3.2.6 Power Supply

There are two power supply sections for this implementation of analog circuit builder board. The main power supply for the analog circuit builder is built externally. There is +/-15V split power supply using a brick switching power supply. The input voltage for this power supply is 220VAc mains supply. Power surge protection circuit components are added for better reliability. The power output level is limited to 10 Watts total.

There are few on board voltage regulator circuits for various fixed and variable voltage needs. Adjustable voltage regulator LM317(Figure 14 a) is used to supply five volt for logic level Vcc needs. The LM317 is also used to generate single supply variable voltage supply with the processor (Figure 14 b). The processor provides a varying PWM signal to set a variable voltage.



a



B

Figure 14: LM317 linear regulator used for a) 5V Vcc supply and b) variable voltage supply.

The need for variable and fixed voltage split power supply is addressed using LDOs (LT3032). This LDO is adjustable using external resistors (Figure 15). The $\pm 3.3V$, $\pm 5V$, $\pm 7.5V$ and variable voltage output are provided to the analog cross point switch array.

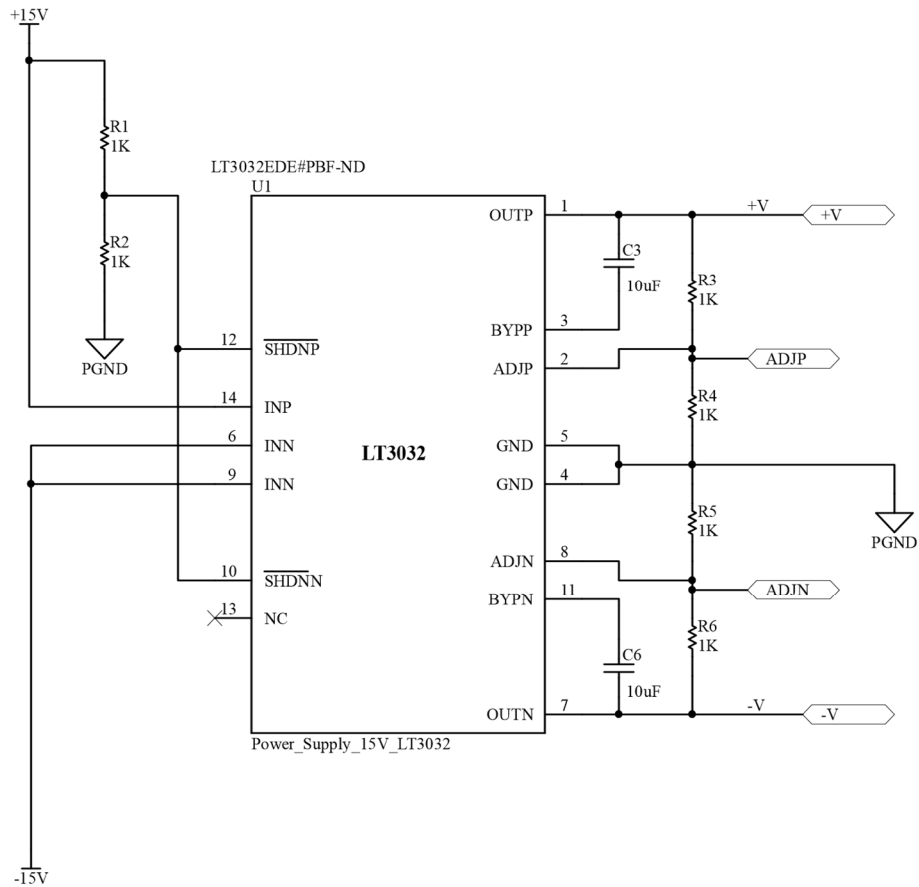


Figure 15: LDO (LT3032) used to supply split power supply

3.4 PCB implementation

3.3.1 PCB parameter selection

The PCB layout of the analog circuit builder involve different initial parameters choices. The size is determined to be 23cm by 16 cm after several readjustments. There is made form 4 layers of copper each with 1 ounce per foot square thickness. The surface finish is determined to be HASL or tin immersion for better solder wettability.

3.3.2 PCB design

The PCB design is started by making foot prints for each circuit element on the board. In this circuit board the majority of the components are surface mount type. Passive components and diodes foot printed are designed according to data sheet or inherited from standard footprint library. Foot print for IC packages like the analog cross point array (cd package) and 4 to 1 analog

multiplexer (MAX package QFN 32) are designed according to datasheet dimension values and footprint recommendations.

The next process of making circuit board is zoning. The board are is divided and allocated for different sub circuits (Figure 16). The zoning is dictated by the user convenience, ease of routing and electromagnetic interface (i.e. cross talk, coupling) between sub-circuits. The zoning is first performed on block diagram level and then translated to PCB layout software.

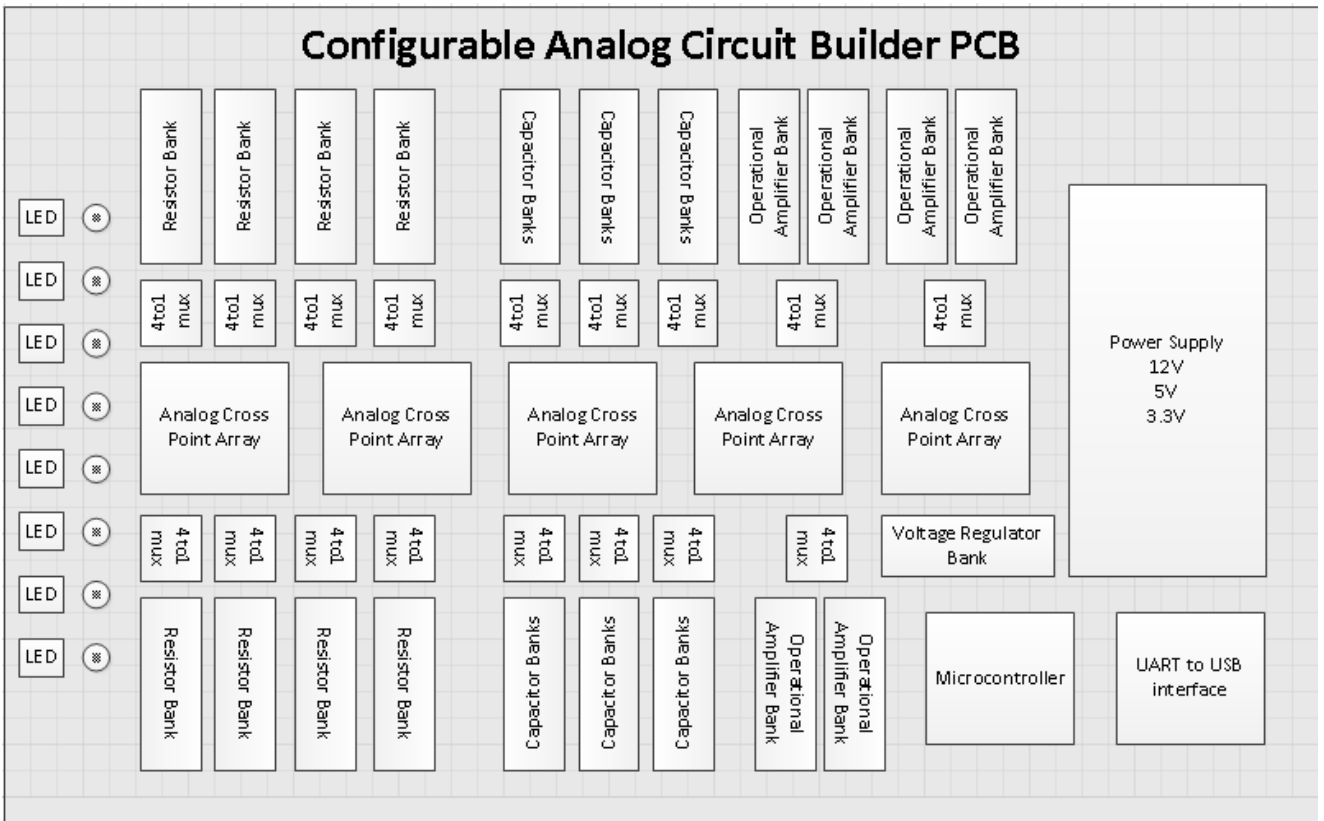


Figure 16: PCB zoning diagram

After deciding on the zoning of sub-circuits the placement of individual components is performed. Components banks are done repetitive therefore, the placement of each components is copied. Trial routing runs are performed in order decide on the placement of major components. The major components like the analog cross point array ICs and pins are routed to conform the placement.

The routing layers are reserved according signal type and placement. The first (in red) and the third layer (i.e. in sky blue) are used for analog signal routing. The second layer (i.e. brown) is used for ground and shielding and few signal lines routing. The fourth layer (i.e. blue) is used for digital signal routing. (Figure 17)

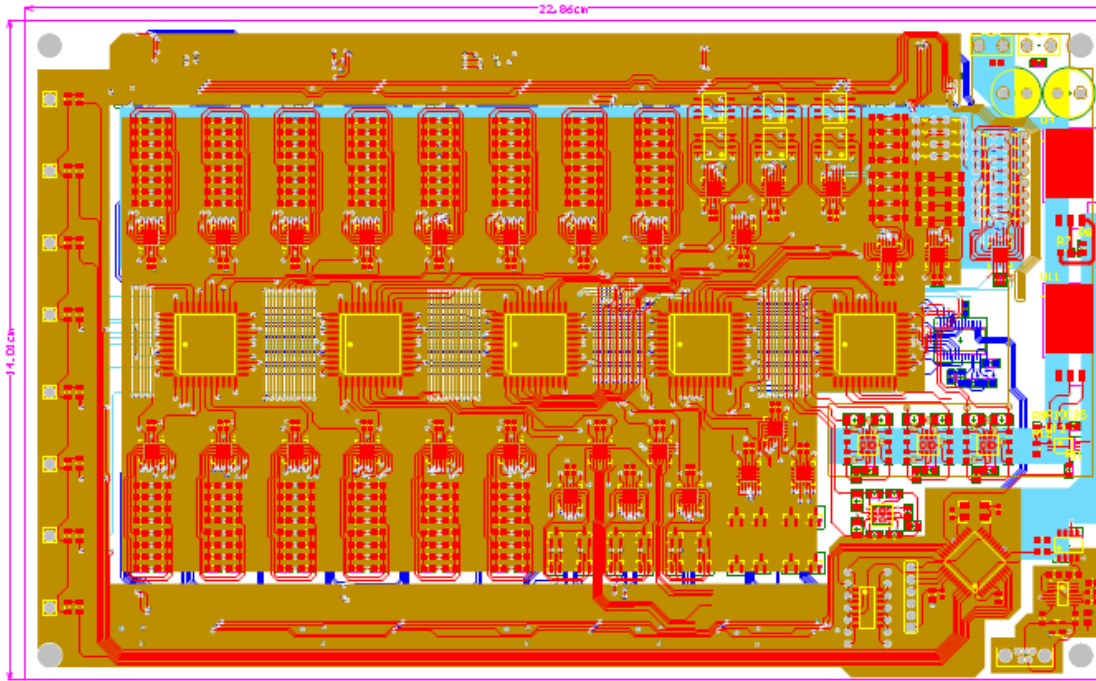

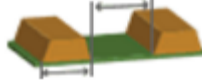





Figure 17: PCB layout for Analog Circuit Builder

3.3.3 PCB fabrication Specification

Once the routing of CACB is finished a fabrication specification (Table 1) and fabrication files are prepared. The fabricating is files include Gerber files, Drill files. The fabrication specification include layer information, copper thickness, surface finish, layer thickness and others parameters.

Table 1: PCB ordering Specification

| Parameter | Value | unit | Description | Remark |
|---------------------|--------|--------|--|----------------------|
| Length : | 228.6 | mm | | |
| Width : | 140 | mm | | |
| Layers : | 4 | layers | | |
| Layer Stacking: | | | Look on Figure 1 | 10/36/10 FR4 spacing |
| Track width(min.) | 7 | mil |  | (milli-inch) |
| Track spacing(min.) | 4 | mil |  | |
| Hole size(min.) | 15 | mil |  | |
| Via | Tented | | | |
| Board Thickness : | 1.6 | mm |  | |
| Finished Copper : | 1 | Oz. |  | |
| Surface Finish : | HASL | | | |
| Solder Mask : | Green | | | |
| Silkscreen : | White | | | |
| Quantity : | 5 | pcs | | |

3.5 Computer side implementation and Conception

3.4.1 SPICE Circuit Listing

The analog circuit building using CACB starts by making schematics of the preferred circuit. There are numerous types of schematics capture software used around. Many schematics capture software packages use some form of SPICE or PSPICE listing. This listing would describe aspects line kind of component, designator of component, value of components, electrical value of sources, and designation of nodes. The LT-Spice schematics capture and simulation software page is used in this project. SPICE listing is generated in *.cir files format.

The SPICE listing analog circuit is read by computer side code and placed in a matrix form. The extraction is done by reading line by line basis. The kinds of components are code by numbers, the values are also place in magnitude and exponents cells of the extraction matrix.

3.4.2 Circuit Net List Processing

The SPICE listing analog circuit of a particular interest is read using a computer side program. Each line is identified for what kind of component is used. Once the component type is known the remaining parameters like net number and component value are stored in matrix form. The matrix listing of SPICE is fed to two separate programs. The first one is the analog component bank mapper and the second is ACPA IC network mapper.

The analog component bank mapper search the component value form lookup table. Once the component is located the component bank number and the location of the component with in the bank. The location of each component is changed to a encoded byte array to be sent to CACB processor.

The ACPA IC mapping code assigns one column(Y value) for each and decides on connection of component banks. A byte array is prepare for ACPA switch mapping in terms of state of switch(on or off). There are 128 switches in one ACPA IC. Which translates to 16 bytes.

The processor side firmware interprets the byte arrays in address value on both ACPA and 4to1 analog multiplexors

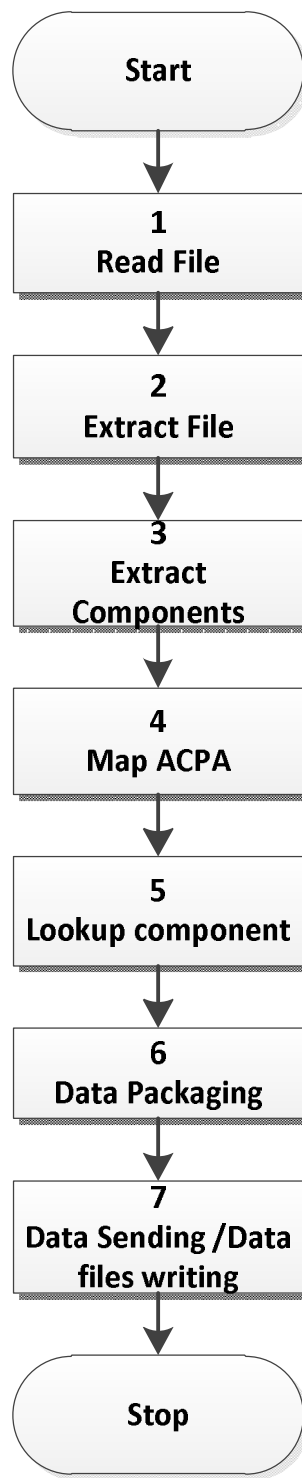


Figure 18: SPICE file extraction and processing flow

Chapter 4: Testing

4.1 Analog Circuit Builder Efficacy Testing Methodology

The basic argument this paper is a configurable PCB based analog circuit builder kit is to be designed and built as a possible rugged alternative to FPAA's or traditional analog circuit building and testing. Several Experiments are conducted to support the argument that this circuit builder could be a rugged alternative.

4.1.1 Basic functionality testing

The analog circuit builder is tested part by part. The power supply circuit was first assembled and tested. Then the processor and computer interface circuit is tested for basic digital tests.

4.1.2 Basic Digital Tests

A basic digital test for the processor include programmability test, input output test. Interface test. Programmability test include the writing of simple codes and program loading. Once the processor is tested for functionality, configuration of different processor interfaces are tested. The original processor choice PIC16F877A is replaced by Atmega328p for the sake of availability and ease of debugging. The debugger selected for this experiment avrdragon debugger and ISP board.

4.1.3 Programming Test

The Atmega328P is programmed to work on debugwire mode. Debug wire is Atmel corporation propriety debugging interface. The atmega328p is configured to work in debugwire mode for this experiment.

4.1.4 Computer Interface Test

The processor is interface to the computer via UART and to serial to parallel port expander (MCP) via SPI. The UART sequence is tested using a stage by stage echo back tests. This test is performed after populating UART to USB interface circuit. The Computer interface was checked by connecting the board via USB cable to a computer and check if a USART com-port is recognized.

4.1.5 Port Expander Test

The SPI interface of processor to the Port expanders is tested after SPI interface code is written. Output registers of the port expander are is tested for accessibility. The port expander is checked receives serial data via SPI interface and changes it to 16 bit parallel data.

The port expander that is connected to ACPA ICs use the 8bit data for X and Y address and the other 8 bit data used for Strobe, Data, chip select and Reset signals. The port expanders that are connected to dual 4to1 analog receive the switching pattern processor. The 16bit received is used to drive two analog multiplexors as they have six input signals each.

The analog cross point arrays (ACPA) are assembled and tested for communication with the processor. This ACPA IC is accessed via a port expander the analog switch interconnections are tested for interconnectivity and resistance value were recoded. The sixteen rows (x0-x15) can connected to any one of eight column values (y0-y7). This test shows that a network of components can be achieved node by node basis. The column wires (y0-y7) serve as the node of the analog circuit built. The row pins are connected to components banks. Five ACPA ICs are accessed using chip select pins.

The dual 4to1 analog multiplexors are tested for communication with port expander and analog performance. There are eight resistor banks. Each resistor bank contains two 4to1 Analog multiplexors and 16 resistors of different assortment. The 4to1 analog multiplexors are digitally switched via port expander ICs. These multiplexors are tested for switching. Component banks are populated with selected circuit components.

4.2 Performance test

4.2.1 Basic switching and re-configuration test

The computer side software extracts the SPICE listing of the analog circuit to be built. This extracted SPICE listing include the kind, value and node connection information. This extracted list is changed to ACPA and component bank mapping value. These values are transferred to CACB via UART. This test conducted using by sending configuration of simple voltage divider

resistor network (Figure 19 a) and RC filter. The established interconnection is tested using continuity test.

The re-configuration is tested by changing voltage divider. The additional third resistor is added to low side resistor. The additional interconnection is checked using continuity test.

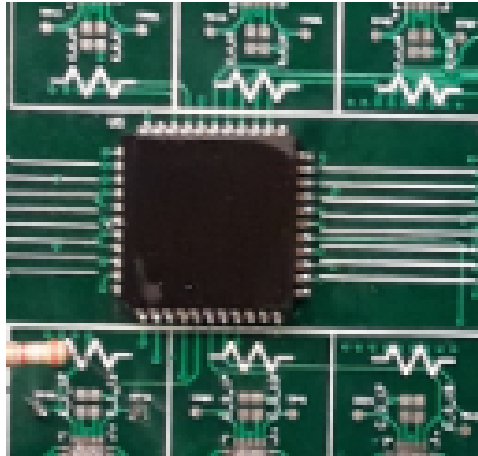
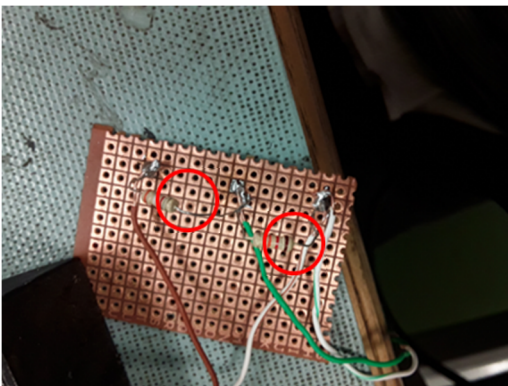


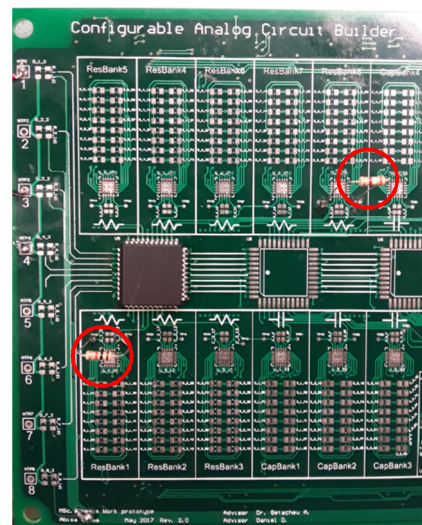
Figure 19: Resistor banks and first ACPA IC.

4.2.2 Voltage Range and Power Test

This analog circuit builder would allow the usage of real components to build to realize analog circuits. The premise that, unlike FPAA's and EPADs this PCB based analog circuit builder can handle better power, is supported by basic voltage range test. The basic voltage swing capabilities of this circuit is tested by using simple voltage divider with different levels of input voltage. The the out put voltage on $R_2=12k$, the power intake are compared



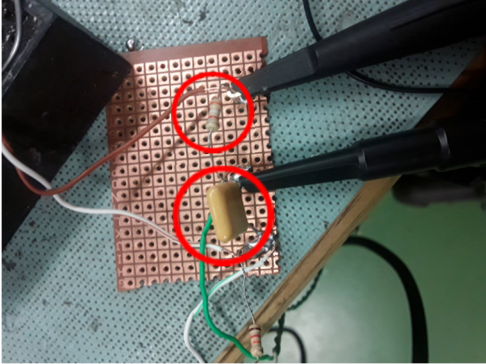
A



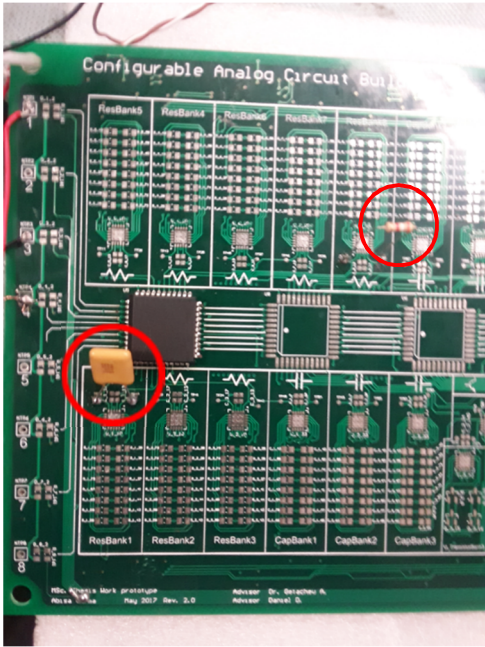
B

Figure 20: Test setup for voltage divider test a) perforated board implemented b) CACB implemented

An RC circuit with input resistor of $R=3.9k$ and output capacitor $4.7\mu F$ is built using soldered perforated board and CACB. The input and out wave forms are captured for comparison. (Figure 21 a Figure 12 b)



a



B

Figure 21 Test setup for RC filter test set up a) perforated board implemented b) CACB implemented

Chapter 5: Result

5.1 Basic functionality testing

5.1.1 Power supply test

The power supply test is performed by supplying 6.5V to the 5V regulator. The single point resistor to power ground to digital ground is shorted to share 5V as VCC supply. A regulated 5V is supplied for all digital VCC requirements.

5.1.2 Programming Test

The Atmega328 is connected to avrdragon via ISP interface (i.e. use SPI pins to Data, Clock, VCC and GND). It is checked for device ID, device voltage automatically. Then it changed to debugger mode trough debugwire feature (Figure 22).

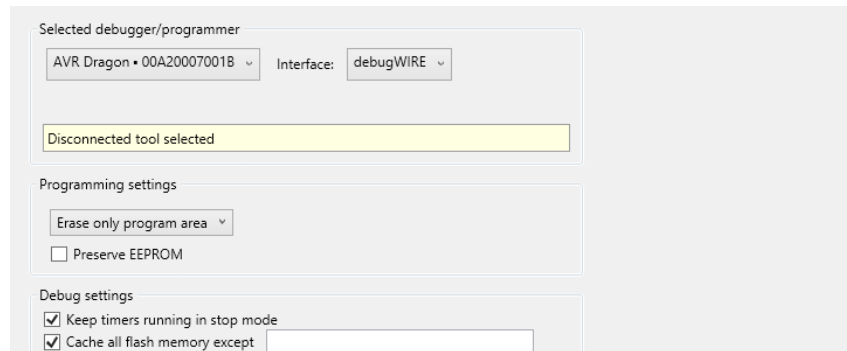


Figure 22 Atmega328 debug mode

5.1.3 Computer interface test

The UART signal is send processor board and an echo program returns every value sent.

5.1.4 Port Expander Interface Test

The sole purpose of using port expander ICs (MCP23S17) is to gate many digital IO pins to drive ACPA ICs (CD22M349MQ) and analog multiplexors. The MCP23S17 is addressed using SPI signal.

SPI library was written to run in 1 MHz clock. Clock and data pins are checked for kind signal by sending a byte in an infinite loop (Figure 23).

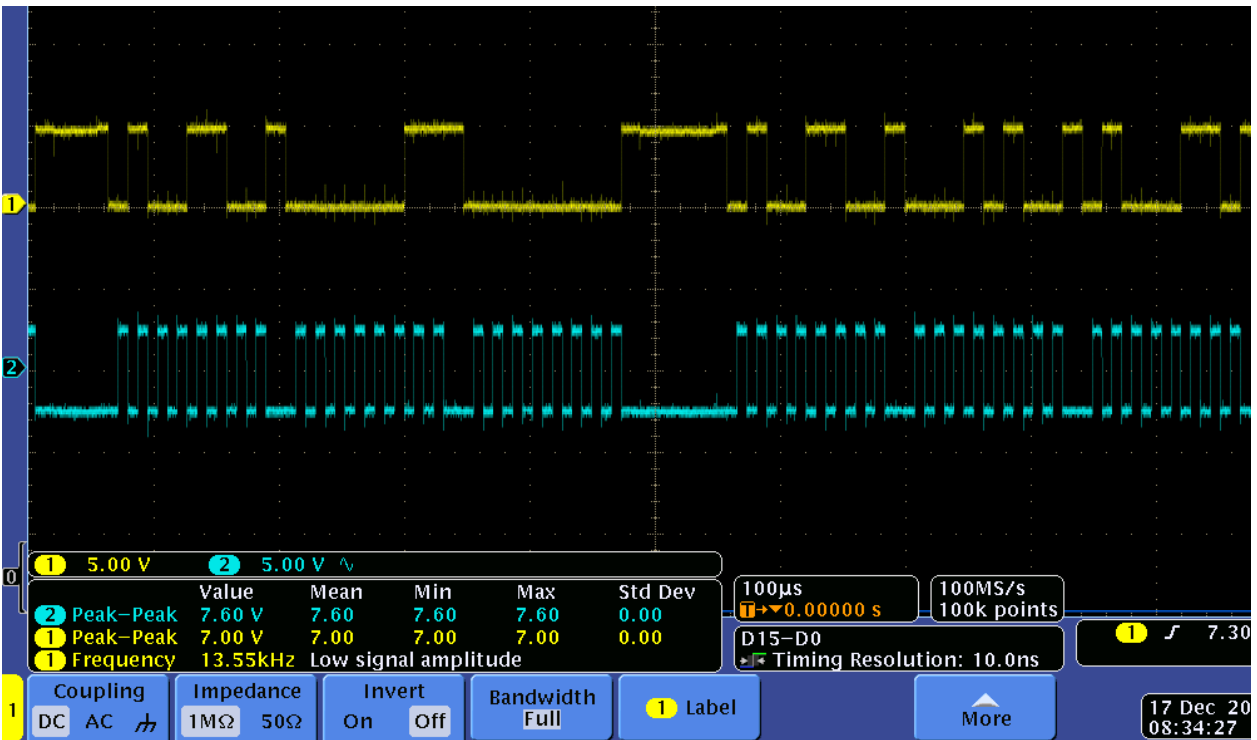


Figure 23 SPI clock and data checking

5.2 Performance test

5.2.1 Basic switching and re-configuration test

The simple voltage divider circuit is formed. The computer side software have selected resistors from Resistor bank 1 and Resistor bank 7. Node Y0, Y2, Y7 correspond to node (Figure 23)

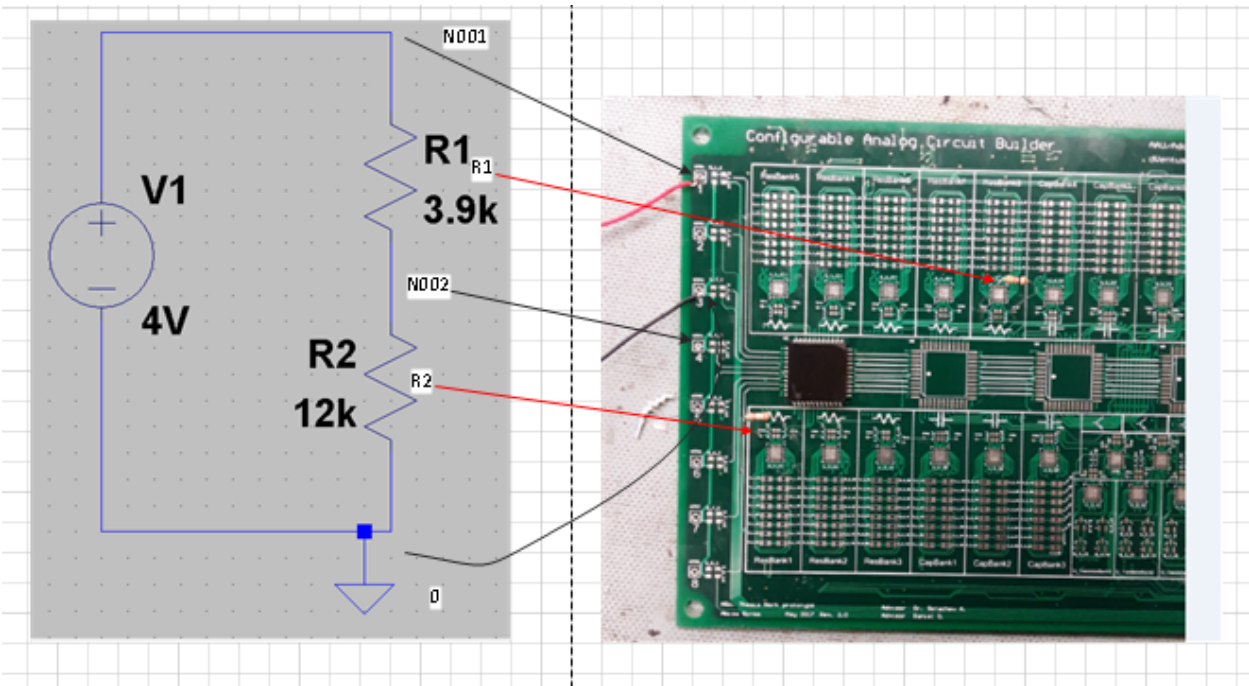


Figure 24 Mapping of circuit on CACB and LT spice schematics capture

The ACPA IC (CD22M349MQ) have added approximately 60 ohms on each interconnection on nodes that have to connections the 80 up to 120 ohms is added to the circuit (Figure 25).

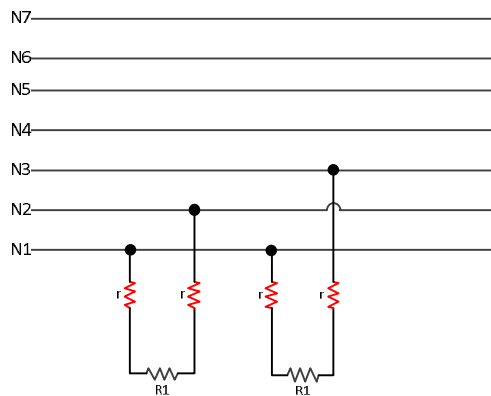


Figure 25 CACB implemented voltage divider switch resistance added

The circuit formation is checked using a millimeter continuity testing. Nodes are formed according schematics diagram intended to be formed.

5.2.2 Voltage Range and Power Test

Voltage divider Test result

A simple comparison of performance between an analog circuit on perforated circuit board and one formed on CACB board. The first circuit that is tested this way was a voltage divider. The voltage divider contain $R1=3.39k$ and $R2=12k$ resistor tied in series. The voltage value across $R2$ is measured. In theory this circuit multiplies an input voltage value 0.75 times. The V_{R2} while being measured from on perforated board circuit implementation value is very similar to the theoretical value(Figure 26). The V_{R2} values while measured form CACB board are similar to the theoretical values.

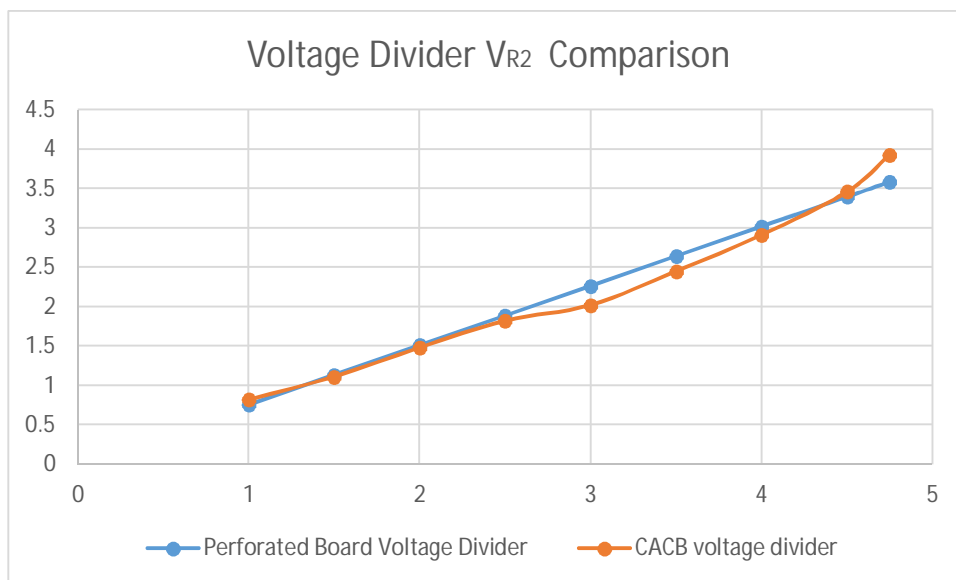


Figure 26 voltage across V_{R2} using perforated board and CACB implemented board

The difference measured between the two implementations is the current (Table 2). There is significantly large current intake by voltage divided built on CACB while there is a very small current(less than 1mA current) taken by voltage divider formed on perforated board.

Table 2: Voltage divider test using CACB

| # | Vin(V) | VR2(V) (ideal) | VR2(V) perforated board | VR2(V) (CACB) | I(mA) CACB |
|---|--------|-------------------|-------------------------------|------------------|---------------|
| 1 | 1 | 0.75 | 0.75 | 0.82 | 32 |
| 2 | 1.5 | 1.13 | 1.13 | 1.11 | 134 |
| 3 | 2 | 1.51 | 1.51 | 1.48 | 208 |
| 4 | 2.5 | 1.89 | 1.88 | 1.82 | 280 |
| 5 | 3 | 2.26 | 2.26 | 2.02 | 335 |
| 6 | 3.5 | 2.64 | 2.64 | 2.45 | 387 |
| 7 | 4 | 3.02 | 3.02 | 2.91 | 397 |
| 8 | 4.5 | 3.40 | 3.4 | 3.46 | 407 |
| 9 | 4.75 | 3.58 | 3.59 | 3.93 | 406 |

The voltage divider formed on CACB board resulted on more heating with a thermal rise of $42.6^{\circ}\text{C}-19.3^{\circ}\text{C}=23.3^{\circ}\text{C}$. The analog cross point array introduces a current leakage that resulted in heating effect for voltage divider circuit.

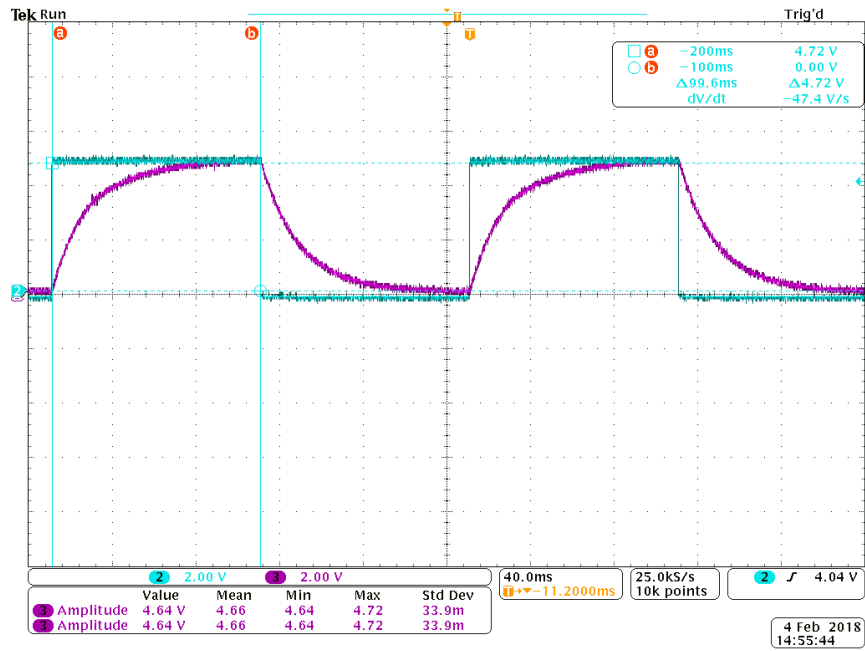
For resistive network the effect of additional switch resistance may be tolerable. A circuit network made of resistor values that are greater than switch resistances in orders of 8 up to 10 times could function with small loss of functionality. The actual loss of performance is subjected to kind and sensitivity of the particular circuit network.

The voltage divider consumes 4.75V by 0.409A which 1.94 watt. This shows that the CACB board could be used within the bounds nearly 2 watts. The switch resistances have added heat loss. Which can reduce performance range.

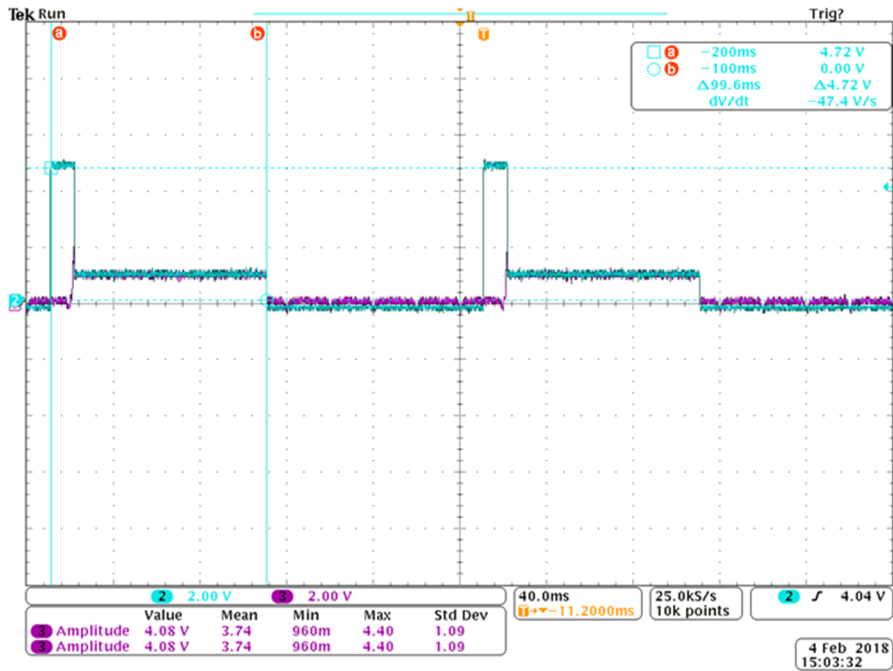
RC filter Test Result

The second voltage tested in parallel comparison is a RC filter circuit. The RC filter contains 3.9k resistor and 4.7uF capacitor. While RC circuit built on perforated board shows a typical capacitor charge discharge voltage curve (shown in Figure 27 a).

The CACB implemented RC filter exhibits an entirely different characteristic curve (shown in Figure 27 b). The input square wave is attenuated and the output voltage is changes to narrow pulse trains. The addition of resistance on the pins and current leakage exhibited on the voltage divider circuit had adverse effect the output characteristics.



A



B

Figure 27 Test Result of RC circuit test a) perforated board implemented b) CACB implemented

Chapter 6: Conclusion and Recommendation

Generally Analog circuits still hold a significant role in most aspects of electrical and electronics design. The building of analog circuits play an important role in analysis and synthesis of analog processing systems. Analog circuits are built on bread board, using solder balls, on printed circuit and using other various technologies. The testing of analog circuit like in the cases of FPGA, in digital design, could be done using configurable kits. One alternative are FPAA. FPAA are not that much commercialized and require their own vendor specific CAD software packages.

In this study a cross bar network based analog circuit builder is implemented. PCB with cross point array switches and multipliers were used together to realize a CACB kit. This CACB is suggested as ragged alternative for analog circuit building.

PCB is designed and fabricated according to simple architecture. The PCB was gradually assembled and tested with computer side software and processor side firmware. In terms functionality the CACB can achieve the building of circuit interconnections. The analog switches in cross point array add unwanted resistance on interconnection. This makes the ACPA IC heat easily reducing the operational range. This also create the addition on board power sources difficult as it adds resistance on power supply path. Analog cross point arrays with low on resistance of switch are poor in voltage swing range. This bring about a tradeoff performance.

The versatility and kinds of components could be limited by space and cost. Modular implementation CACB could be more cost effective and versatile if it has been implemented in modular manner. Modularity could also add to flexibility on the user end.

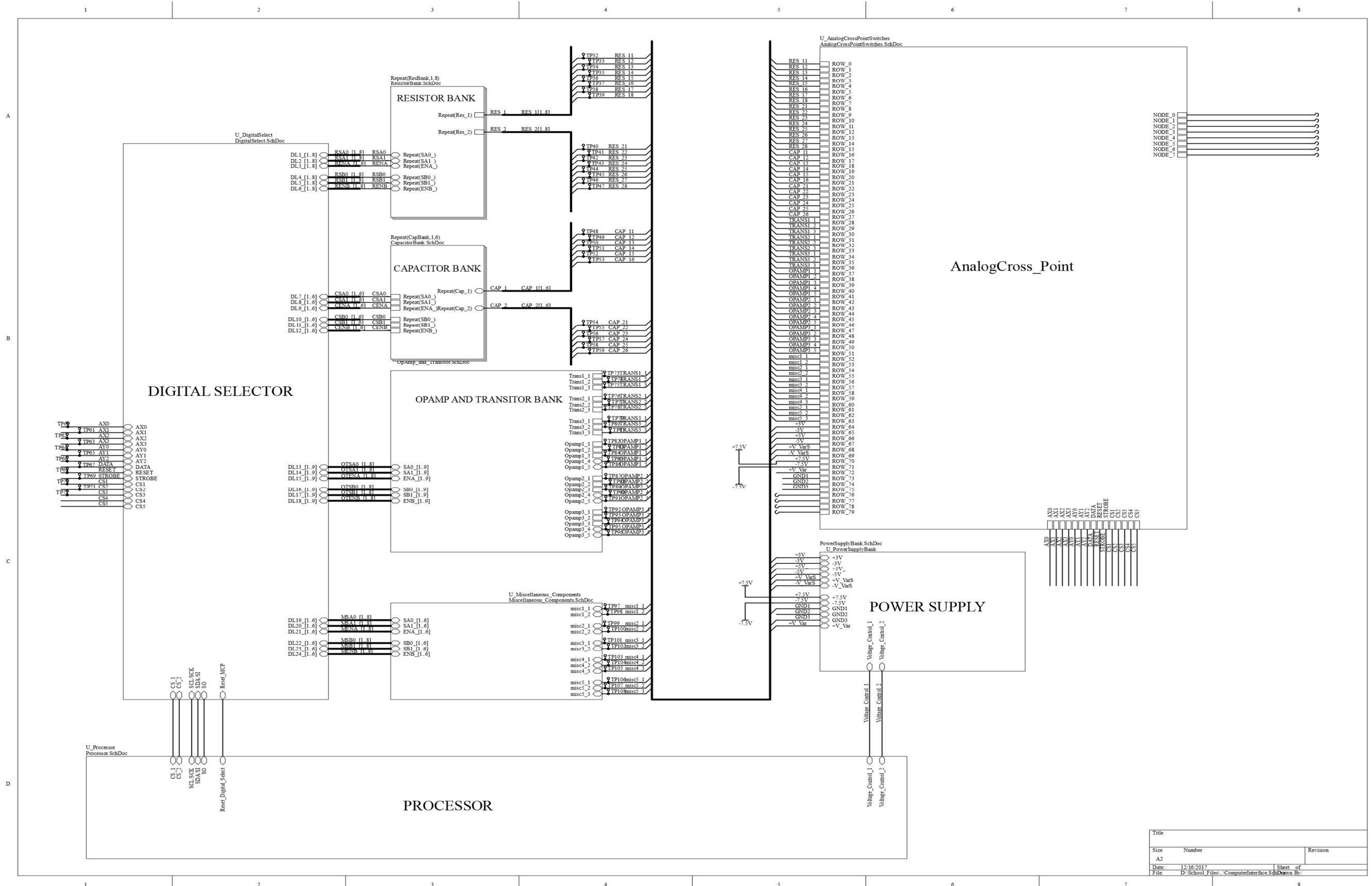
Further developments could be possible which intern could achieve better results or be better marketable. Modularization and or using better network could be tried. Even further debugging, emulation and synthesis features could be tried for better functionality.

Generally, the CACB is viable attempt to simplify analog circuit building and testing. This could be helpful in both industry and academia.

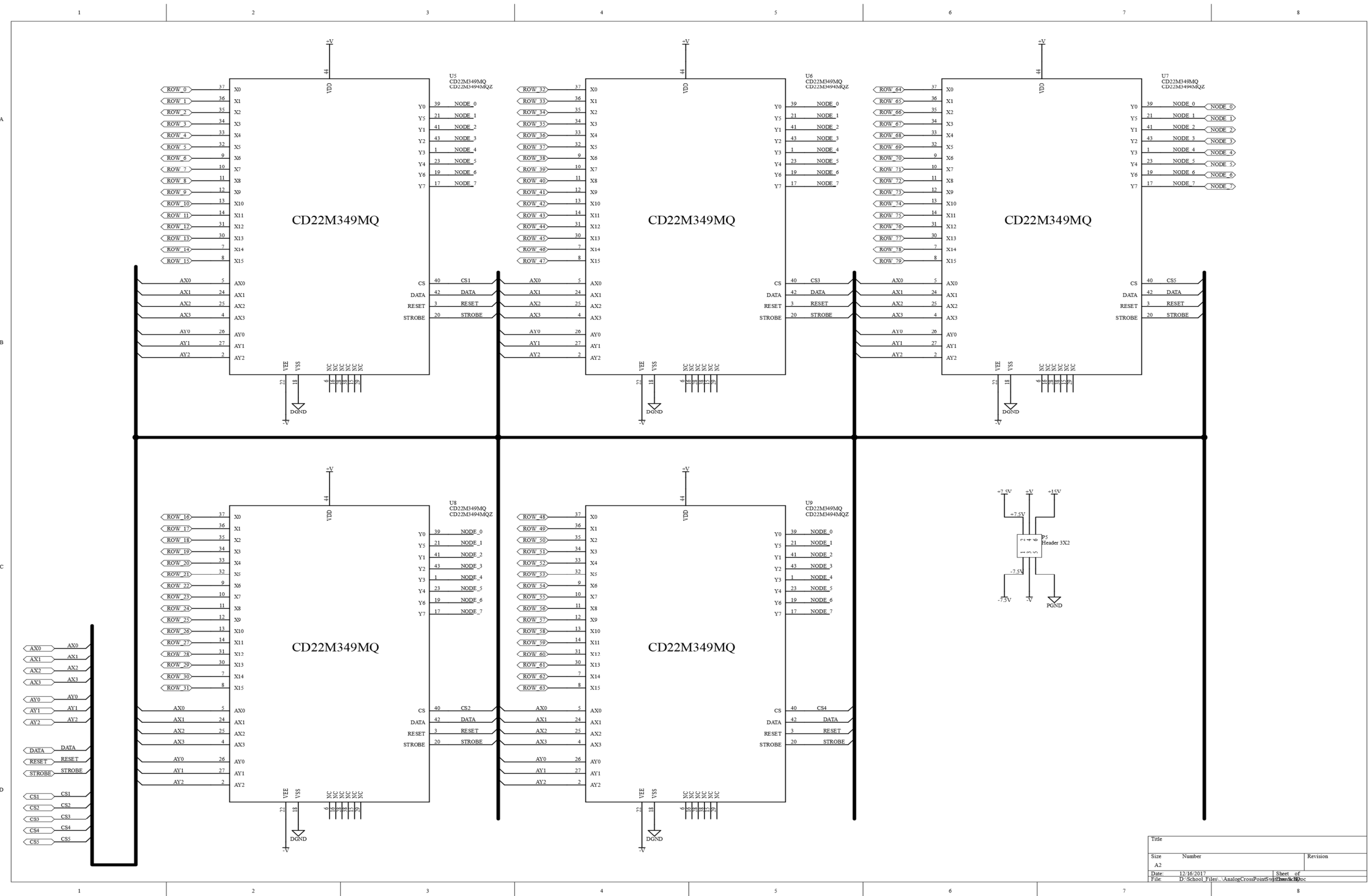
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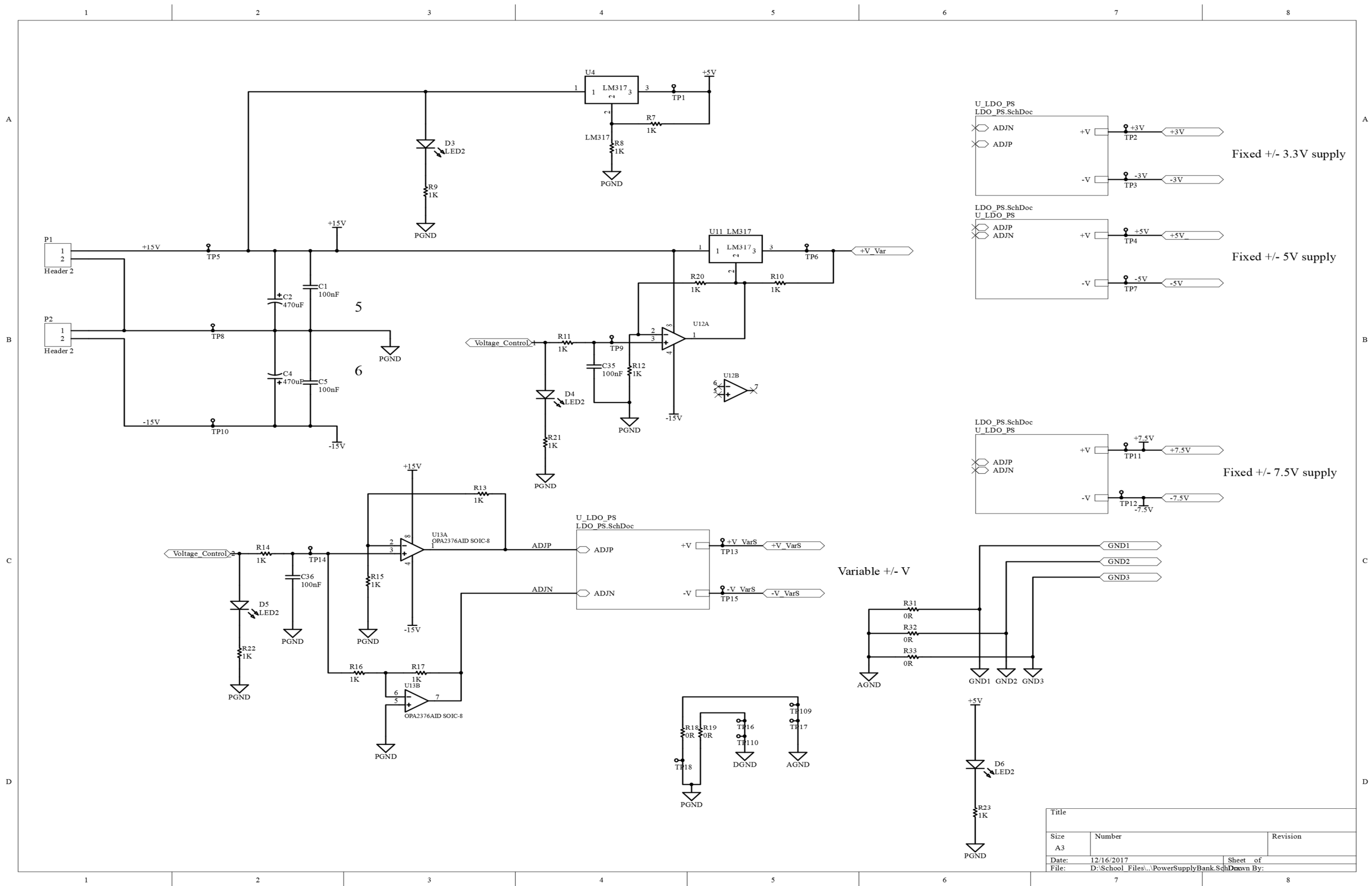
Appendix A: CACB schematics

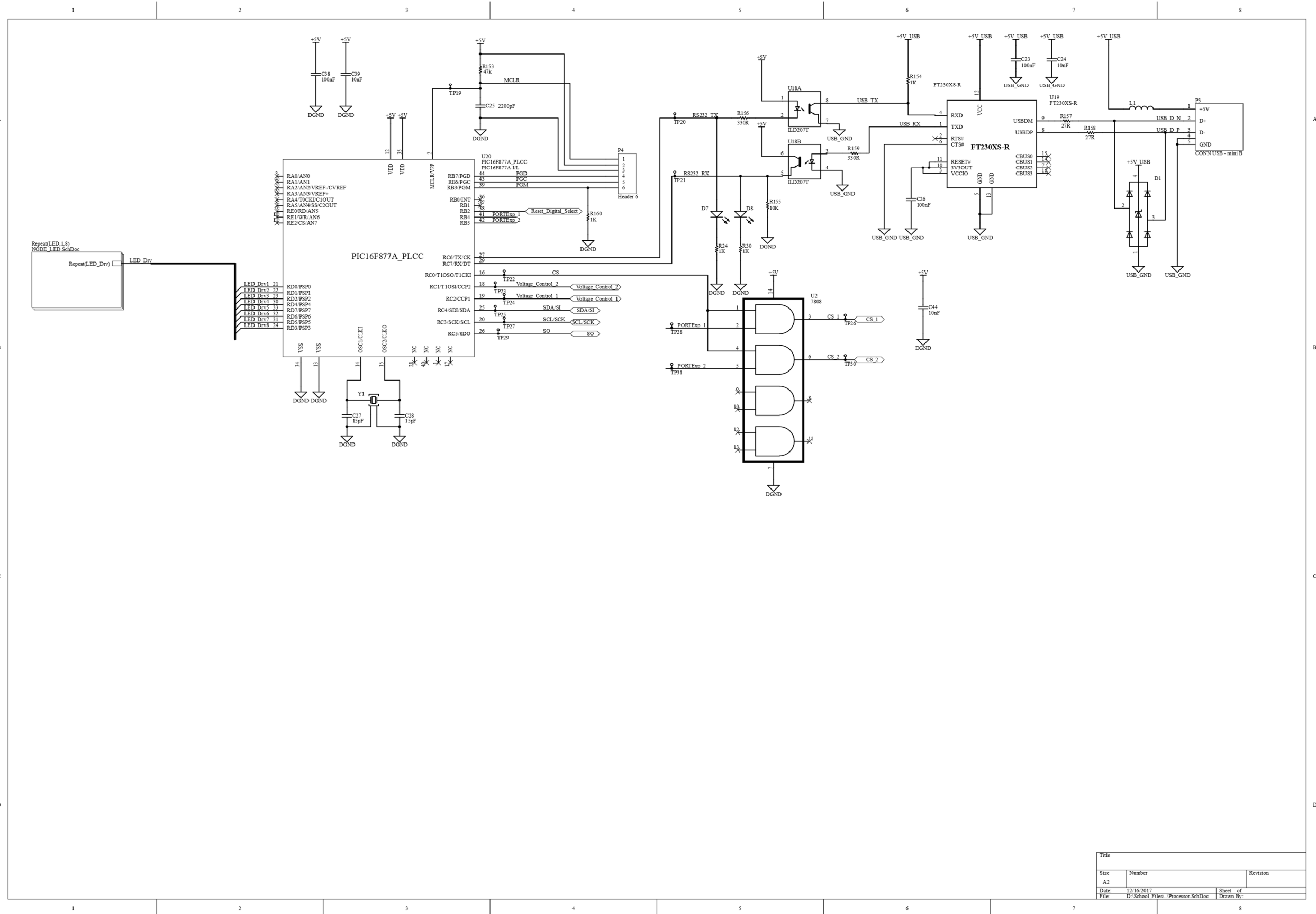


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| File: | D:\School Files - ComputerInterfaceSchDoc\Drawn By: | |

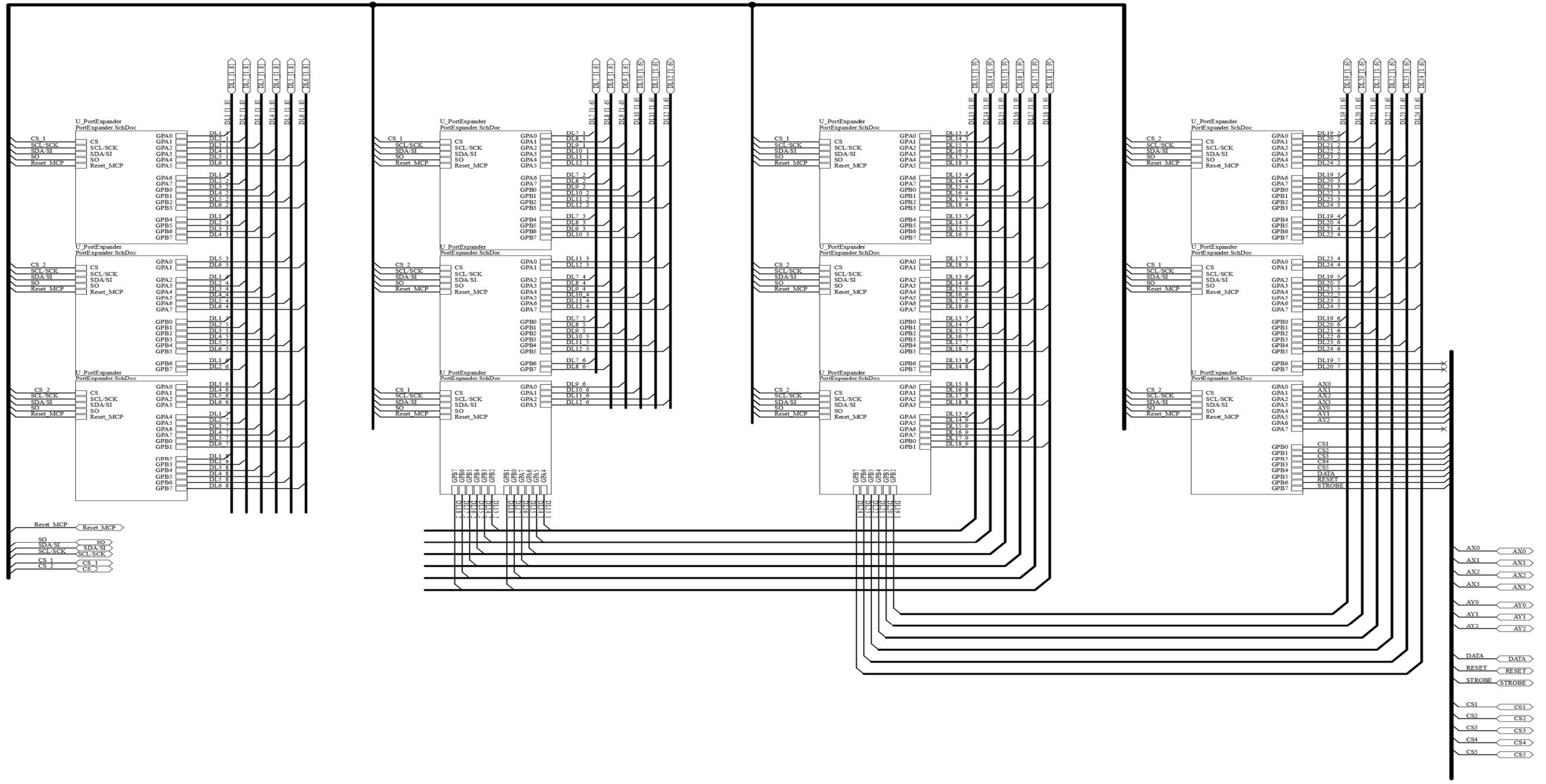


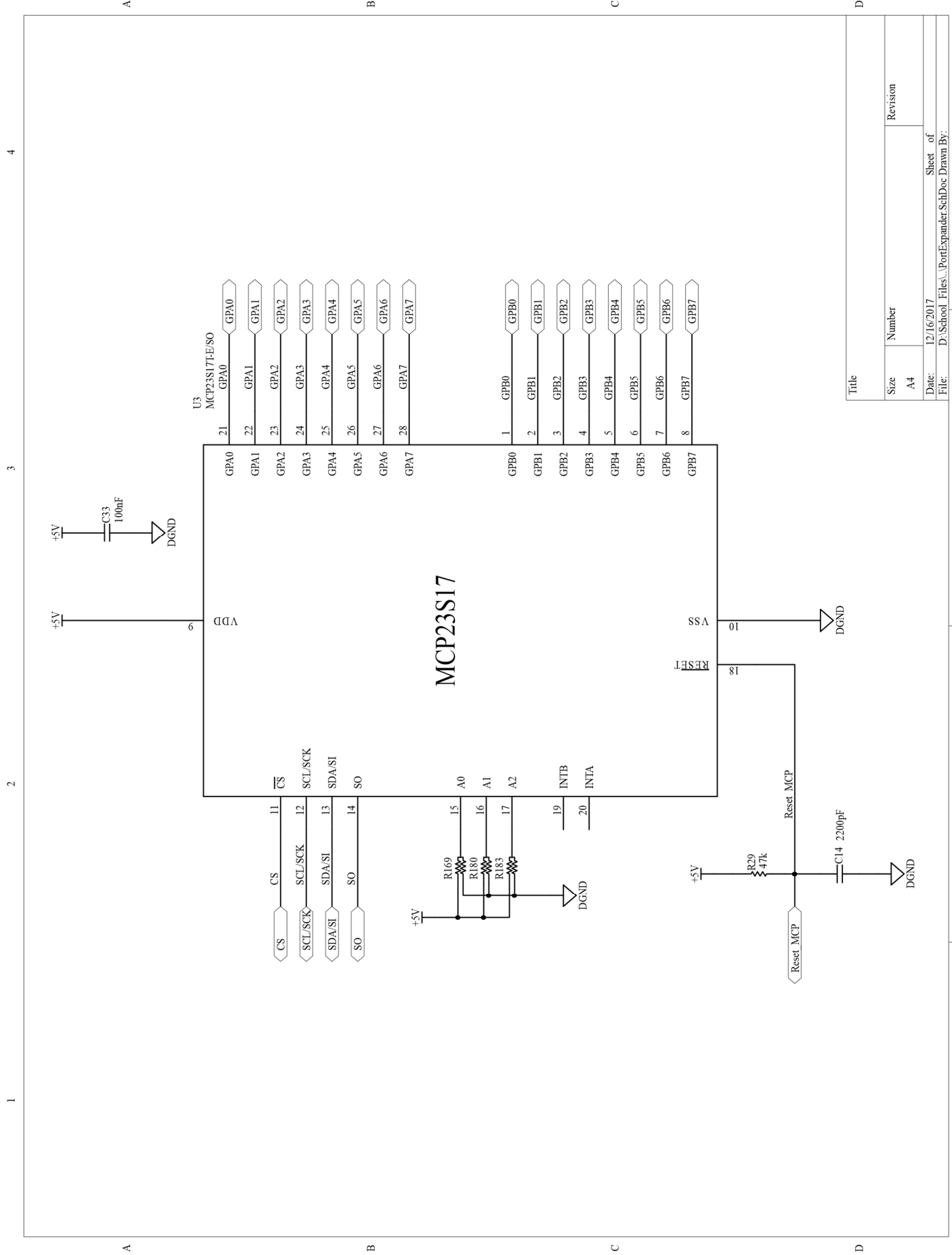
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| File | D:\School Files\...AnalogCrossPointS...10.brd | 10 of 10 |



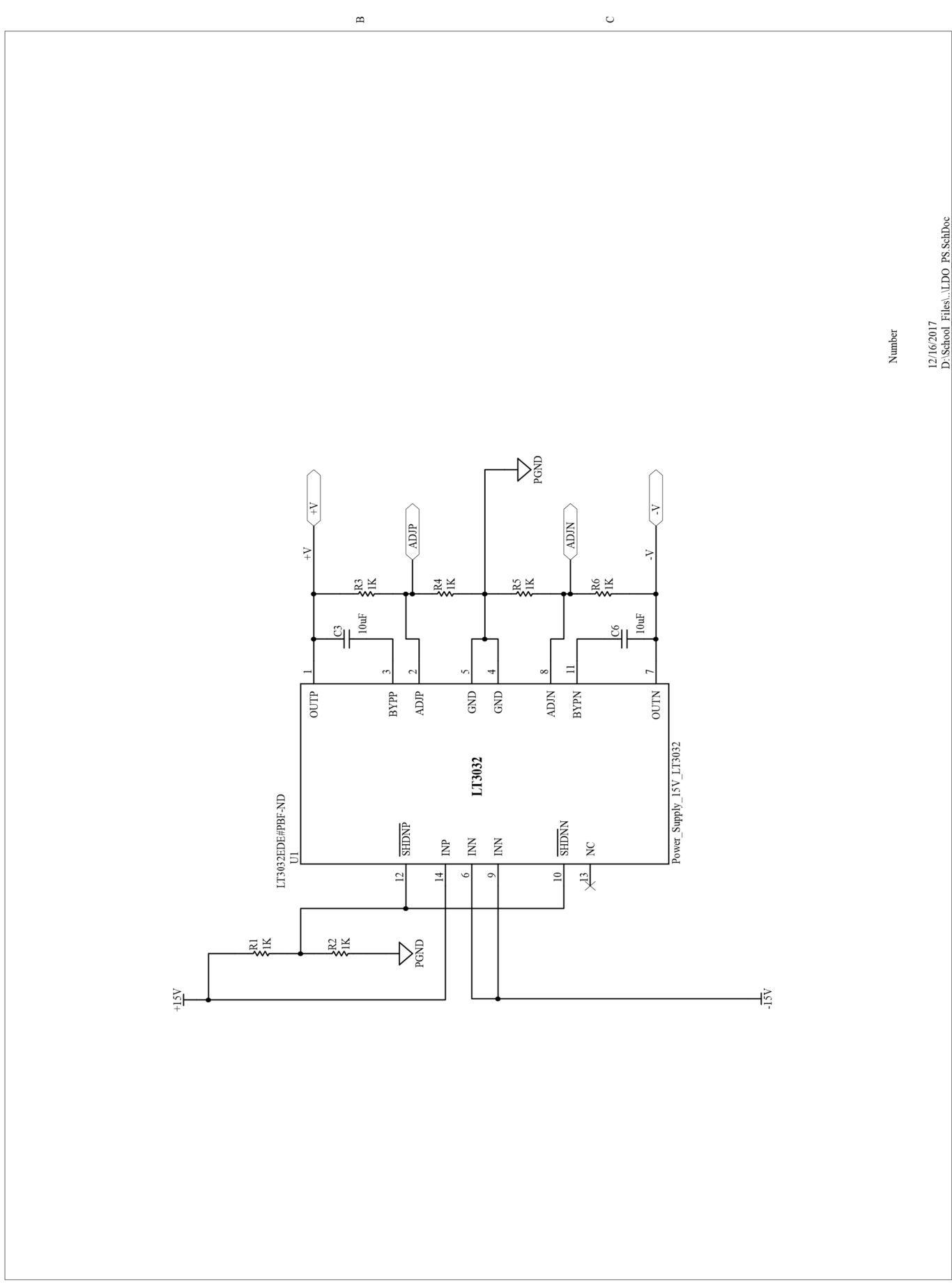


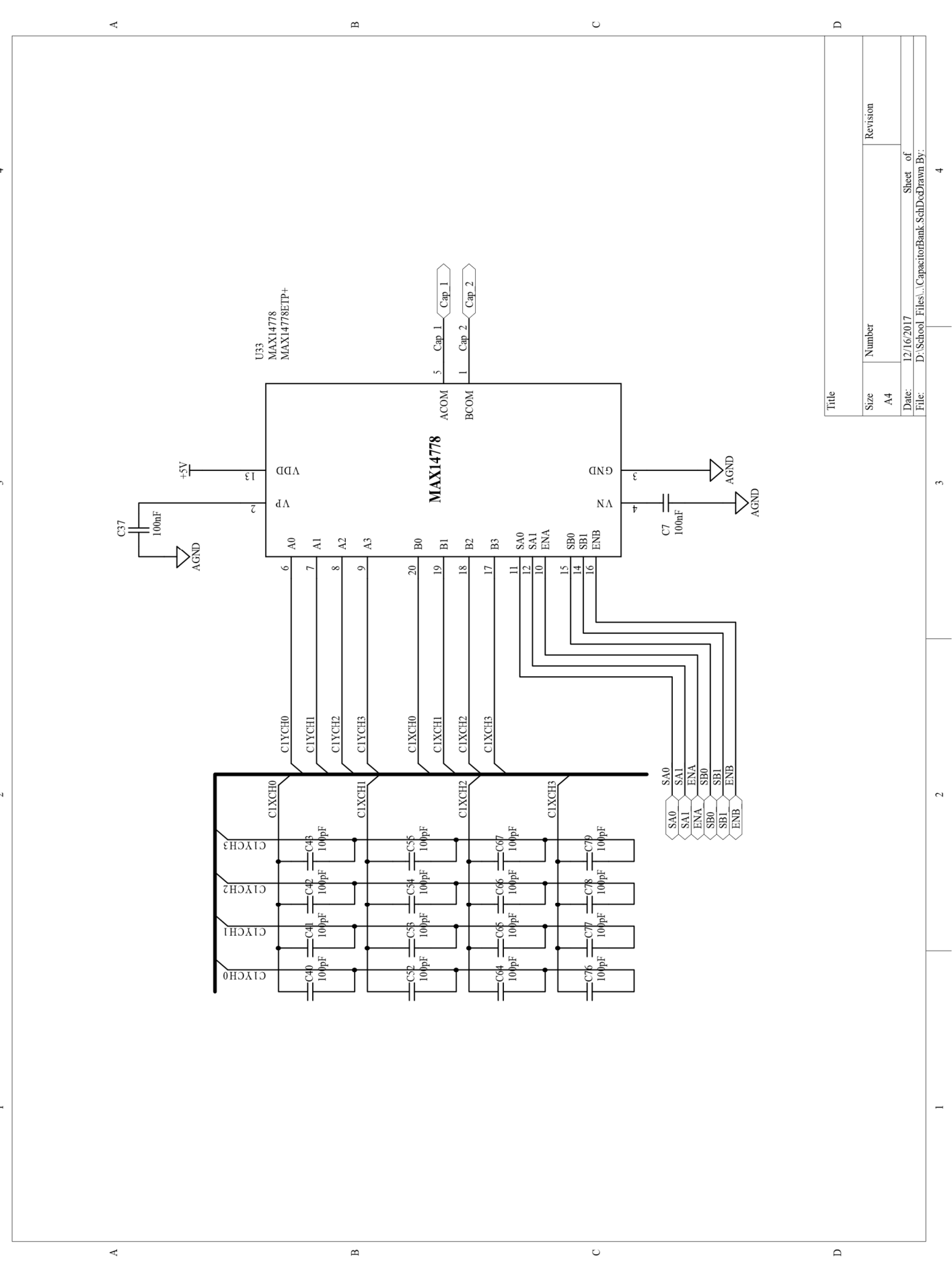
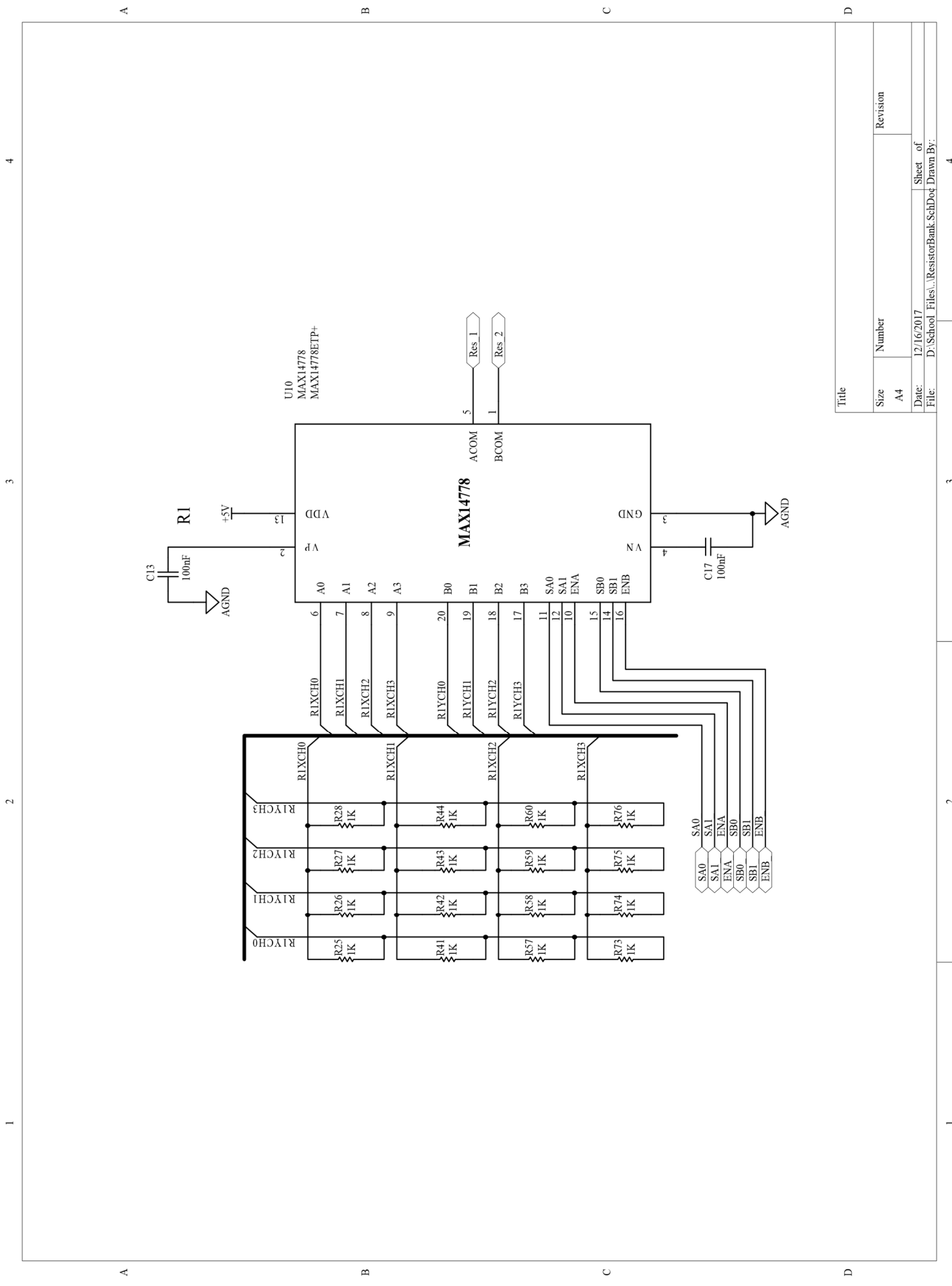
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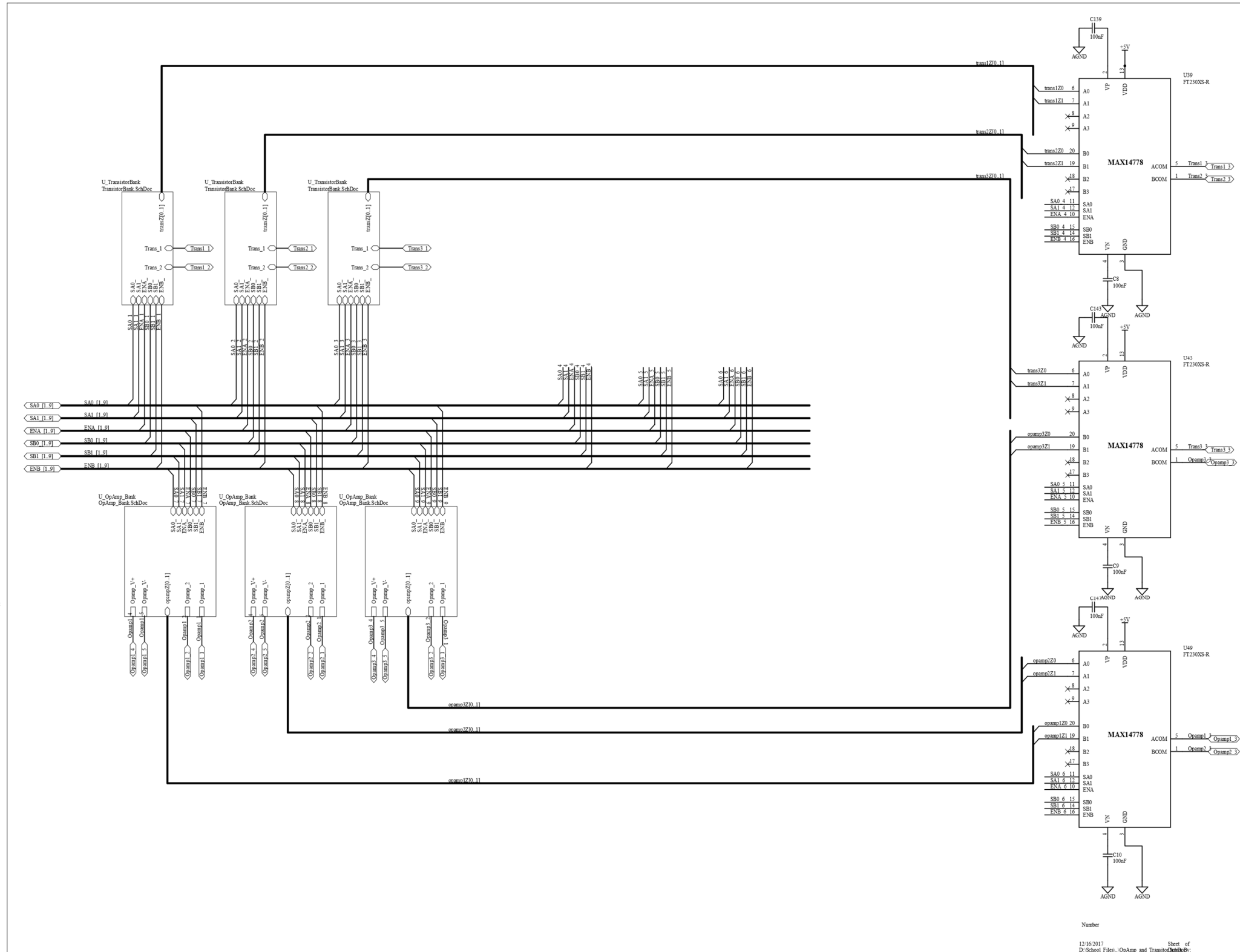


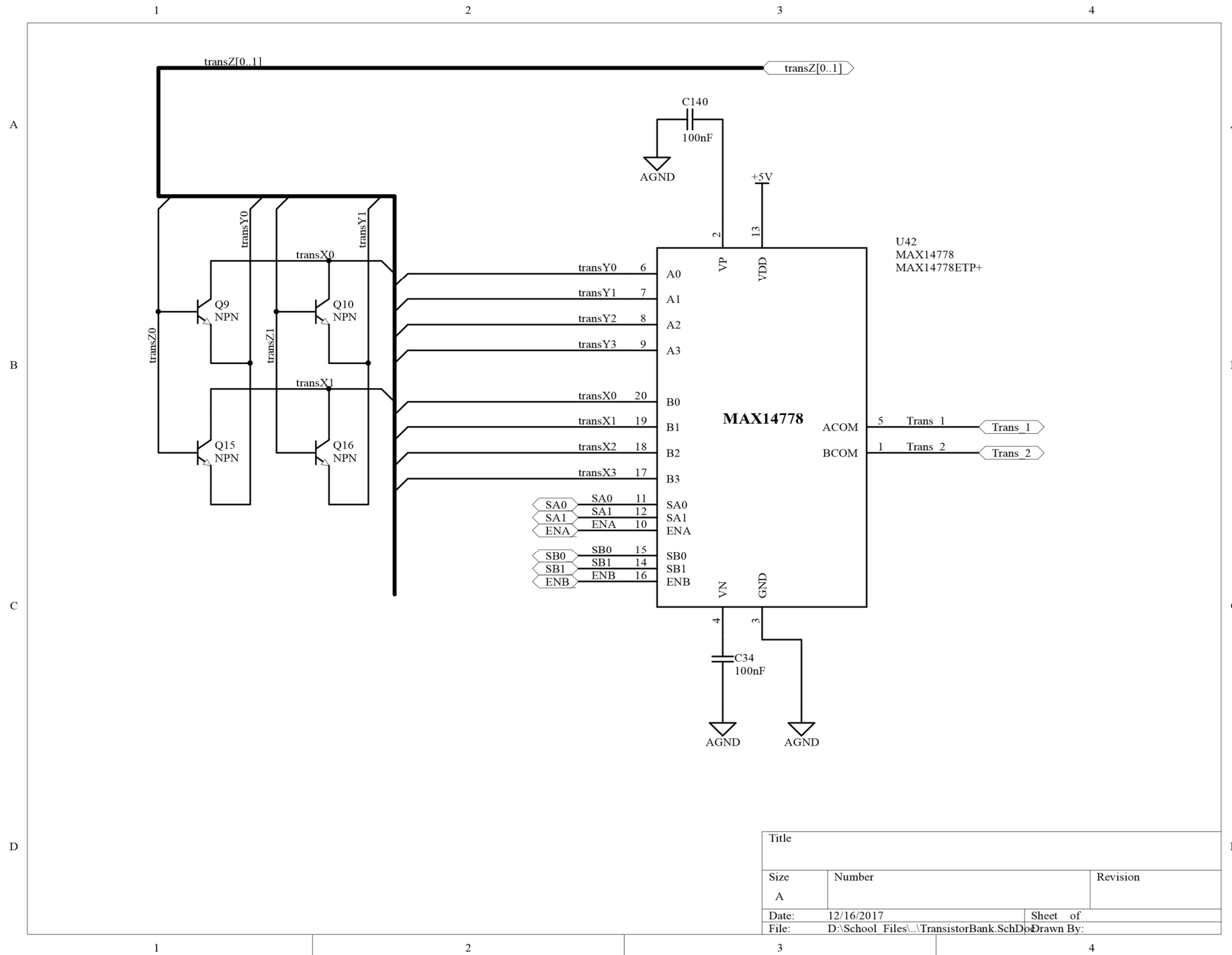


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| File: | D:\School Files\...\TransistorBank.SchDoc | |
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Appendix B: Processor Side code listing

```
/*
 * CACB_Processor.c
 *
 * Created: 9/29/2017 6:37:10 PM
 * Author : asiba
 */
#define F_CPU 1600000UL
#include <avr/io.h>
#include <avr/interrupt.h>
#include <util/delay.h>
#include <avr/sleep.h>
#include "spi.c"
#include "CACB_Port_Expander.c"
#include "uart.c"
#include "CACB_Cross_Point_Array.c"
int8_t eco=0;
volatile int8_t rx_buffer_full=0;
ISR(USART_RX_vect)
{
    rx_buffer_full= BufferWrite();

    if (rx_buffer_full==1)
    {
        //disable reception and RX Complete interrupt
        UCSR0B &= ~((1<<RXEN0)|(1<<RXCIE0));
        //enable transmission and UDR0 empty interrupt
        UCSR0B |= (1<<TXEN0)|(1<<UDRIE0);
    }
}
//UDR0 Empty interrupt service routine
ISR(USART_UDRE_vect)
{
}
```

```

void setup(void);

int main (void)
{
    setup();
    DDRD=0b00000010;
    //Init buffer
    BufferInit();
    USART0Init();
    SPI1_Init();

    PORTB|=(1<<PORTB0); //the first group of 6 port expanders
    PORTB|=(1<<PORTB1);

    //enable global interrupts
    sei();
    PORTC=0xAA;
    rx_buffer_full=0;
cross_point_write();
    int8_t i=3;
    while(1)
    {
        PORTC=0xFF;
        PORTC&=~(1<<i);
        _delay_ms(500);
        PORTC|=(1<<i);
        _delay_ms(500);
    }
}

void setup(void)
{
    DDRB = 0xFF;
    DDRC = 0xFF;
    //DDRD=0xFF;
    DDRD=0b00000010;
    SPI1_Init();
    USART0Init();

}

```

```

#define F_CPU 1600000UL
#include <avr/io.h>
#include "CACB_Port_Expander.h"
#include "spi.h"
unsigned short i=0,j=0;
unsigned short group_flg=0;
//unsigned short group_flg=0;
uint8_t
mux_val[24]={0xFF,0xFF,0xFF,0x55,0xFF,0xFF,0xFF,0xFF,0xFF,0x55,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0
xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF};
//1,2,3,4,5,6,7,8,9,10,11,255,13,14,15,16,17,18,19,20,21,22,23};
void group(uint8_t group_fl)
{
    switch (group_fl)
    {
        case 0:
            PORTB&=(1<<PORTB0)|~(1<<PORTB1);

            break;

        case 1:
            PORTB&=~(1<<PORTB0)|(1<<PORTB1);

            break;
    }
}

void setup_MCP23S17(char address)
{
    MCP23S17_write(IOCON, 0x38,0x40|(address<<1));
    MCP23S17_write(IODIRA, 0x00,0x40|(address<<1));
    MCP23S17_write(IODIRB, 0x00,0x40|(address<<1));
    MCP23S17_write(GPPUA, 0x00,0x40|(address<<1));
    MCP23S17_write(GPPUB, 0x00,0x40|(address<<1));
    MCP23S17_write(IPOLA, 0x00,0x40|(address<<1));
    MCP23S17_write(IPOLB, 0x00,0x40|(address<<1));
}

```

```

void MCP23S17_write(char address,char value,char H_address)
{
    group(group_flg);

    SPI1_Write(H_address);
    SPI1_Write(address);
    SPI1_Write(value);
        PORTB|=(1<<PORTB0); //the first group of 6 port expanders
        PORTB|=(1<<PORTB1);
        // PORTB0=1;
        // PORTB1=1;

}
void byte_send(char A_byte,char B_byte,char address)
{

MCP23S17_write(OLATA, A_byte,0x40|(address<<1));
MCP23S17_write(OLATB, B_byte,0x40|(address<<1));
}
void write_byte_array()
{
group_flg=0;
group(0);
        for(i=0;i<6;i++)
        {
            setup_MCP23S17(i);
        }

        for(i=0;i<6;i++)
        {
            byte_send(mux_val[2*((j*6)+i)],mux_val[2*((group_flg*6)+i)+1],i);
            //byte_send(170,170,i);
        }

group_flg=1;
group(1);
        for(i=0;i<6;i++)
        {
            setup_MCP23S17(i);

```

```

    }
    for(i=0;i<6;i++)
    {
        byte_send(mux_val[2*((group_flg*6)+i)],mux_val[2*((j*6)+i)+1],i);
        //byte_send(170,170,i);
    }
}

#include "CACB_Port_Expander.h"
#include "CACB_Cross_Point_Array.h"
#include "uart.h"
#include <util/delay.h>
int8_t cs_val=0; // chooses between 5 cross point array switches
int8_t addr_val=0; // chooses the address byte
int8_t config_port=0;
int8_t switch_val=0;
volatile int8_t switch_state[80];
int8_t switch_s[16]={ 1,0,0,2,0,132,0,0,0,0,0,0,0,0,0,0};
//-----
    int8_t byte_group=0;
    int8_t byte_pos=0;
    int8_t bit_pos=0;
    int8_t bit_val=0;
    int8_t bitmask=0;

/////

void cross_point_write()
{
    uint8_t dflt_conn=0;

    for (dflt_conn=0;dflt_conn<16;dflt_conn++)
    {
        switch_state[dflt_conn]=switch_s[dflt_conn];
    }

//    copy_acpa_bytes();
    int8_t DAT=0;
    //group(0);

```

```

for (cs_val=0;cs_val<2;cs_val++)
{
    for (addr_val=0;addr_val<127;addr_val++)
    {
        group_flg=0;
        config_port=0;
        config_port|=1<<cs_val;

        // 7           6           5           4:0
        DAT=switch_bit(addr_val,cs_val);
        UART_Transmit(addr_val);
        UART_Transmit(DAT);
        config_port|=(DAT<<5); // strobe
RESET DATA cs4-cs0
        config_port=config_port&(~(1<<7));
        config_port=config_port&(~(1<<6));

        //write on address and configuration port(PORTA and PORTB of MCP23S17) strobe
low

        //config_port|=0x40;
        //_delay_us(5);
        setup_MCP23S17(6);
        byte_send(addr_val,config_port,6); //byte_send(char A_byte,char B_byte,char address)
        //write on address and configuration port(PORTA and PORTB of MCP23S17) strobe
high

        _delay_us(1);

        setup_MCP23S17(6);
        config_port=config_port|((1<<7));
        config_port=config_port&(~(1<<6));
        byte_send(addr_val,config_port,6);
        //write on address and configuration port(PORTA and PORTB of MCP23S17) strobe
low

        _delay_us(1);
        config_port=config_port&(~(1<<7));
        config_port=config_port&(~(1<<6));
        setup_MCP23S17(6);
        byte_send(addr_val,config_port,6);

```

```

        _delay_us(1);
    }
}

int8_t switch_bit(int8_t sw_pos,int8_t cs)
{
    bitmask=0;
    bit_val=0;
    byte_group=0;
    bit_pos=0;
        byte_group=cs<<4;
        byte_pos=(sw_pos/8)+byte_group;
        bit_pos=sw_pos%8;

        bitmask=(1<<bit_pos);
        bit_val=switch_state[byte_pos];
        bit_val&=bitmask;
        bit_val=bit_val>>bit_pos;
return bit_val;
}

void node_show(int8_t address,int8_t dat)
{
    int8_t y=address>>4;
    PORTC=0xFF;
    if (dat==1)
    {
        PORTC=PORTC&(~(1<<y));
    }
}

```