ADDIS ABABA UNIVERSITY

ADDIS ABABA INSTITUTE OF TECHNOLOGY

SCHOOL OF GRADUATE STUDIES

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Modeling Carbon Nanotube Field Effect Transistor for Analog and Digital Circuit Design with VHDL-AMS

A thesis submitted to the school of graduate studies in partial fulfillment of the requirements of degree of

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(Microelectronics)

By

Demisew Teferi Mokonnen

Advisor: - Dr. Adeyabeba Abera

July 2011

Addis Ababa, Ethiopia

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Name: Demisew Teferi Mokonnen

Signature: ____________

Place: Addis Ababa

Date of submission: July 2011 G.C.

This thesis has been submitted for examination with my approval as a university advisor.

Dr. Adeyabeba Abera _____________________

Advisor's Name Signature

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ABSTRACT

The objective of this thesis is to study the basic electronic properties of carbon nanotubes (CNTs here after) and to model the I-V characteristics of metal-oxide-semiconductor field-effect transistor like carbon nanotube field effect transistor (MOSFET-like CNTFET). And finally validate the model by constructing circuits. Electronic properties such as energy band structure, density of state, carrier density, carrier velocity and effective mass are investigated. A complete analytical model of MOSFET-like CNTFET is developed and it was validated by construction of circuits. MOSFET-like CNTFET is chosen because of their relative unipolar property. The model developed is based on analytical calculation of channel potential using electrostatic capacitance and quantum capacitance. Electron phonon scattering effect, band to band tunneling effect (BTBT), source/drain doped region resistance and contact resistance effects are considered in this model. The model requires neither iteration nor numeric integration, hence suitable for hardware description language (HDL) implementation. The model was implemented in VHDL-AMS. Parameters such as gate insulator thickness, gate insulator dielectric constant, CNT diameter, channel length and temperature are examined to observe the performance dependency. Results showed that reducing insulator thickness and increasing dielectric constant improve performance with no compromise other than cost. Channel length scaling increases on-current and also increases off-current, for high bias voltage due to BTBT effect. In addition, the effect of temperature on performance of MOSFET-like CNTFET and the dependency of threshold voltage on diameter of CNT was observed. Finally, using the VHDL-AMS model, circuits were constructed. Resistive-Load inverter, CMOS inverter, and phase shift oscillator circuits are constructed, simulated, and analyzed.

CHAPTER 1
INTRODUCTION

1.1 Background

Since the introduction of transistors, continuous reduction of electronic circuit size and power dissipation have been the ongoing theme in electronics industry. Moore's law, initiated by Gordon Moore, Intel's founder, represents this evolution [1]. According to this law it is predicted that the performance of integrated circuit will double in every 18 months. However, as the feature size becomes smaller, scaling the silicon MOSFET becomes increasingly harder. This increasing challenge is due to short channel effects [2, 3], which introduce leakage currents, such as tunneling of carriers through the thin gate oxide, from source to drain and from drain to body, and technology limit such as control of the density and location of dopant atoms in the channel and source/drain region to provide high on/off-current ratio.

There are many solutions proposed to circumvent these limitations. Some solutions include modifications on the existing structures and technologies in hopes of extending their scalability. One such example is the use of double gate instead of single gate in conventional MOSFET in which case the additional gate is used to provide a stronger control of the channel potential by gate bias [4]. Other solutions involve using new materials and technologies to replace the existing silicon MOSFETs. Some of the new devices proposed to replace silicon MOSFET are nanowires [5] (such as ZnO nanowire transistors, silicon nanowire transistors), carbon nanotube transistors, and single electron tunneling (SET) transistors, and graphene nanoribbon transistors. Among these new device structures carbon nanotube transistors are regarded as the most promising device to replace conventional silicon transistors [6].

1.1.1 Carbon Nanotube Properties

Carbon nanotube (CNT) based electronics are currently considered as promising building blocks of a future nanoelectronic technology due to unique properties of CNTs such as [7]:

- CNTs are one dimensional (1-D) device and, hence, carrier transport is 1-D. This implies a reduced phase space for scattering of the carriers and opens up the possibility of nearly ballistic transport which implies low power dissipation.

- All chemical bonds of the carbon atoms are satisfied and there is no need for chemical passivation of dangling bonds as in silicon. This implies that CNT electronics would not be bound to use SiO_2 as an insulator. High dielectric constant and crystalline insulators can be used.
- The strong covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration which is main problem when existing metals (such as Cu, Al) are used as interconnect at nanoscale level.
- In principle, both active devices (transistors) and interconnects can be made out of semiconducting and metallic nanotubes, respectively.

In addition, medium scale integrated circuits with more than 100 CNT thin-film transistors (TFTs) have been successfully fabricated [8]. Figure 1.1 shows 53-stage ring oscillator (the largest, in number, CNT-based integrated circuits reported so far).

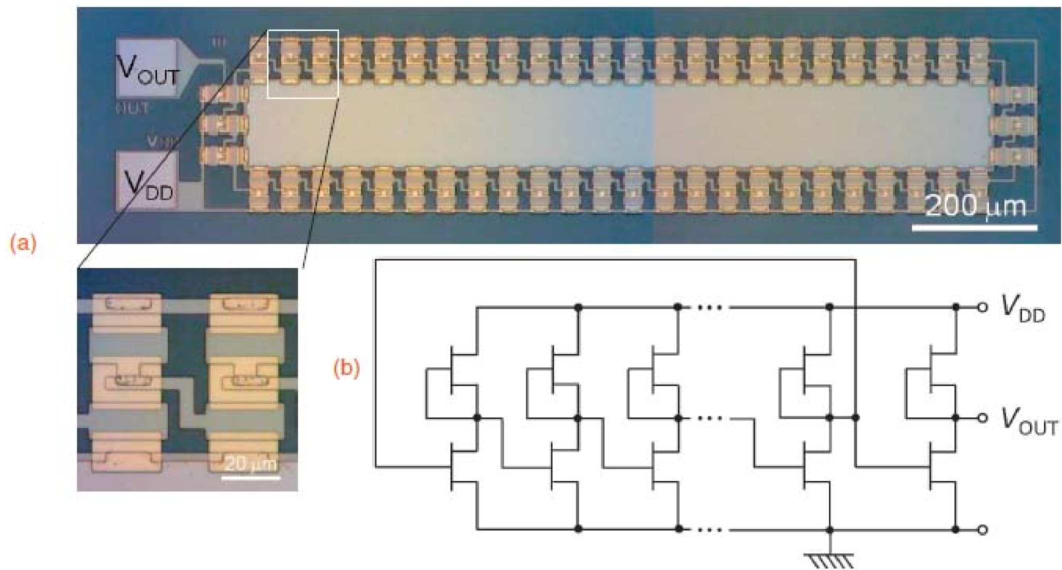


Figure 1.1(a) 53-stage ring oscillator with an output buffer, (b) Ring oscillator circuit with an output buffer [8].

The performance of any transistors is improved when scaled before reaching certain limits. It has been reported theoretically that the scaling of channel of carbon nanotube field effect transistor (CNTFET, here after) up to 50 Å (5 nm) is possible with adequate switching characteristics [9]. Also it is reported as scaling improves performance of CNTFET with substantial increases in on-current and resistances closer to the quantum limit [10]. The smallest CNTFET to date is demonstrated having channel length, $L_g \approx 20$ nm with super

performance; increase in on-current and drop in low-field resistance, both from reduced scattering in the channel [11]. These experimental demonstrations make CNTFET very promising for future electronics.

1.1.2 Carbon nanotube field effect transistors

Carbon nanotube field effect transistor (CNTFET), first demonstrated in 1998 [12, 13], is three (or four, if bulk is considered as fourth) terminal device. It consists of a semiconducting CNT bridging two contacts (source and drain) and acting as a carrier channel. Channel is turned on or off electrostatically using the third contact called gate. CNTFET can be categorized into two major types based on their principle of operations; (1) Schottky barrier CNTFET (SB-CNTFET) and (2) MOSFET-like CNTFET or sometimes called Conventional CNTFET (C-CNTFET). It can also be categorized in to two major types based on their physical structure; (1) Planar CNTFET and (2) Coaxial CNTFET structures.

1.1.2.1 SB-CNTFET vs. MOSFET-like CNTFET

SB-CNTFET

SB-CNTFET is CNTFET where metal source/drain contacts are directly connected to the gate controlled nanotube channel as shown in Figure 1.2 (a) [14]. The work function difference, greater than zero, between metal and channel CNT creates potential barrier called Schottky Barrier (SB). The conductivity of SB-CNTFET is governed by the majority carriers tunneling through the SBs at the end contacts. The on-current and thereby device performance of SB-CNTFET is determined by the contact resistance due to the presence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance as shown on Figure 1.2 (b) [15].

SB-CNTFET shows ambipolar transport behavior. Ambipolar transport means the device operates both as n-type and p-type carriers depending on the polarity of gate bias, V_{gs}, (n-type for positive V_{gs} and p-type for negative V_{gs}). This property of SB-CNTFET worsens their on-current to off-current ratio and, hence, their application in conventional digital application. But the ambipolar characteristic is now explored to build new logic architectures that are different from conventional CMOS logic. This direction can create a new logic family based on SB-CNTFETs [16].

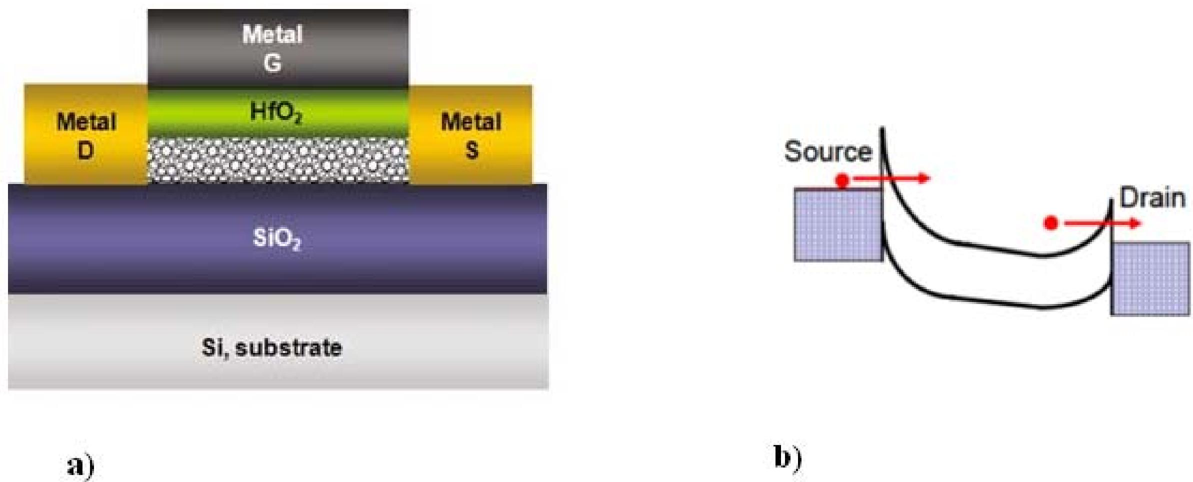


Figure 1.2 a) The structure of SB-CNTFET [14], b) Tunneling of electron from source and to drain through potential barrier called Schottky Barrier (SB) [15].

MOSFET-like CNTFET

Unlike SB-CNTFET, MOSFET-like CNTFET exhibits unipolar behavior by suppressing either electron (for p-type) or hole (for n-type) transport with heavily doped source/drain. The structure of MOSFET-like CNTFET is composed of two un-gated portions that are heavily (n^{++}/p^{++}) or lightly (n/p) doped as shown in Figure 1.3 (a) [17].

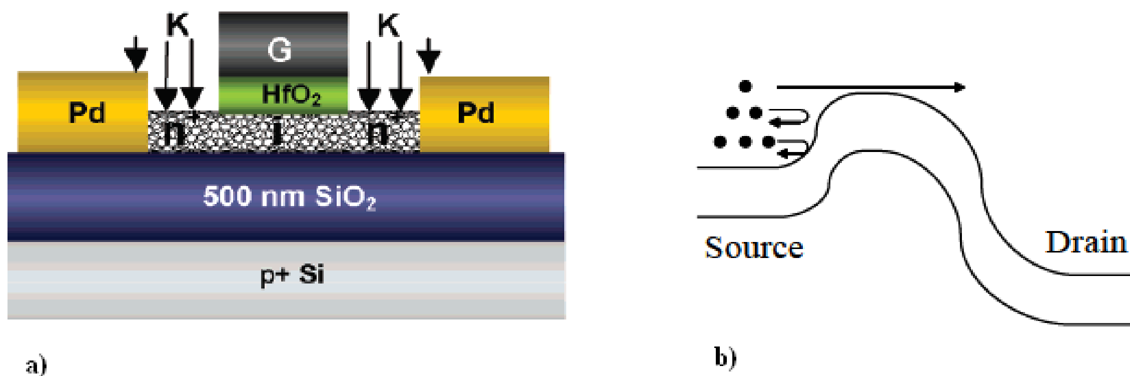


Figure 1.3 a) The structure of MOSFET-like CNTFET; ungated regions are doped with K (potassium) to form n-type CNTFET [17], b) Operation mechanism of MOSFET-like CNTFET [15]

The non-tunneling potential barrier, as shown in Figure 1.3 (b), in the channel region and thereby the conductivity is modulated by the gate-source bias. The on-current is limited by the amount of charges that can be induced in the channel by the gate. Also MOSFET-like CNTFETs will be more

scalable than SB-CNTFET. The focus of this thesis is on such kind of transistor and the detail of principle of operation is presented in chapter three.

1.1.2.2 Planar vs. Coaxial structure

Planar CNTFETs

Planar CNTFETs constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The nanotube and the metallic source/drain contacts are arranged on an insulated substrate, with either the nanotube being draped over the pre-patterned contacts, or with the contacts being patterned over the nanotube. The gate electrode can be on the back side of the insulated (with SiO_2) substrate (heavily doped), or alternatively is patterned on top of high dielectric insulated (ZrO_2, HfO_2) nanotube.

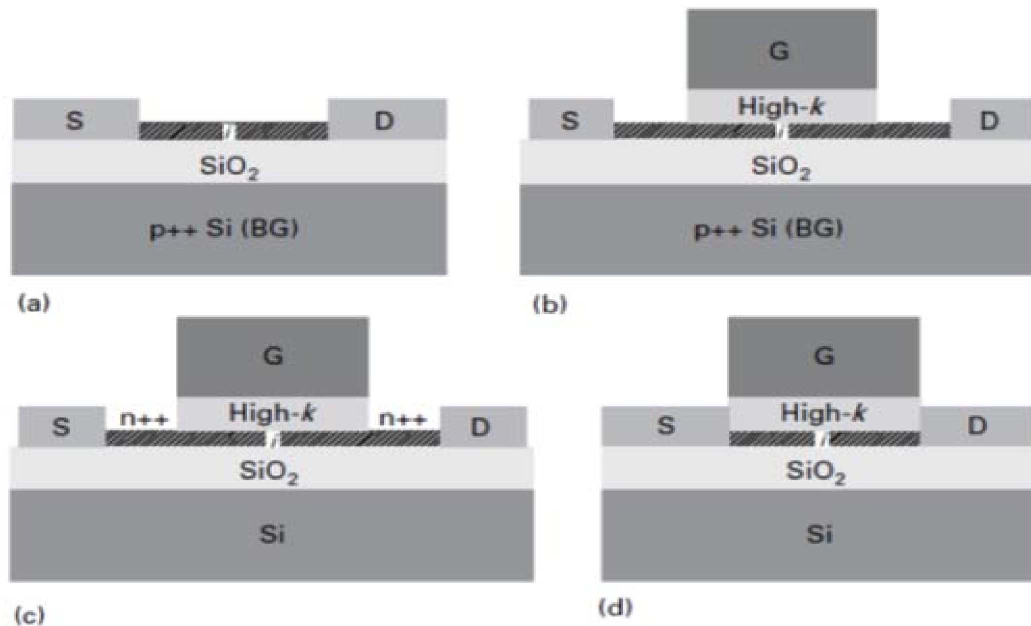


Figure 1.4 shows different planar structures of CNTFET (a) A back-gated CNTFET with the heavily doped Si substrate serving as the gate). (b) CNTFET featuring both a top-gate and a back-gate. The top-gate is used to control the channel and the back-gate is used to (electrostatically) dope the CNT extension regions to achieve a low-resistance path to the S/D contacts. (c) A CNTFET with chemically doped nanotube extension regions. (d) Top gated CNTFET with no deliberate extension for doping. Note that “i” represents an intrinsic semiconducting CNT [18].

Figure 1.4 shows different planar structures of CNTFET [18]. Figure 1.4(a) show the structure of the first CNTFET demonstrated [12]. It shows back-gated CNTFET with the heavily doped Si

substrate serving as the gate (p++ refers to heavy hole doping). However, a top-gate is preferred over a back-gate to provide localized and greater control of the nanotube channel, as well as to afford individual gate control in a multi-transistor circuit [18]. Figure 1.4(b) shows the CNTFET featuring both a top-gate and a back-gate. The top-gate is used to control the channel and the back-gate is used to (electrostatically) dope the CNT extension regions to achieve a low-resistance path to the Source/Drain contacts. Figure 1.4(c) shows the top-gated CNTFET with source and drain extensions doped chemically. Figure 1.4(d) shows the top-gated CNTFET with no deliberate extensions. CNTFETs shown on Figure 1.4(a) and Figure 1.4(d) are Schottky barrier CNTFETs and that are shown on Figure 1.4(b) and Figure 1.4(c) are MOSFET-like CNTFETs.

Coaxial CNTFET structure

Coaxial CNTFET structure is a further improvement upon the top-gate device geometry as shown in Figure 1-0.5 [19]. This kind of structure is also called wrap-around gate CNTFET or gate-all-around CNTFET. In this kind of structure, instead of gating just the part of the CNT that is closer to the metal gate contact as in planar structure, the entire circumference of the nanotube is gated. This maximize capacitive coupling between the gate electrode and the nanotube channel. Hence, it increases the control of channel conductance and improves the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.

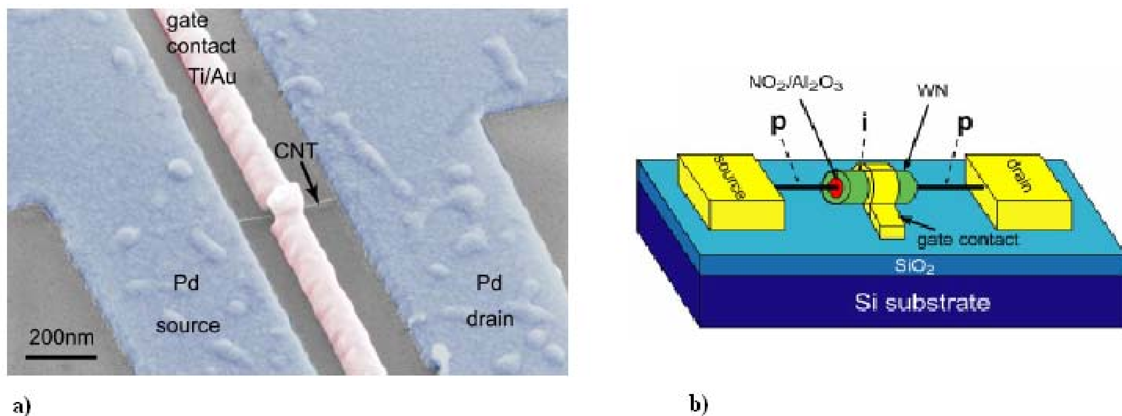


Figure 1.5 a) Scanning Electronic Microscope (SEM) image of a p/i/p Gate all around (GAA)-CNTFET located on a heavily p-doped Si substrate with 100 nm SiO_2. b) Illustrations of actual device shown in a) with more visible cross section [19].

1.1.3 Modeling in VHDL-AMS

VHDL-AMS stands for Very High Scale Integrated Circuit Hardware Description Language - Analog and Mixed Signal. It is a hardware description language (HDL), which has been approved as the new IEEE 1076.1 standard in March 1999 [20]. It is the only (to the best of my knowledge) IEEE-standardized hardware description language for analog and mixed signal systems. The following are features of VHDL-AMS that makes it suitable for development of models of semiconductor devices:

- It is IEEE-standardized which allows model portability.
- It allows multi-level modeling, i.e. different levels of abstraction of model behavior. For example, it allows modeling of Processors and also allows modeling of transistors. In addition, it allows implementation of complex algorithms and also allows implementation of simple equations.
- In addition, it is suitable for multi-domain modeling such as electrical, thermal, electromagnetic, mechanical, radiant and fluidic domains.
- Finally it allows mixed-signal modeling supporting analog and digital modeling.

Modeling of semiconductor devices may not require all features described above. However, these features of VHDL-AMS allow models of semiconductor devices to be integrated into systems that require all or parts of those features [21].

1.2 Problem statement

The problem addressed in this thesis is to develop fully analytical MOSFET-like CNTFET model, which take into consideration scattering effects and source/drain extension resistance effects, and implement into VHDL-AMS. The first part of the problem is to derive a model equation for the MOSFET-like CNTFET. A detailed study of electronic property of Carbon Nanotubes was undertaken for this purpose. The later part of the problem is implementing the derived model equations into VHDL-AMS and making it functional, for instance, for constructions of different electronic circuits.

1.3 Objectives

The objectives of this study are to achieve the following specific objectives.

1. To understand the electronic properties of carbon nanotubes which are necessary to model and investigate the performance of CNTFET.
2. To model the I-V characteristics of CNTFET.
3. To implement and evaluate the model performance in VHDL-AMS

1.4 Scopes of the study

Based on available resources and limited time frame this thesis is limited to the following scope of work:

1. Studying the basic electronic properties of single walled carbon nanotubes and applying the concept into MOSFET- like CNTFET modeling.
2. Implementing the model equations into VHDL-AMS and simulating the I-V characteristics.
3. Investigating the dependency of the performance of CNTFET on different parameters such as channel length, CNT diameter, thickness of insulator and temperature.
4. Constructing simple digital and analog circuits using the model.

1.5 Significance of the study

The final outcome of this study is fully analytical MOSFET-like CNTFET model in VHDL-AMS. The model costs small CPU time and suitable for constructing circuits with more transistors. Hence, it can be used to see the performance of these transistors with more complex circuits.

The thesis is presented in logical order, first basics of CNT, then CNTFET and its modeling, which makes it easier to understand for novice. Also the way the model is implemented into VHDL-AMS is more general and can be extended to other models.

1.6 Outline of Thesis Organization

The thesis has five chapters. In chapter one, this chapter, questions like 'why carbon nanotube based electronics got attention?' and 'why modeling in VHDL-AMS?' are tried to be answered. Different types of CNTFETs based on principle of operation and based on their structure are introduced. The

objective of the thesis is also defined in this chapter. Chapter two describes the basics of carbon nanotubes. Starting with its basic structure, its electronic property is detailed. It is just a foundation for taking any action toward CNTs. An integrated model for MOSFET-like CNTFET which is non-iterative, small CPU time cost and VHDL-AMS compatible is presented in chapter three. It started with principle of operation of MOSFET-like CNTFET, and then the concept quantum capacitance is defined and used to calculate channel potential. And the chain goes to calculation of drain to source current. In doing so electron phonon scattering effects (both acoustic and optical scattering) are considered. The leakage current due to band to band tunneling and source/drain doped region resistance effects are also added here in this chapter. In Chapter four the model equations developed in chapter three are used to implement with VHDL-AMS. Using the model, by varying different parameters we see the effects of those parameters on the transistor performance and finally circuits are constructed, simulated and analyzed to validate the model. Chapter five concludes the work and recommend what will be done in future.

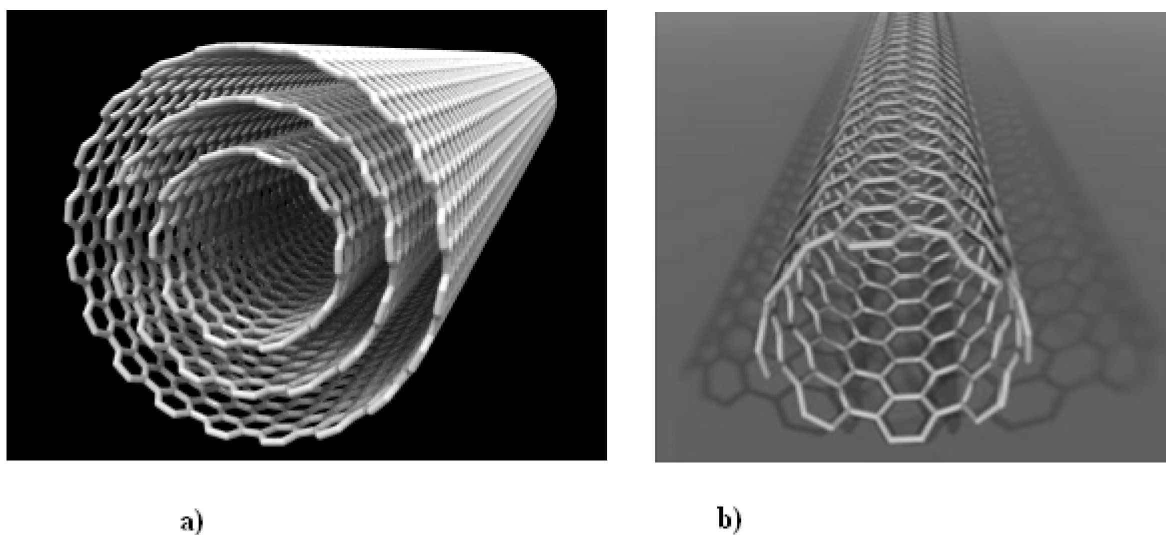
CHAPTER 2

BASICS OF CARBON NANOTUBES

In this chapter the basics of carbon nanotubes that are necessary to understand the operation of carbon nanotube transistor are discussed in detail.

2.1 Carbon nanotube Structure

Carbon nanotubes are sheets of graphite rolled in the shape of the tube [22]. If the graphite is of only single layer (in which case it is called graphene) the carbon nanotube formed is single walled carbon nanotube (SWCNT) and if the graphite is of two or more layers the carbon nanotube formed is multi walled carbon nanotube (MWCNT). Figure 2.1(a) shows MWCNT of three walls and Figure 2.1(b) shows the SWCNT. In this thesis SWCNT is only our main concern.



a) b)

Figure 2.1 Carbon nanotubes: a) Multiwalled carbon nanotubes (MWCNT) and b) Single-walled carbon nanotubes (SWCNT [22]

Given the sheet of graphene, as shown in Figure 2.2, SWCNT (or simply CNTs here after) can be cut in different directions called chirality or some times called helicity. Chirality is expressed by the chiral vector; $\vec{C}_h$ which is expressed by two primitive vectors $\vec{a}_1$,$\vec{a}_2$ and mathematically given by,

$$\vec{C}_h = n\vec{a}_1 + m\vec{a}_2 \qquad 2.1$$

where n and m are intergers; and $0 \leq |m| \leq n$).

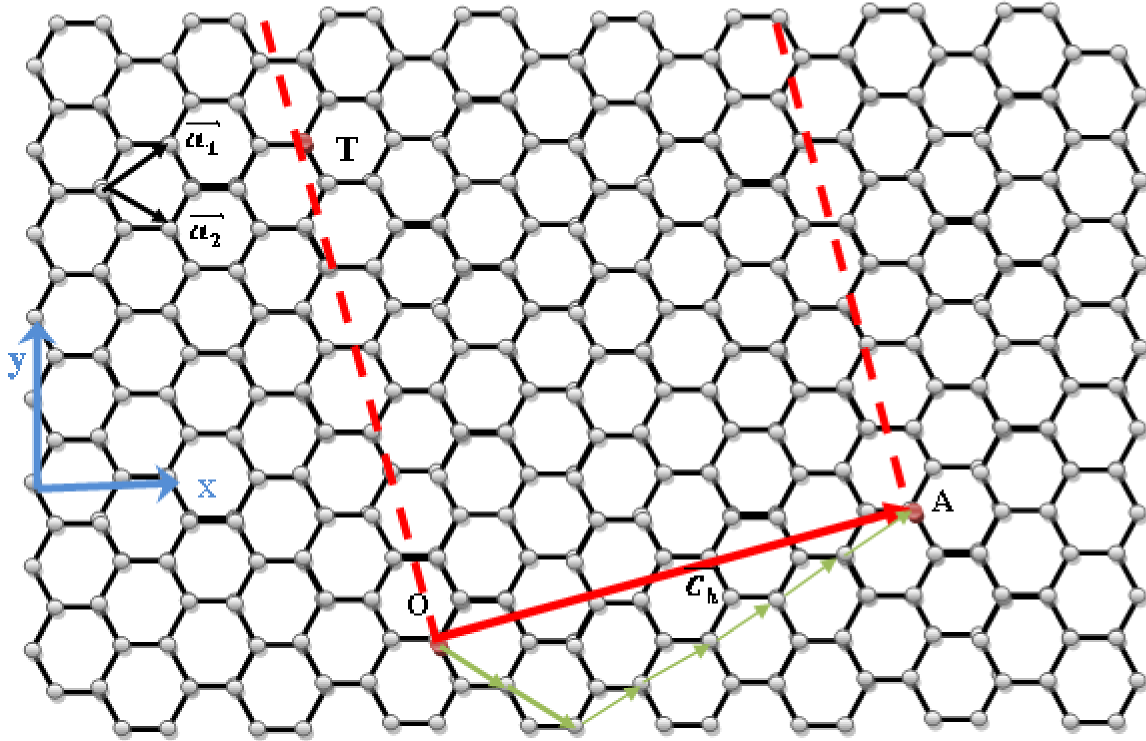


Figure 2.2 Two dimensional hexagonal lattice of carbon where the primitive vectors are indicated by $\vec{a_1}$ and $\vec{a_2}$. A CNT is conceptually formed by cutting the lattice along the vectors OT and OA and connecting point O and A by rolling it into a seamless cylinder. The length of vector $\vec{C_h}$ defines the circumference of the CNT formed.

The specific chiral vector shown in Figure 2.2 is $\vec{C}_h$ = (5, 2). A CNT is conceptually formed by cutting the lattice along the vectors OT and OA and connecting point O and A by rolling it into a seamless cylinder [22]. The length of vector $\overrightarrow{C_h}$ defines the circumference of the CNT formed. The diameter of the CNT formed is found from the circumference as follows

$$D_{CNT} = |\overrightarrow{C_h}|/_{\pi} = \frac{a\sqrt{n^2 + m^2 + n * m}}{\pi} \quad (2.2)$$

Where a=$|\overrightarrow{a_1}| = |\overrightarrow{a_2}|$ =0.249 nm is lattice constant (the distance between crystallographically equivalent atoms).

The chirality also gives us a basis for dividing the tubes into three different classes. A carbon nanotube described by (n, m) can be classified as shown in Figure 2.3 [23]:

- Zigzag if m = 0
- Armchair if n = m

- Chiral if $n \neq m$

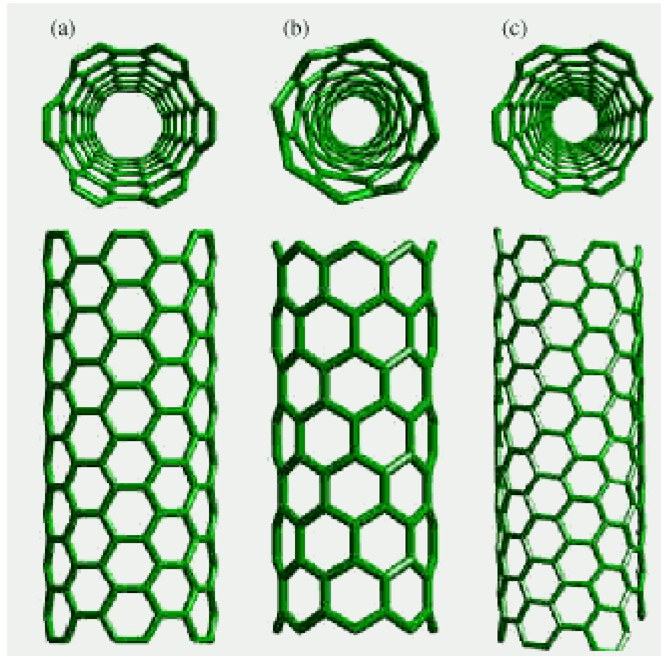


Figure 2.3 The three types of CNTs [23] a) Zigzag b) Armchair c) Chiral

2.2 Basic electronic properties of Carbon nanotubes

As stated earlier the CNT can be conceptually viewed as a rolled-up graphene sheet to seamless tube. And a simple way to study the electronic properties of CNT is to start with that of graphene's electronic property. The lattice structure of graphene in real space consists of hexagonal arrangement of carbon atoms as shown in Figure 2.4(a) [14]. Isolated carbon atoms have four valence electrons in 2s, $2p_x$, $2p_y$, and $2p_z$ atomic orbitals. As carbon atoms form graphene, three atomic orbitals, 2s, $2p_x$, and $2p_y$, are hybridized into three sp^2 orbitals in the same plane while the $2p_z$ orbital remains perpendicular to other orbitals. The hybridized orbitals are responsible for σ bonds between the adjacent carbon atoms and the $2p_z$ orbital results in π bonds out of the plane of graphene as shown in Figure 2.4(b) [24].

Generally, electrical transport properties are determined by the electrons (holes) near the Fermi level, since only these electrons (holes) have easy access to the unoccupied (occupied) states. In graphene, the π orbitals, which lie near the Fermi level as shown in Figure 2.4 (c) [24], are responsible for the electrical transport properties by forming delocalized states. The band structure

of graphene derived from π orbitals can be calculated by the tight-binding approximations [18] to be:

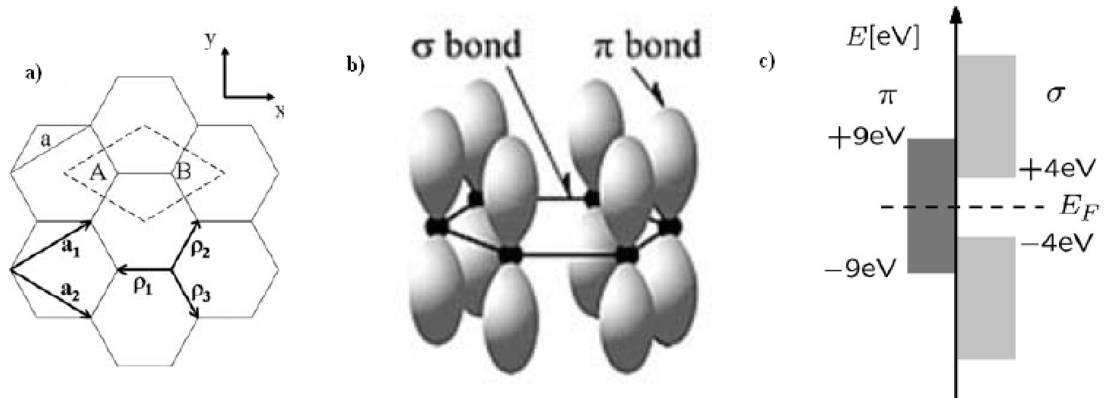


Figure 2.4 a) Real space representation of a graphene lattice; a unit cell is shown as a dashed rhombus with two carbon atoms (A and B). Vectors ρ_j connect nearest neighbor carbon atoms. [14] b) sp^2 hybridization in graphene; σ bonds, π bonds [24] c) Energies of σ bonds and π bonds with respect to Fermi level [24].

$$E(\boldsymbol{k}) = \pm V_\pi \sqrt{1 + 4\cos\left(\frac{\sqrt{3}a}{2}k_x\right)\cos\left(\frac{a}{2}k_y\right) + 4\left(\cos\left(\frac{a}{2}k_y\right)\right)^2} \tag{2.4}$$

Where V_π is carbon to carbon interaction energy. Its value varies between 2.7 eV to 3.3 eV. For routine calculations, the extracted value $V_\pi \approx 3.1$ eV from experimental measurements is commonly used. 'a=0.249 nm' is lattice constant. $k = k_x\hat{\imath} + k_y\hat{\jmath}$ is wave number. k_x and k_y are its component in x and y directions respectively. The E-k plot for graphene is shown in Figure 2.5.

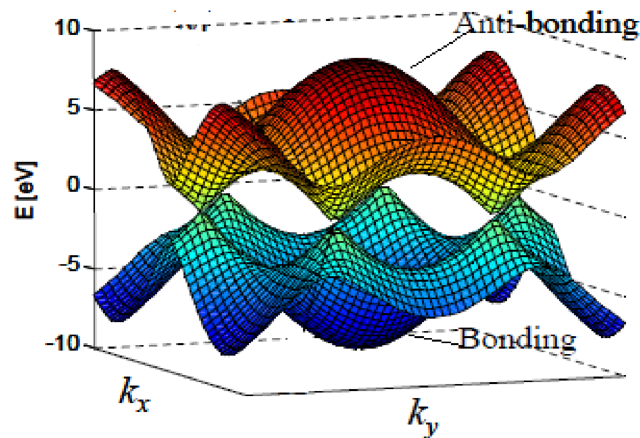


Figure 2.5 E-k dispersion relations for graphene from equation (2.4)

2.2.1 E-k dispersion relation of Carbon nanotube

Due to the small diameter of CNT, the quantization of wave vector in the circumferential direction occurs. A general analytic E-k dispersion relation for CNT is obtained by applying periodic boundary conditions in the circumferential direction to the 2-D graphene sheet E-k dispersion relation. Analytically, the dispersion of CNT is given by the formula [22]

$$E(k_l, p) = \pm V_\pi \sqrt{1 + 4\cos t_1 \cos t_2 + 4\cos t_2 \cos t_2} \quad (2.5)$$

Where k_l is the wavenumber along the length of CNT or in direction of transport and p is quantization number in the circumferential direction. And other parameters are

$$t_1 = \frac{\sqrt{3}}{4} a \frac{m-n}{\sqrt{n^2+m^2+nm}} k_l + \frac{\pi}{2} \frac{n+3m}{n^2+m^2+nm} p \quad (2.6)$$

$$t_2 = \frac{\sqrt{3}}{4} a \frac{m+n}{\sqrt{n^2+m^2+nm}} k_l + \frac{\pi}{2} \frac{3n-m}{n^2+m^2+nm} p \quad (2.7)$$

To distinguish between the metal and semiconducting CNT, a simple rule has been established:

- If n - m is divisible by 3 then the CNT is metallic. This means when n-m is divisible by 3 substituting in equation (2.6) and (2.7) then in to equation (2.5) at k_l=0 and p=0 gives E (k_l, p) =0. This implies that there is no band gap.
- If n - m is not divisible by 3 then the CNT is a semiconductor.

Using equation (2.5), the complete E-k relation for semiconducting CNT with chirality of (19, 0) is shown in Figure 2.6 (a). From the figure it clear that there is band gab. In Figure 2.6 (b) the complete E-k relation for metallic CNT with chirality of (24, 0) is shown. At k_l=0 the lowest subband of conduction band and highest subband of valance band touch each other.

Around the Fermi point with carriers' energy satisfying the condition $|E(k_l, p)|/V_\pi < 1$, CNT E−k dispersion relation given in equation (2.5) can be approximated as [25], [26]

$$E(k_l, p) = \pm \frac{\sqrt{3}}{2} a V_\pi \sqrt{k_p^2 + k_l^2} \quad (2.8)$$

Where for metallic CNT (i.e. mod (n-m, 3) = 0) $k_p = \frac{2}{D_{CNT}} p;\ p = 0,1,2,\ldots$ and for semiconducting CNT (i.e. mod (n-m, 3) $\neq$ 0), $k_p = \frac{2}{D_{CNT}} \frac{6p-3-(-1)^p}{12};\ p = 1,2,3,\ldots$ Two different examples

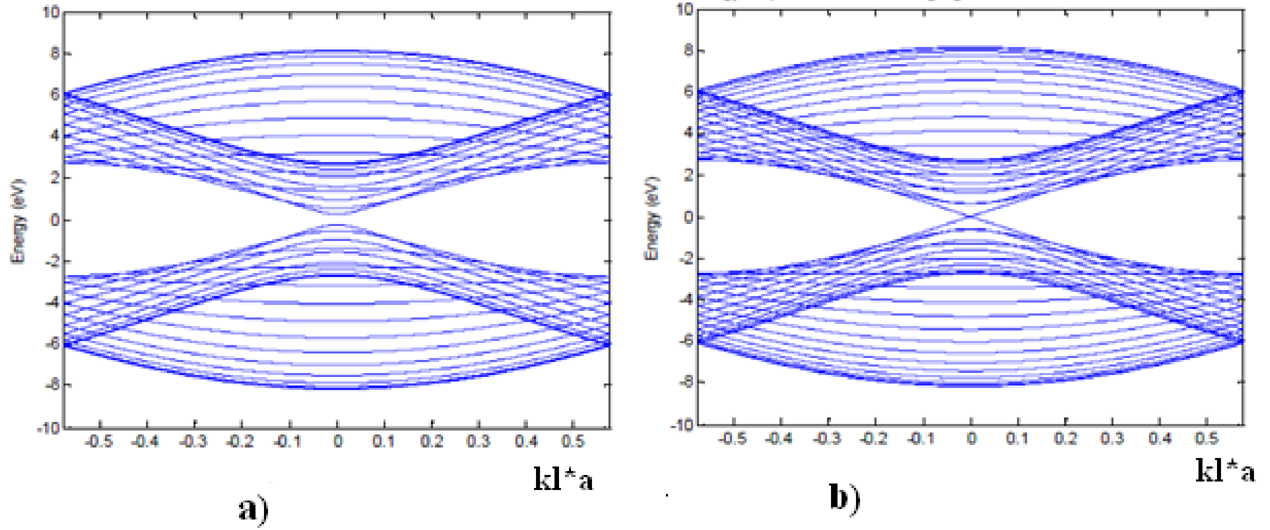


Figure 2.6 All possible energy bands a) for semiconducting CNT (19, 0) and b) for metallic CNT (24, 0)

implementing equation (2.8) are shown in Figure 2.7(a) and (b) representing a semiconducting and metallic CNT respectively.

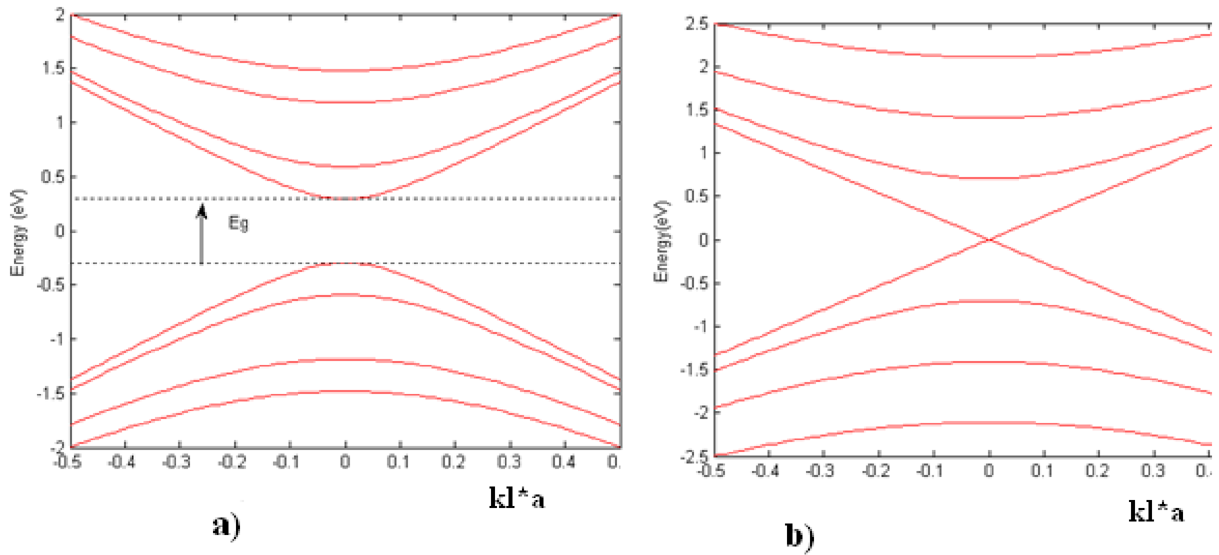


Figure 2.7 Energy bands near the Fermi level a) for semiconducting CNT (19, 0) b) for metallic CNT (24, 0)

From equation (2.8) lowest conduction sub-band for metallic CNT is $E(k_l = 0, p = 0) = 0$ and the lowest conduction sub-band for semiconducting CNT is $E(k_l = 0, p = 1) = \frac{\sqrt{3}}{2} aV_\pi k_1 = \frac{\sqrt{3}}{2} aV_\pi \times$

$\frac{2}{3D_{CNT}}$. Hence the band gap of semiconducting CNT is $E_g = 2 \times E(k_l = 0, p = 1)$. Substituting for constants, $V_\pi \approx 3.1$ eV and a=0.249 nm, band gap is derived to be:

$$E_g = \frac{0.89}{D_{CNT}} nm\ eV \tag{2.9}$$

Here diameter is in nm. From equation (2.9) we see that band gap is inversely proportional to diameter of nanotube.

2.2.2 Density of states (DOS)

The DOS tells us the number of available states per unit energy range or, in k-space, the number of allowed states per unit wave number (k) range and it clearly depends on the E-k relationship. In a 1-D solid, the number of states between E and E + dE is the differential wave vector dk normalized to the length of one state [27]:

$$D(E)dE\ L = 2\frac{dk_l}{2\pi/L} \tag{2.10}$$

Where L is the length of the 1-D system and 2π/L is the length of one k-state; the factor of 2 in the numerator accounts for spin degeneracy. From equation (2.10) general formula for the electron DOS in a 1-D solid can be derived as follows:

$$D(E)dE\ L = 2\frac{dk_l}{2\pi/L} = L * \frac{1}{\pi} * \frac{dk_l}{dE} dE$$

$$\Rightarrow D(E) = \frac{1}{\pi} * \frac{dk_l}{dE} = \frac{1}{\pi} * \left(\frac{dE}{dk_l}\right)^{-1} \tag{2.11}$$

Equation (2.11) is the general formula for DOS in a 1-D solid. For carbon nanotube to derive expression for DOS using equation (2.8) it is important first to define the term “degeneracy”. Degeneracy is defined as the case where a different set of quantum numbers results in the same energy [18]. The family of degeneracy include spin degeneracy, subband degeneracy, point degeneracy at the Fermi energy, and Brillouin zone mirror symmetry [18]. The detail of when and how to take these effects in to consideration is give in references [18, 25] and considering these effects equation (2.11) using equation (2.8) is evaluated to be

$$D(E) = \sum_{p=-\infty}^{\infty} \frac{D_0|E|}{\sqrt{E^2 - E(0,p)^2}} \text{ for } |E| > E(0,p) \text{and zero otherwise} \tag{2.12}$$

Where$D_0 = \frac{8}{\sqrt{3}\,\pi V_\pi a}$, $V_\pi = 3.1$ eV and a = 0.249 nm

Figure 2.8 shows the DOS for (19, 0) and (18, 0) CNT with similar diameter (~ 1.5 nm) using equation (2.12). From the Figure 2.8 it is shown that for metallic CNT, drawn in red color, there are allowable states for all energy range as expected but for Semiconducting CNT, drawn in blue color, from –E(0,1) to E(0, 1) DOS is zero due band gap.

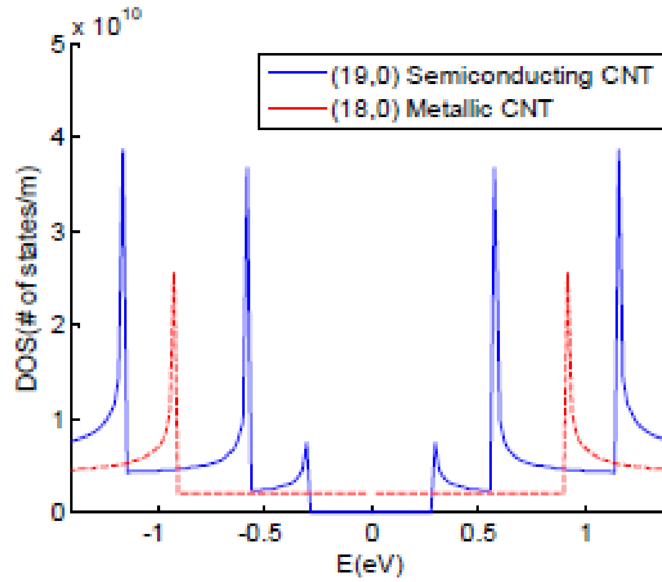


Figure 2.8 The density of states for (19, 0) semiconducting and (18, 0) metallic CNT, calculated using the Equation (2.12)

2.2.3 Carrier velocity

The carrier velocity tells us the speed of the electron/hole. It is associated with the maximum information (or signal) frequency that the electrons can transmit. Formally, the carrier velocity is defined as [28]

$$v(E) = \frac{2\pi}{h}\frac{\partial E}{\partial k_l} \tag{2.13}$$

Using equation (2.8) for $E(k_l, p)$ we obtain expression for v(E) as

$$v(k_l, p) = \frac{\pi}{h}\sqrt{3}\, a\, V_\pi \frac{k_l}{\sqrt{{k_p}^2 + {k_l}^2}}$$

$$\Rightarrow v(E(k_l, p)) = \frac{\pi}{h}\sqrt{3}\, a\, V_\pi \left(\frac{\sqrt{E^2 - E(0,p)^2}}{E}\right) \tag{2.14}$$

Note that the velocity at the bottom of subbands $(E(0, p))$, such as the lowest subbands $E(0,1)$, vanishes to zero. We can conclude that, owing to Heisenberg's uncertainty principle, which requires electron waves to have a finite speed or no electron is found in specific subbands and at specific substates with probability one, such states (with zero velocity) are not legitimate states. Electron with zero velocity means we can get that electron any time at particular state.

2.2.4 Effective mass

The effective mass, m_{eff} of an electron in a semiconductor is generally given by [29]

$$m_{eff}(E) = \frac{\hbar^2}{\partial^2 E / \partial {k_l}^2} \tag{2.15}$$

Using equation (2.8) for expression of energy, effective mass near the bottom of the sub-bands is given by:

$$m_{eff} = \frac{2\hbar^2 k_p}{\sqrt{3}\, a\, V_\pi} \tag{2.16}$$

2.2.5 Carriers density

The carriers (electrons or holes) density is a central property of semiconductors. It is the total number of occupied states in the subband. Here in this topic we focus on the electron carrier density and results apply equally well to holes due to the electron–hole symmetry in the CNT band structure. Electron carrier density is given to be:

$$n_{CNT} = \sum_{p=1}^{P} \left[\int_{E(0,p)}^{\infty} D(E) f(E, \mu_f) dE \right] \tag{2.17}$$

Where P is number of subband, $E(0, p)$is lowest energy of each pth subband, $D(E)$ is density of state given in equation (2.12), $f(E, \mu_f)$is Fermi Dirac distribution function and μ_f is Fermi level.

Equation (2.17) takes into consideration all subbands. But Fermi Dirac distribution function decays rapidly for higher energies as shown in Figure 2.9 [18]. Therefore, we can take only the first two subbands for lower bias application (sub 1 V) without lose of accuracy. Hence, equation (2.17) is rewritten as:

$$n_{CNT} = \sum_{p=1}^{2}\left[\int_{E(0,p)}^{\infty} D(E) f\left(E, \mu_f\right) dE\right] \tag{2.18}$$

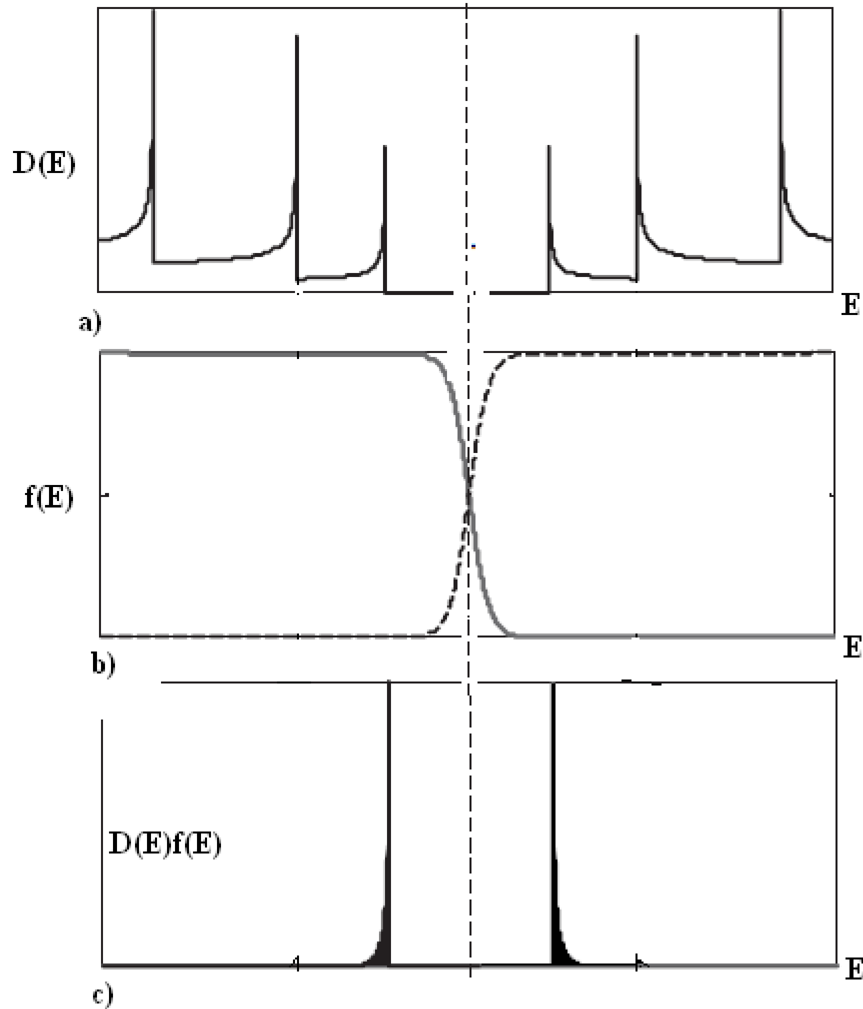


Figure 2.9 Illustrates contribution of first two subbands to carrier density relative to higher subbands (a) DOS (b) f (E) for electrons (solid) and holes (dashed). (c) DOS multiplied by the Fermi–Dirac function showing only the first subband contributes appreciably to carrier density at equilibrium [18].

CHAPTER 3

MODELING MOSFET-LIKE CNTFET TRANSISTOR

3.1 Introduction

In the previous chapter, the electronic structure of the Carbon nanotube is reviewed to sufficient detail. Efforts have been made in recent years on modeling CNTFET for understanding device operation in digital logic and analog circuit application [30, 31]. Early CNTFET models simply used self-consistent numerical iterations and integration [30] which is not good for circuit level designs. Circuit-level models have been developed based numerical approximation [31], [32] but they didn't consider the effect of source/drain region resistance. A compact model has been developed which considered scattering effects and source/drain region resistance effects but resort to SPICE simulator to solve iterative differential equations to compute the channel potential [33].

Here in this chapter, we propose an integrated model for MOSFET-like CNTFET which is non-iterative, costs small CPU time, and VHDL-AMS compatible. The physical structure of n-type MOSFET-like CNTFET is shown in Figure 3.1. The basic structure is similar to a conventional n-type MOSFET with the channel replaced by a semiconducting CNT. The portion of semiconducting

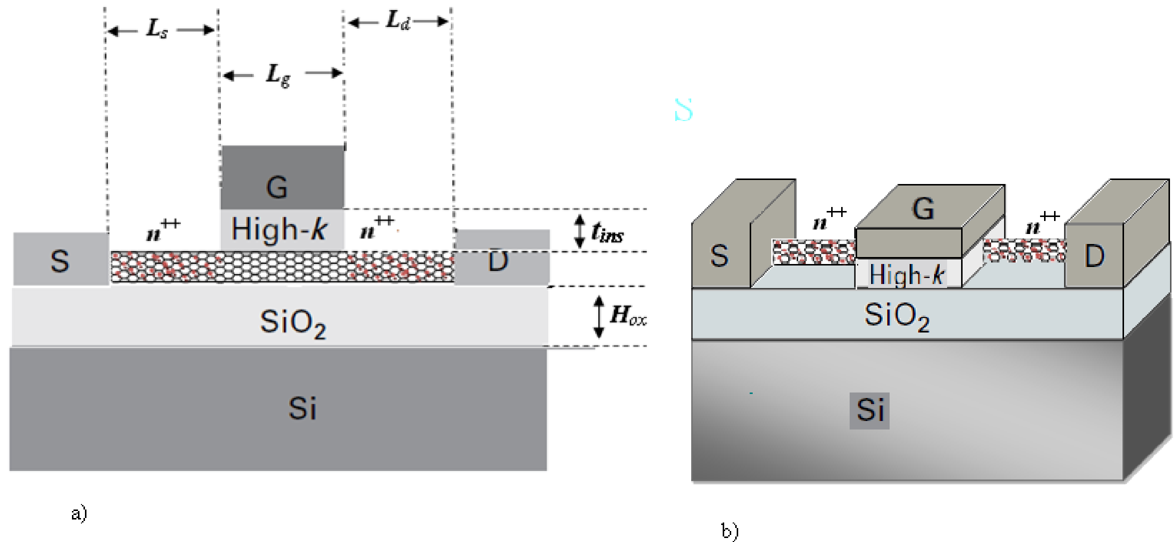


Figure 3.1 A physical diagram of a MOSFET-like CNTFET a) Shows necessary physical dimensions to be used in modeling. b) Shows the simple 3D visualization. Where Ls is length of doped CNT in source side, L_d is length of doped CNT in drain side, L_g is length of channel covered by gate t_{ins} is thickness of insulator between gate and channel and H_{ox} is the height of SiO_2 between channel and substrate.

CNT under gated region is defined by the gate length (L_g), the highly doped (n^{++} for n-type or p^{++} for p-type) ungated portions on the side of source and drain are defined by source length (L_s) and drain length (L_d), respectively. The thickness of insulating material between gate and channel is defined by t_{ins} with dielectric constant k_1 and the thickness of insulating material (usually SiO_2) between channel and substrate is H_{ox} with dielectric constant k_2.

3.2 Principle of operation

In MOSFET-like CNTFET the function of the gate bias, V_{gs}, is to modulate the top of the energy

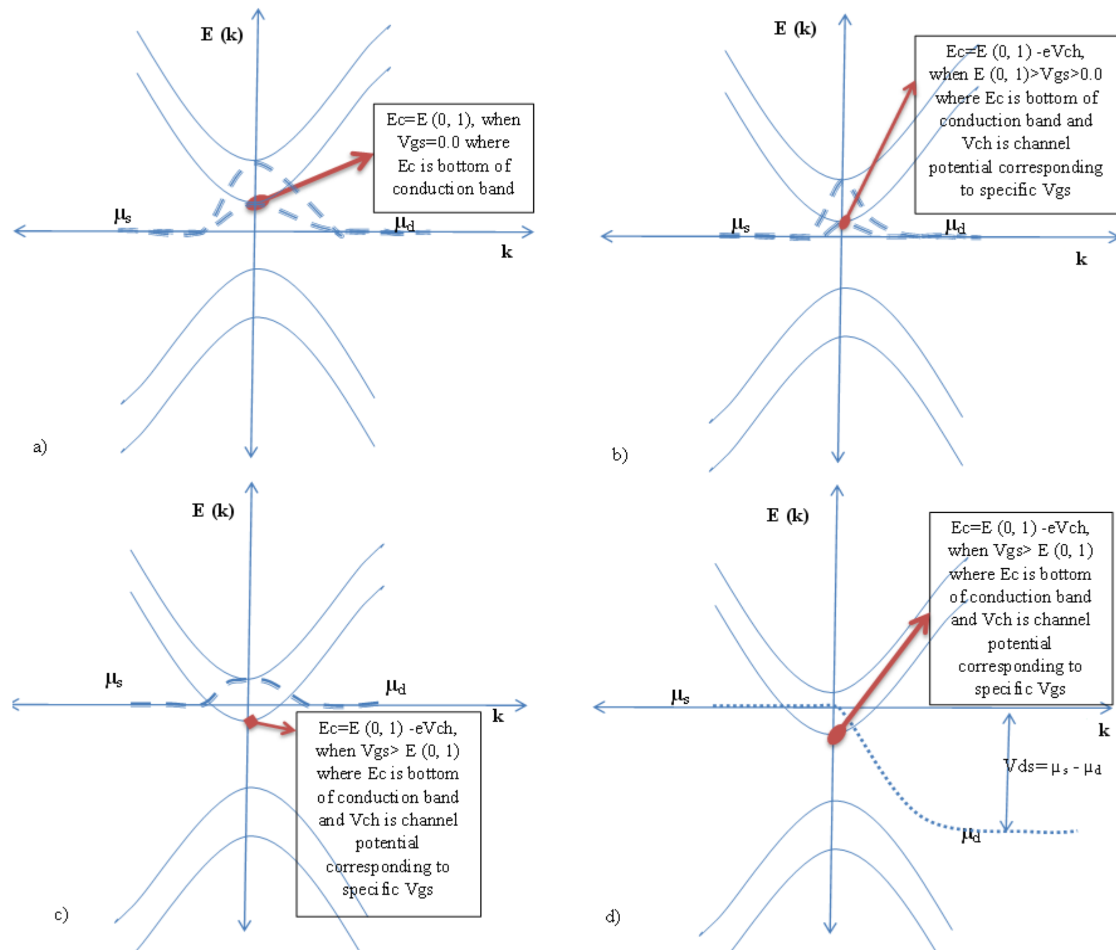


Figure 3.2 Shows the principle of operation of MOSFET-like-CNTFET. A positive voltage V_{gs} applied to the gate moves the E (0, 1) downwards by V_{ch}. a) shows the case when Vgs=0 and $\mu_s = \mu_d$. b) Shows the case when 0<Vgs<E (0, 1) and $\mu_s = \mu_d$. c) Shows the case when Vgs>E (0, 1) and $\mu_s = \mu_d$. And d) shows the case when Vgs>E (0, 1) and $\mu_s - \mu_d = V_{ds}$.

barrier. We assume that the application of the gate bias moves the whole band profile up or down invariably by channel potential, V_{ch}. The channel potential, V_{ch}, is the local electrostatic potential

that accounts for the excess charge induced in the channel due to an external electric field [18]. The Figure 3.2 illustrates the principle as follows.

Note that in Figure 3.2 (a), (b), and (c) the source Fermi level and drain Fermi level are equal ($\mu s= \mu_d$) which means equilibrium, no net flow of charges from right to left or vice versa. In Figure 3.2 (a) there is no applied gate voltage and the barrier (shown in broken line) is not moved up or down and hence there is no or very few injection of charges, since there is no available state that touches or cross Fermi level. In Figure 3.2 (b) with applied V_{gs}, the barrier is moved down by V_{ch}. But V_{gs} is not enough voltage to give V_{ch} that bring minimum of conduction band (E_c), top of barrier, below Fermi level and, hence, still there is no or very low injection of charges in to channel. When E_c is brought below Fermi level, as shown in Figure 3.2 (c), there will be available states for injection of charges. However, the device is still in equilibrium since there is no directing electric field along the channel (from drain to source) for motion of charges that will result in current. In Figure 3.2 (d) there is enough, V_{gs}, that bring E_c below Fermi level and also there is potential between drain and source, V_{ds}, resulting in electric field along the channel that will result in current. Therefore, from the figure we see that, qualitatively, for this transistor to conduct electric current there must be enough applied voltage to gate and also to drain. The magnitude of current depends on channel potential, V_{ch}, which correspond to particular gate voltage, V_{gs}, and also depends on drain to source potential, V_{ds}. To see quantitatively the dependence of current on V_{gs} or V_{ds}, the precise dependence of channel potential on gate voltage has to be calculated.

3.3 Channel potential calculation

We see from Figure 3.2 that when V_{gs} increases V_{ch} also increases but what is their relationship quantitatively? This is answered based on Figure 3.3. Figure 3.3 (a) shows a conventional MOS capacitor like in MOSFET. MOS capacitor is formed when source and drain are grounded to study the effect of gate bias voltage. In the Figure 3.3 (a) if the channel is insulator, then the node (V_{ch}) is completely disconnected from ground and V_{ch} is equal to V_{gs}. But if the channel is conductor then it behaves like the negative plate of a parallel plate capacitor, so that the channel potential V_{ch} is connected to ground. What is not obvious is the case in intermediate situations when the channel is neither an insulator nor a conductor i.e. when channel is semiconducting like semiconducting CNTs. Now in this situation conductivity of the channel depends on the number of carriers in channel. This in turn depends on how far subband is lowered so that there are available states near

Fermi level which is function of V_{ch}. Therefore, V_{ch} depends on number of carriers in channel and in turn the number of carriers depends on V_{ch} and they are related by recently introduced quantity called quantum capacitance [34] which is likely term to relate charge and voltage (channel).

Unlike electrostatic capacitance which depends on physical geometry, quantum capacitance depends on number of available states in the channel which is discrete number hence the name 'quantum capacitance' and it is given by the change of channel charge carriers, Q_{CNT}, with respect to change of channel potential, V_{ch}:

$$C_q(V_{ch}) = \frac{\partial Q_{CNT}}{\partial V_{ch}} \tag{3.1}$$

Where C_q is quantum capacitance per unit length which is function of channel potential, Q_{CNT} is charge carrier per unit length in channel and V_{ch} is channel potential.

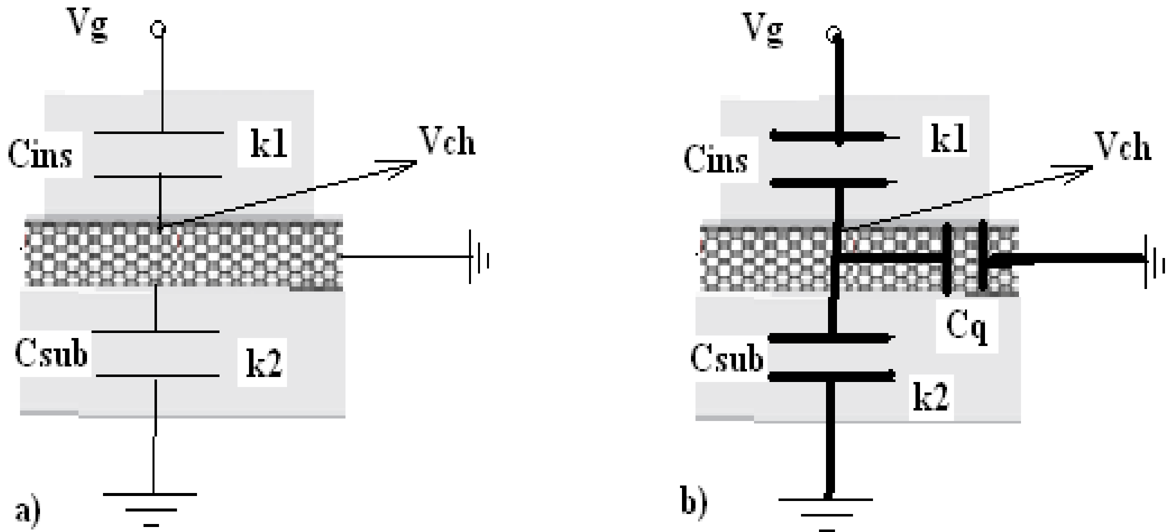


Figure 3.3 Equivalent circuit representation of the MOS capacitor showing Electrostatic capacitances and quantum capacitance a) conventional MOS capacitor b) equivalent circuit of MOS capacitor of CNTFET containing quantum capacitor in addition to geometrical capacitors.

Q_{CNT} is in turn given by:

$$Q_{CNT} = \int_{0}^{+\infty} \frac{D(E)}{2} \times [f(E - V_{ch} - \mu_s) + f(E - V_{ch} - \mu_d)]dE \tag{3.2}$$

Where D (E) is density of state given in equation (2.12), f (E) is Fermi-Dirac distribution function given by $f(E) = 1/(1 + e^{\frac{E}{KB \times T}})$, μ_s is source Fermi level and μ_d is drain Fermi level. Using equation (3.1) and (3.2) C_q is approximated to be [18]:

$$C_q(V_{ch}) = \sum_{p=1}^{P} \frac{2e^2 N_0(p) e^{\frac{eV_{ch} - E(0,p)}{K_B T}}}{K_B T \left(1 + 0.63 e^{\frac{eV_{ch} - E(0,p)}{K_B T}}\right)^2} \tag{3.3}$$

Where T is temperature in Kelvin, K_B is Boltzmann constant, E (0, p) is lowest energy of pth subband calculated from equation (2.8) and N_0 (p) is effective density of state of pth subband given by:

$$N_0(p) = \frac{8}{a} \frac{E(0,p) + 2K_B T}{E(0,p) + 8V_\pi} \sqrt{\frac{2K_B T}{3\pi E(0,p)}} \tag{3.4}$$

Where $V_\pi \approx 3.1$ eV carbon to carbon interacting energy in CNT crystal lattice and a=0.249 nm is lattice constant. From Figure 0.3 (b) by using voltage division rule we can calculate V_{ch} in terms of V_{gs} to be:

$$V_{ch} = \frac{C_{ins}}{C_{ins} + C_{sub} + C_q(V_{ch})} V_{gs} \tag{3.5}$$

Usually thickness of insulator, SiO_2, between channel and substrate is big and dielectric constant is small which implies that C_{sub} is low when compared to C_{ins} and C_q and we can modify to:

$$V_{ch} = \frac{C_{ins}}{C_{ins} + C_q(V_{ch})} V_{gs} \tag{3.6}$$

From equation (3.6) we see that for $C_{ins} >> C_Q$, $V_{ch} \approx V_{gs}$ which could be achieved if we use materials with high dielectric constant. Hence substituting equation (3.3) in to (3.6) we can obtain channel potential.

3.4 Drain to Source Current (I_{ds})

We consider two current sources in the MOSFET-like CNTFET model: (1) the thermionic current contributed by the semiconducting sub-bands (I_{thermo}) and (2) the leakage current (I_{btbt}) caused by the band to band tunneling mechanism through the semiconducting sub-bands.

3.4.1 Thermionic current (I_{thermo})

We only consider the electron-current for the n-type MOSFET-like CNTFET because the hole current is suppressed by the n-type heavily doped source/drain, and is negligible compared to current contributed by electron in conduction band. The method is first to calculate the current due to electrons coming from the left (source side) and then to add that due to electrons arriving from the right (drain side). The expressions for these are similar except for the Fermi levels and directions.

The current due to electrons from the left is given by

$$I_s = 2e\int_0^{\infty} f(E(k_l),\mu_s)v(k_l)T(k_l)\frac{dk_l}{2\pi} \tag{3.7}$$

Where the factor of 2 in front accounts for the two spins. The Fermi function $f\big(E(k_l),\mu_s\big)$ gives the probability that each state is occupied, governed by the Fermi level μ_s of the left lead (source). The factor of velocity $v(k_l)$ turns the charge density into a current density. The transmission coefficient $T(k_l)$ gives the probability that an electron passes from left to right without scattering and contributes to the current. If it is reflected it leaves the system to the left and makes no contribution. Finally, the integral is restricted to positive values of k_l because we include only electrons coming from the left, source side, and move to right, with positive velocity.

Integration over energy is simpler and usual rather than wave number and we can do by changing the variable of integration and using

$$dk_l = \frac{dk_l}{dE(k_l)}dE(k_l) = \frac{2\pi}{hv(k_l)}dE(k_l) \tag{3.8}$$

And from Figure 3.2 in presence of gate bias we can obtain the limits of integration as: when $\mathrm{k_l} = 0$ for the $\mathrm{p^{th}}$ subband, $\mathrm{E(k_l) = E(0, p) - eV_{ch}}$ and when $\mathrm{k_l} \Rightarrow \infty$ then $\mathrm{E(k_l)} \Rightarrow \infty$. Therefore, substituting equation (3.8) into equation (3.7) we get

$$I_s = 2e \sum_{p=1}^{\boldsymbol{P}} \left(\int_{E(0,p)-eV_{ch}}^{\infty} f(E, \mu_s) v(E) T(E) \frac{dE}{hv(E)} \right)$$

$$\Rightarrow I_s = 2e \sum_{p=1}^{\boldsymbol{P}} \left(\int_{E(0,p)-eV_{ch}}^{\infty} f(E, \mu_s) T(E) \frac{dE}{h} \right) \tag{3.9}$$

Where P is the number of all subbands. As stated in section 2.2.5 only the first two subbands have visible impact on-current calculation for sub 1 V bias voltage. Therefore, the value of P here after is $\mathrm{P} = 2$ but kept as it is to make formula more general.

The expression for the current due to electrons coming from the right (drain) to left (source) is identical. The only differences are the sign, as the electrons are travelling in the opposite direction.

$$I_d = -\frac{2e}{h} \sum_{p=1}^{P} \left(\int_{E(0,p)-eV_{ch}}^{\infty} f(E, \mu_d) T(E) dE \right) \tag{3.10}$$

The net current is the sum of drain and source current:

$$I_{thermo} = I_s + I_d = \frac{4e}{h} \sum_{p=1}^{P} \left(\int_{E(0,p)-eV_{ch}}^{\infty} \big(f(E, \mu_s) - f(E, \mu_d)\big) T(E) dE \right) \tag{3.11}$$

If the transport is of fully ballistic, the transmission coefficient, T(E), is unity and equation (3.11) modified to:

$$I_{thermo,ballistic} = \frac{4e}{h} \sum_{p=1}^{\boldsymbol{P}} \left(\int_{E(0,p)-eV_{ch}}^{\infty} \big(f(E, \mu_s) - f(E, \mu_d)\big) dE \right) \tag{3.12}$$

Equation (3.12) is evaluated to be:

$$I_{thermo,ballistic} = \frac{4ek_BT}{h}\sum_{p=1}^{P}\left[ln\left(1+e^{\frac{eV_{ch}-\mu_s-E(0,p)}{k_BT}}\right)-ln\left(1+e^{\frac{eV_{ch}-\mu_d-E(0,p)}{k_BT}}\right)\right] \quad (3.13)$$

In reality transport is not fully ballistic due to various sources of scattering and hence $\mathrm{T(E)} < 1$. Here, in this thesis we consider only electron-phonon scattering.

The atoms in any solid are constantly vibrating about their mean position with increased displacement as a function of temperature. These lattice vibrations are called phonons. Interaction of the mobile electrons and phonons is a major source of scattering called electron-phonon scattering. Electron-phonon scattering can be categorized into (1) acoustic phonon scattering which is nearly elastic scattering mainly with low energy acoustic phonons and (2) optical phonon scattering which is strongly inelastic scattering for carriers with energy (kinetic) greater than 0.160 eV [35]. The scattering strengths are characterized by mean free path (MFP). MFP is an average length an electron travel without scattering. In this thesis MFP for Acoustic phonon scattering is denoted by $\mathrm{l_{AP}}$ and for Optical phonon scattering is $\mathrm{l_{OP}}$. Figure 3.4 shows possible electron-phonon scatterings in a first subband [36]. The filled and empty circles indicate the states which are occupied and empty, respectively.

The arrows indicate some possible scattering transitions. The arrow 1 indicates an elastic electron-phonon scattering (no lose of energy), while the arrow 2 and 3 indicate inelastic electron-phonon scatterings. Because the optical phonon energy is about 0.160 eV with small dispersion, the emission energy of phonons required by inelastic electron-phonon scatterings is simply set at 0.160 eV. The transitions 1 and 2 toward empty states are permitted; however, the transition 3 toward filled states is prohibited because of the exclusion principle. Hence, scattering from substate, say, 1 to another substate 2 is allowed if (1) the substate 1 is filled with electrons, and (2) the substate 2 is empty so that it can accept the scattered carrier from substate 1.

Assuming that the optical phonon-scattering MFP which is recently shown to scale with diameter [37], at room temperature, to be $\mathrm{l_{OP}(300) = 15D_{CNT}}$ and the acoustic phonon-scattering MFP, $\mathrm{l_{AP}(300) = 651D_{CNT}}$, [38] are constant for given diameter if both conditions are met, we normalize the effective acoustic phonon-scattering MFP, $\mathrm{l_{AP,eff}(E,T)}$, and the effective optical phonon-scattering MFP, $\mathrm{l_{OP,eff}(E,T)}$, of the semiconducting subbands to the available target empty states [39].

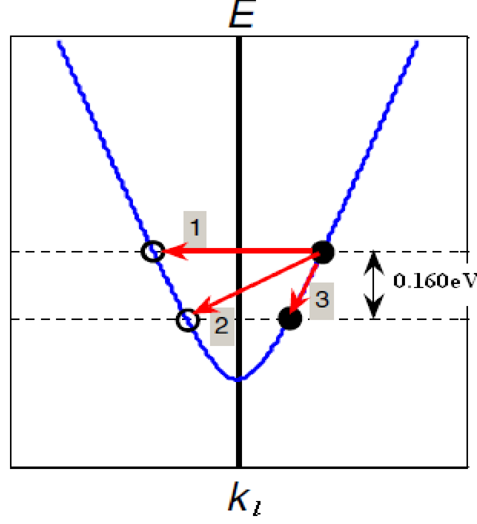


Figure 3.4 Possible electron-phonon scatterings [36]

$$l_{AP,eff}(E,T) = l_{AP}(300)\frac{300}{T}\frac{D_0}{D(E)\big(1-f(E)\big)} \tag{3.14}$$

$$l_{OP,eff}(E,T) = l_{OP}(300)\frac{N_{op}(300)+1}{N_{op}(T)+1}\frac{D_0}{D(E-\hbar\omega_{op})\Big(1-f\big(E-\hbar\omega_{op}\big)\Big)} \tag{3.15}$$

Where D_0 and $D(E)$ are as given in equation (2.12). f(E) is Fermi Dirac distribution function. $N_{op}(T) = 1/\left(e^{\hbar\omega_{op}/k_B T} - 1\right)$ is Bose-Einstein factor [40] which tells the Optical Phonon occupation and $\hbar\omega_{op} = 0.160$ eV is minimum kinetic energy required for optical phonon scattering to occur.

The effective phonon-scattering MFP, $l_{eff}(E,T)$ is, like conductance connected in series, in the form of

$$\frac{1}{l_{eff}(E,T)} = \frac{1}{l_{AP,eff}(E,T)} + \frac{1}{l_{OP,eff}(E,T)}$$

$$\Rightarrow\ l_{eff}(E,T) = \frac{l_{AP,eff}(E,T)\,l_{OP,eff}(E,T)}{l_{AP,eff}(E,T) + l_{OP,eff}(E,T)} \tag{3.16}$$

And transmission probability in equation (3.10) at given temperature is given by

$$T(E) = \frac{l_{eff}(E)}{l_{eff}(E) + L_g} \tag{3.17}$$

If we substitute equation (3.17) in to equation (3.11) it is not possible to evaluate the integral analytically and hence, approximations are needed.

The first approximation is for effective acoustic phonon scattering, $l_{AP,eff}$ equation (3.14). Acoustic phonon scattering is nearly constant with bias and $f(E)$ is negligible compared to one [32]. The other approximation is instead of density of state, $D(E)$, average density of state is used [32] and equation (3.14) is modified to:

$$l_{AP,eff} = \frac{l_{AP}(300)\frac{300}{T}}{\sqrt{1 + \frac{E_g}{1.83k_BT}}} \tag{3.18}$$

For optical phonon scattering, effective optical phonon scattering, $l_{AP,eff}$, for carrier energy higher than $\hbar\omega_{op} = 0.160$ eV is assumed to be constant with energy and equation (3.15) is modified to be:

$$l_{OP,eff} = l_{OP}(300)\frac{N_{op}(300) + 1}{N_{op}(T) + 1} \tag{3.19}$$

Therefore, for carrier kinetic energy below $\hbar\omega_{op} = 0.160$ eV only acoustic phonon scattering is considered and hence, effective phonon scattering is given by:

$$l_{eff,low} = l_{AP,eff} \tag{3.20}$$

On the other hand for carrier kinetic energy above $\hbar\omega_{op} = 0.160$ eV effective phonon scattering is given by:

$$l_{eff,high} = \frac{l_{AP,eff}l_{OP,eff}}{l_{AP,eff} + l_{OP,eff}} \tag{3.21}$$

And equation (3.17) is split into two; for kinetic energy lower than $\hbar\omega_{op}$ and for kinetic energy higher $\hbar\omega_{op}$.

$$T_{low} = \frac{l_{eff,low}}{l_{eff,low} + L_g} \tag{3.22}$$

$$T_{high} = \frac{l_{eff,high}}{l_{eff,high} + L_g} \tag{3.23}$$

And the integral in equation (3.11) is also split into two as follows

$$I_{thermo} = \frac{4e}{h}\sum_{p=1}^{P}\left[\int_{E(0,p)-eV_{ch}}^{E(0,p)-eV_{ch}+\hbar\omega_{op}} \big(f(E,\mu_s) - f(E,\mu_d)\big)T_{low}dE + \int_{E(0,p)-eV_{ch}+\hbar\omega_{op}}^{\infty} \big(f(E,\mu_s) - f(E,\mu_d)\big)T_{high}dE\right] \tag{3.24}$$

Integrating equation (3.24) we get:

$$I_{thermo} = \frac{4ek_BT}{h}\sum_{p=1}^{P}\left[T_{low}\left(ln\left(1 + e^{\frac{eV_{ch}-E(0,p)+\mu_s}{k_BT}}\right) - ln\left(1 + e^{\frac{eV_{ch}-E(0,p)+\mu_d}{k_BT}}\right)\right) + \left(T_{high} - T_{low}\right)\left(ln\left(1 + e^{\frac{eV_{ch}-E(0,p)-\hbar\omega_{op}+\mu_s}{k_BT}}\right) - ln\left(1 + e^{\frac{eV_{ch}-E(0,p)-\hbar\omega_{op}+\mu_d}{k_BT}}\right)\right)\right] \tag{3.25}$$

Note that $\mu_s - \mu_d = eV_{ds}$ and assuming $\mu_s = 0$ (reference) equation (3.25), which is general, is modified to be:

$$I_{thermo} = \frac{4ek_BT}{h}\sum_{p=1}^{P}\left[T_{low}\left(ln\left(1 + e^{\frac{eV_{ch}-E(0,p)}{k_BT}}\right) - ln\left(1 + e^{\frac{eV_{ch}-E(0,p)-eV_{ds}}{k_BT}}\right)\right) + \left(T_{high} - T_{low}\right)\left(ln\left(1 + e^{\frac{eV_{ch}-E(0,p)-\hbar\omega_{op}}{k_BT}}\right) - ln\left(1 + e^{\frac{eV_{ch}-E(0,p)-\hbar\omega_{op}-eV_{ds}}{k_BT}}\right)\right)\right] \tag{3.26}$$

3.4.2 Band to band tunneling current (I_{btbt})

Band to band tunneling (BTBT) is undesired effect that happens for higher bias voltage (V_{ds}) when the gate voltage is low/negative for n-type CNTFET or low/positive p-type CNTFET. For BTBT to occur in CNTFETs, fields along the length of a tube have to be created (V_{ds}) that are strong enough to shift the conduction and valence band relative to each other by at least the gap energy of the semiconductor [41]. Therefore one requirement for BTBT to occur is $eV_{ds} \geq E_g$ as shown in Figure 3.5. The other is there must be enough empty states at the drain side to accept the carriers that

tunnel from the source/channel region. The band to band tunneling probability (T_{btbt}) is given by [26], [42], [43]

$$T_{btbt} = exp\left(\frac{-\pi\sqrt{m_{eff}}\sqrt{\left(E_g\right)^3}}{8\, e\, \hbar\, F}\right) \tag{3.27}$$

Where m_{eff} is effective mass as given in equation (2.16), E_g is band gap, $\hbar$ is reduced plank's constant and $F = (V_{ds} + E_f - V_{ch})/l_{relax}$ is the electrical field triggering the tunneling process near

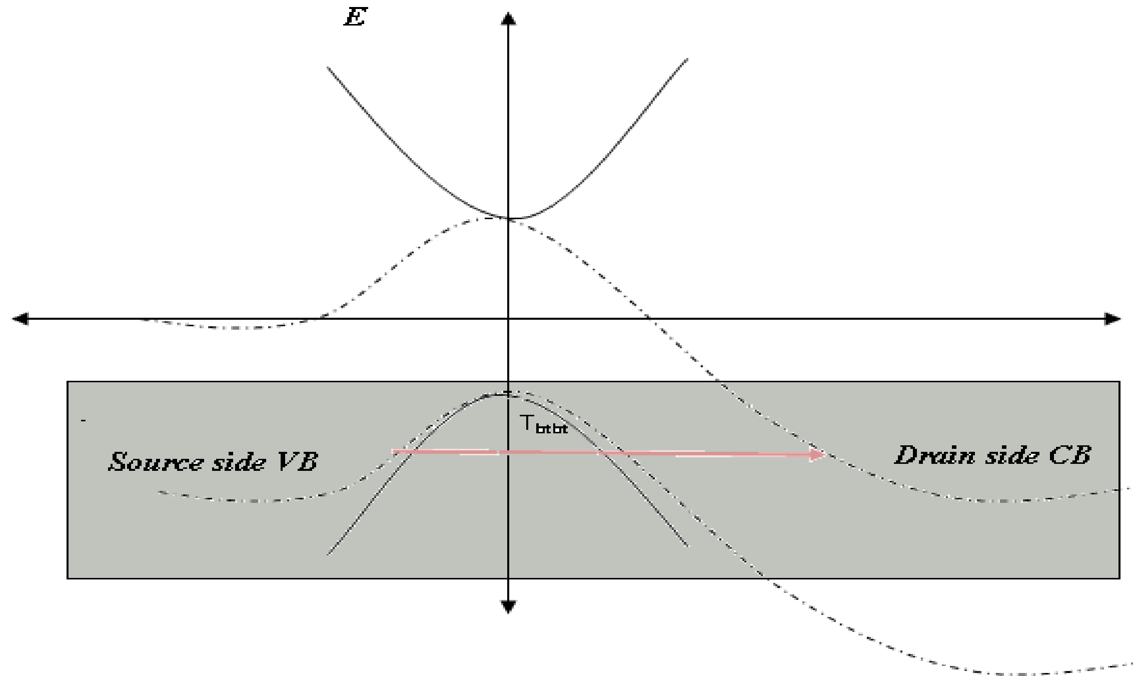


Figure 3.5 shows the region (shaded) in which tunneling likely to happen when gate voltage is low or zero. If drain side Conduction band (CB) is lower than source side valence band (VB) tunneling of electron from source/channel region to drain occur with probability T_{btbt}.

the drain side junction. Assuming the potential difference relaxes over the distance l_{relax} which is a fitting parameter. In this thesis $l_{relax} \approxeq L_g/2$ is taken as default unless specified to fit to experimental data.

The BTBT current is approximated by the BTBT tunneling probability (T_{btbt}) times the maximum possible tunneling current integrating from the conduction band at drain side up to the valance band at source side [26],

$$I_{btbt} = \frac{4e}{h} \int_{\frac{E_g}{2}-E_f}^{eV_{ds}-\frac{E_g}{2}-E_f} (1 - f(E))T_{btbt} dE \tag{3.28}$$

E_f is fermi level of doped source/drain region. Evaluating equation (3.28) for $eV_{ds} > E_g$ gives:

$$I_{btbt} = \frac{4ek_BT}{h} T_{btbt} \left[\ln\left(1 + e^{\frac{eV_{ds}-E_g/2-E_f}{k_BT}}\right) - \ln\left(1 + e^{\frac{E_g/2-E_f}{k_BT}}\right) \right] \cdot \frac{max(eV_{ds} - E_g, 0)}{eV_{ds} - E_g} \tag{3.29}$$

3.5 Source and drain region resistance

The heavily doped nanotube regions of the CNTFET can act as both the Source/Drain extension region and the local interconnect between two adjacent devices. Two typical cases for device connectivity are considered [33]: 1) The drain of one transistor is connected to the source of another transistor, i.e., the doped CNT acts as interconnect between two devices in series without a metal contact in between as shown in Figure 3.6 (a), and 2) the Source/Drain of one transistor is connected to the metal contact, e.g., at the output node as shown in Figure 3.6 (b).

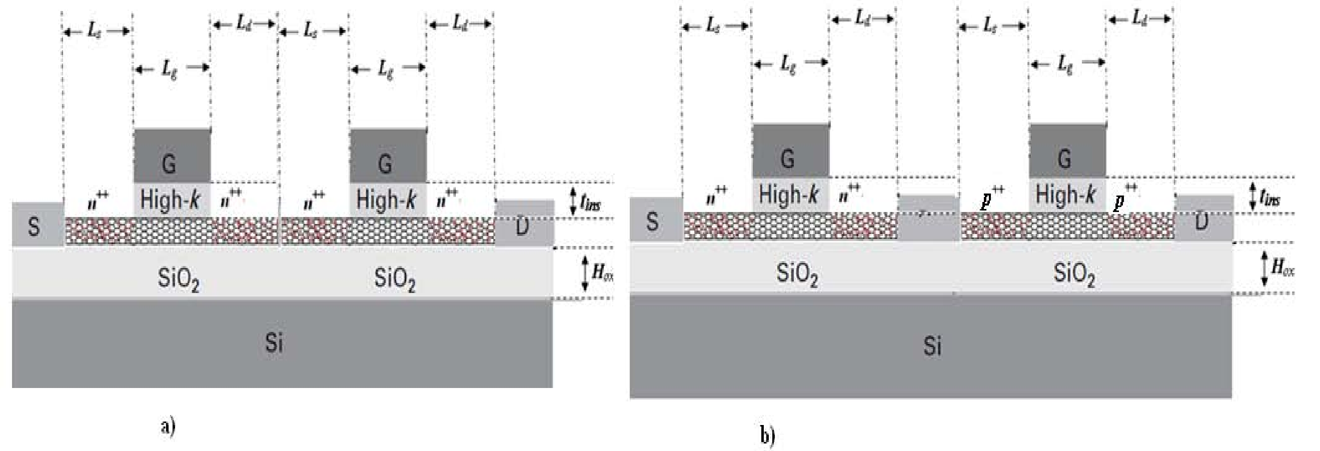


Figure 3.6 shows two MOSFET-like CNTFETs a) that are connected directly with a doped CNT and (b) that are connected by metal contact.

The resistance of an ideal carbon nanotube connected to transparent (reflection less) contact is the quantum resistance or contact resistance, R_q, which is given by [44]:

$$R_q = \frac{h}{4e^2} \tag{3.30}$$

The quantum resistance is only valid when electrons travel without scattering i.e. when the length L of the CNT is much shorter than the electron effective MFP. For arbitrary CNT lengths greater than the mean free path, electrons will experience scattering and the total resistance taking in to account scattering effect is given by: [44]

$$R = R_q \left[1 + \frac{L}{l_{eff}}\right] = R_q + R_q \frac{L}{l_{eff}} \tag{3.31}$$

Hence, total resistance given in equation (3.31) has two parts: the 1st one (to the left of the equation) is resistance between CNT to Metal interface and the 2nd part is due to scattering in CNT region. For the two device connectivity cases stated above in Figure 3.6, if the two devices are connected directly with doped CNT then there will be no contact resistance and the resistance will be due to only scattering effects given by:

$$R_{s,d} = R_q \frac{L_{s,d}}{l_{eff}} \tag{3.32}$$

If the two devices are connected with metal contact in between contact resistance has to be included and total resistance is given by

$$R_{s,d} = R_q + R_q \frac{L_{s,d}}{l_{eff}} \tag{3.33}$$

We can define two parameters S_c or D_c representing the source or drain connectivity: they are equal to 0 if source (drain) is connected to the doped CNT; otherwise, they are equal to 1. Hence, equations (3.32) and (3.33) are modified to:

$$R_s = R_q S_c + R_q \frac{L_s}{l_{eff}} \ and \ R_d = R_q D_c + R_q \frac{L_d}{l_{eff}} \tag{3.34}$$

Where l_{eff} is effective MFP around 20–50 nm depending on doping level of CNT [45] and set 20 nm as default.

CHAPTER 4

METHODOLOGY OF VHDL-AMS IMPLEMENTATIONS, SIMULATION RESULTS AND APPLICATIONS

In chapter three the model equations of MOSFET-like CNTFET were successfully developed. In this chapter, we do implement them in VHDL-AMS and simulate the curve tracer circuit that is used for simulation of I-V characteristics using DC sweep analysis in Simplorer 7.0 student version VHDL-AMS simulator from Ansoft Corporation [46]. Also the model is validated by constructing circuits.

4.1 VHDL-AMS Implementations

As introduced in section 1.1.3, VHDL-AMS is a hardware description language for describing digital, analog and mixed-signal electrical as well as non-electrical systems [47]. It supports the hierarchical description and simulation of continuous and mixed-continuous/discrete system [48]. The language support modeling at various abstraction levels in electrical and nonelectrical energy domains. The devices to be modeled are described by ordinary differential equations and algebraic equations. The solution of the equations describing the behavior of the system may include discontinuities. It has a ways of handling discontinuities for example by using 'BREAK' statement.

A VHDL-AMS model consists of an entity and one or more architectures. The entity specifies the interface of the model to the outside world. It includes the description of the ports of the model (the points that can be connected to other models) and the definition of its generic parameters. The architecture contains a set of equations and declarations for the implementation of the model. It may be coded using a structural style of description, a behavioral style, or a style combining structural, and behavioral elements. A structural description is a netlist; it is a hierarchical decomposition of the model into appropriately connected instances of other models. A behavioral description consists of concurrent statements to describe event-driven behavior and simultaneous statements to describe continuous behavior. Concurrent statements include the concurrent signal assignment for data flow modeling and the process statement for more general event-driven modeling. For the details about modeling with VHDL-AMS the reader is referred to reference [47] and [48].

4.1.1 CNTFET VHDL-AMS Model

In our CNTFET modeling case, the ports to be described are Drain, Source, Gate, and Bulk of nature electrical as shown in Figure 4.1 at 25th line. Those ports are used to connect to other circuit components. The parameters used in our model, as stated in chapter three, are channel length (L_g), doped source extension length (L_s), doped drain extension length (L_d), gate to channel insulator thickness (t_{ins}), dielectric constant of insulator between channel and substrate (k2), dielectric constant of insulator between channel and gate (k1), chirality indexes (n, m), source connectivity (S_c), drain connectivity (D_c), Temperature (Tem), and Fermi levels of doped region (E_f). Those parameters are declared as 'generic constants' as shown in Figure 4.1 from 11th line to 24th line. We used four 'packages'. Lines 5th and 6th show the packages for calculating currents contributed by 1st subband and 2nd subband respectively. The 7th line shows a package for calculating channel potential. The 8th line shows a package that contains commonly used constants such as plank's

```
1   LIBRARY IEEE;
2   USE IEEE.math_real.ALL;
3   USE IEEE.electrical_systems.ALL;
4   LIBRARY work;
5   USE work.Ids_1.ALL;
6   USE work.Ids_2.ALL;
7   USE work.channel_potential.ALL;
8   USE work.physical_constants.ALL;
9   ENTITY nCNTFET IS
10      GENERIC(--MODEL PARAMETERS
11          Lg:REAL:=2.0E-8;--channel length or gate length
12          Ls:REAL:=1.0E-8;--doped source side length
13          Ld:REAL:=1.0E-8;--doped drain side length
14          tins:REAL:=8.0E-9;--Gate to channel insulator thickness
15          k1:REAL:=15.0; --dielectric constant of gate to channel insulator
16          k2:REAL:=3.9; --dielectric constant of channel to substrate insulator
17  --      n   : REAL := 19.0;--chiral number
18  --      m   : REAL := 0.0;--chiral number
19          dcnt:REAL:=1.5e-9;-- diameter of the tube
20          Sc:REAL:=0.0;--source connectivity which is 0.0 if source connected to doped CNT
21          Dc:REAL:=0.0;--source connectivity which is 0.0 if source connected to doped CNT
22          Tem: REAL := 300.0;--Temperature
23          Vfb:REAL:= 0.0;-- flat band voltage
24          Ef :REAL :=0.0);----Fermi level of doped regions
25      PORT(TERMINAL Drain, Gate, Source, Bulk:ELECTRICAL);
26  END ENTITY nCNTFET;
```

Figure 4.1 Interface for n-type MOSFET-like CNTFET VHDL-AMS model; the entity

constant, pi, electron charge and others used in our model. The ports' and the parameters' names are the same for both n-type and p-type MOSFET-like CNTFET. Therefore, only the name of the "ENTITY" is different. For n-type MOSFET-like CNTFET we used the entity name nCNTFET and

for p-type MOSFET-like CNTFET the entity name is pCNTFET. The whole codes of both nCNTFET and pCNTFET models are given in Appendix.

4.1.2 CNTFET symbol

Different authors used different symbols for carbon nanotube field effect transistors. Figure 4.2 shows the commonly used symbols. Figure 4.2 (a) shows the symbols used by Prégaldiny et al [49]. Figure 4.2 (b) shows the symbols used by O'Connor et al [50].We used the symbol shown in Figure 4.2 (c) which is the commonly used symbol for FETs. The simulator used is SIMPLORER simulation system Version 7.0.5 student version © Ansoft Corporation for DC sweep analysis and SIMPLORER simulation system Version 9.0 © Ansoft Corporation for circuits having greater than two transistors [46]. They have internal symbol generator and templates.

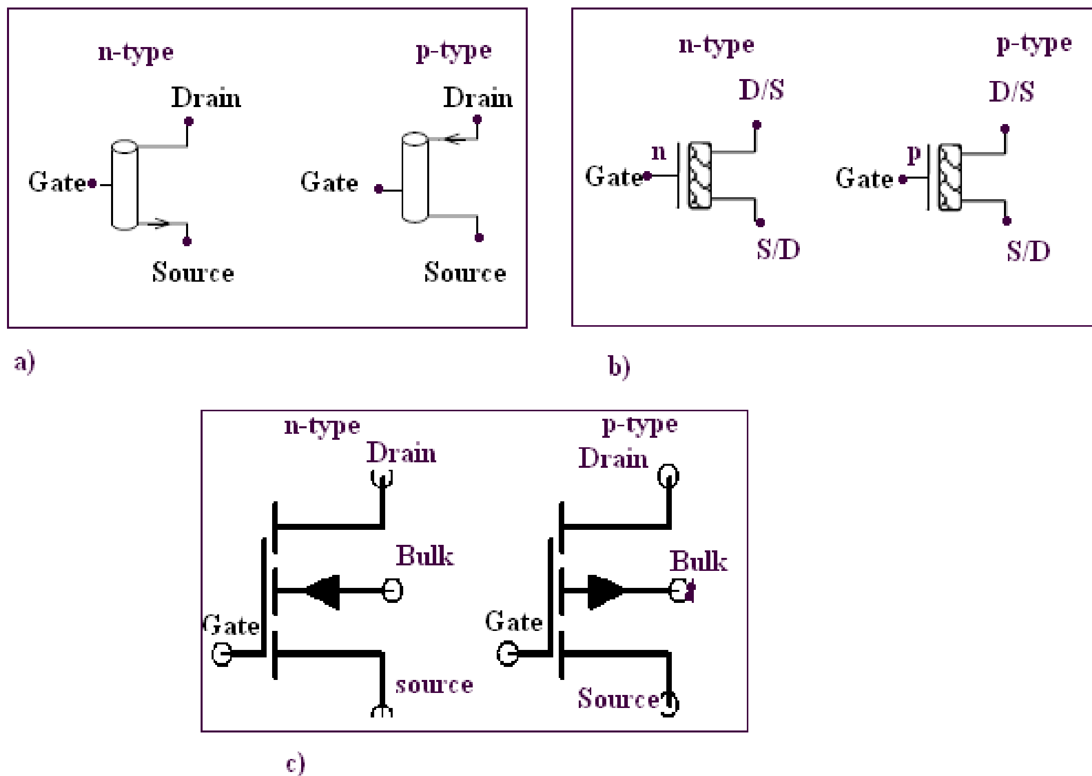


Figure 4.2 Different symbols used for CNTFETs a) symbols used by Prégaldiny et al [49] b) symbols used by O'Connor et al [50] c) commonly used FET symbols

4.2 Simulation results

The analytical expression of the current given in chapter three, in equation (3.26) and equation (3.29) is used for simulation with the following parameters:

- Channel length L_g=20.0 nm,
- Doped source extension region L_s=10.0 nm,
- Doped drain extension region L_d=10.0 nm,
- Thickness of insulator between gate and channel t_{ins}=8.0 nm,
- Chirality n=19 and m=0 which correspond to diameter D_{cnt}=1.5 nm,
- Dielectric constant of insulator between gate and channel is assumed to be Hafnium Dioxide (HfO_2) with k1=15.0,
- Dielectric constant of insulator between substrate and channel assumed to be silica (SiO_2) k2=3.9,
- Doped regions Fermi level Ef=0.0 eV,
- Flat band voltage V_{fb}=0.0 V,
- Source connectivity which is Sc=1.0 if connected to metal and Sc=0.0 if connected to another CNT with default status connected to another CNT i.e. Sc=0.0,
- Drain connectivity which is Dc=1.0 if connected to metal and Dc=0.0 if connected to another doped CNT with default status connected to another CNT i.e. Dc=0.0 and
- Tem=300.0 Temperature in Kelvin.

Those listed parameters' values are default values unless specified. Our simulation is done using Simplorer 7.0 student version VHDL-AMS simulator from Ansoft Corporation [46]. With this simulator we can create our own library, in 'Model Agent', in which we wrote our own model's VHDL-AMS code, and created the symbol. Advantage of this simulator is we can use schematics rather than hand written test bench. We can run TR, DC, and AC analysis. In addition, we can perform DC sweep analysis that is essential for us, for instance, to see I_{ds} vs. V_{ds} for different values of V_{gs}. Curve tracer circuit used is shown in Figure 4.3.

4.2.1 Current-voltage (I-V) Characteristics

Current-voltage characteristics using VHDL-AMS implemented model of MOSFET-like CNTFET is shown in this subsection. Figure 4.4 shows drain to source current (I_{ds}) versus drain voltage or

from Figure 4.3 I_{ds} versus 'e2' for different values of 'e1'. As it can be clearly seen from the Figure 4.4, on-current (I_{on}) depends on gate voltage.

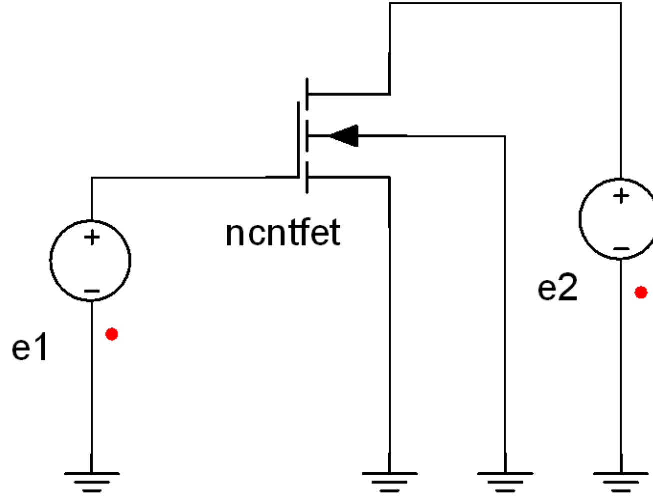


Figure 4.3 The nCNTFET circuit used for tracing curves with different bias and parameter variation

For example for V_g=0.60 V the on-current is I_{on}=19.89 μA and for V_g=0.50 V the on-current is I_{on}= 9.70 μA. To get the expression for on-current equation (3-26) and equation (3-29) are rewritten as:

$$I_{thermo} = \frac{4ek_BT}{h}\sum_{p=1}^{P}\left[T_{low}\left(\ln\left(1+e^{\frac{eV_{ch}-E(0,p)}{k_BT}}\right)-\ln\left(1+e^{\frac{eV_{ch}-E(0,p)-eV_{ds}}{k_BT}}\right)\right)\right.$$
$$\left.+\left(T_{high}-T_{low}\right)\left(\ln\left(1+e^{\frac{eV_{ch}-E(0,p)-\hbar\omega_{op}}{k_BT}}\right)-\ln\left(1+e^{\frac{eV_{ch}-E(0,p)-\hbar\omega_{op}-eV_{ds}}{k_BT}}\right)\right)\right] \qquad (4.1)$$

and

$$I_{btbt} = \frac{4ek_BT}{h}T_{btbt}\left[\ln\left(1+e^{\frac{eV_{ds}-E_g/2-E_f}{k_BT}}\right)-\ln\left(1+e^{\frac{E_g/2-E_f}{k_BT}}\right)\right]\cdot\frac{max(eV_{ds}-E_g,0)}{eV_{ds}-E_g} \qquad (4.2)$$

Now as V_{ds} is getting larger equation (4.1) reduced to:

$$I_{thermo,ON} = \frac{4ek_BT}{h}\sum_{p=1}^{P}\left[T_{low}\left(\ln\left(1+e^{\frac{eV_{ch}-E(0,p)}{k_BT}}\right)\right)+\left(T_{high}-T_{low}\right)\left(\ln\left(1+e^{\frac{eV_{ch}-E(0,p)-\hbar\omega_{op}}{k_BT}}\right)\right)\right] \qquad (4.3)$$

Clearly, equation (4.3) is function of V_{ch} which is in turn a function of V_{gs}. However, I_{btbt} is function of both V_{gs} and V_{ds}, hence, remains affected as V_{ds} gets higher and higher especially when $V_{ds}>E_g/e$ and the total on-current is given by:

$$I_{on} = I_{thermo,ON} + I_{btbt} \tag{4.4}$$

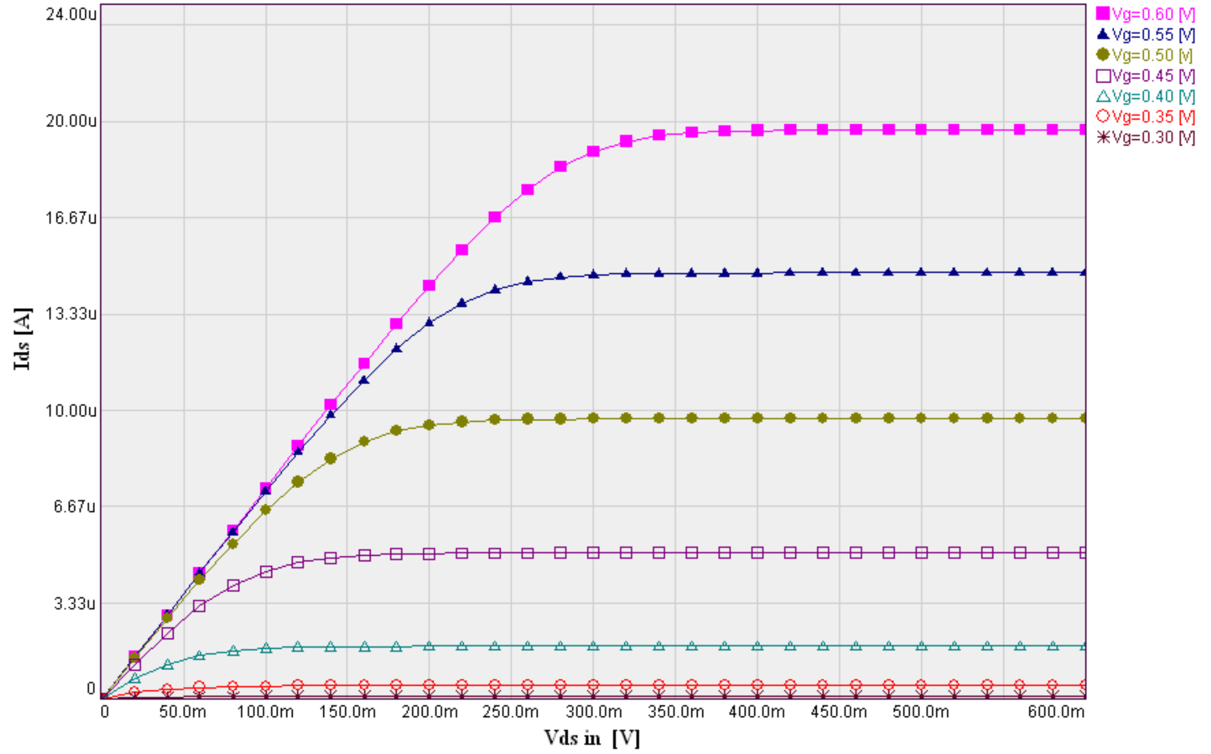


Figure 4.4 I_{ds} versus V_{ds} for different values of gate voltage Vg (0.30 V to 0.60 V with steps of 0.05 V) with Ef=-0.08 eV and other parameters as default.

Figure 4.5 shows I_{ds} Versus V_{gs} in linear scale for different values V_{ds}. From the figure we see that threshold voltage does not depend on V_{ds}. For two different values of V_{ds} (e.g. 0.2 V and 0.6 V) threshold voltage is the same. Generally, the threshold voltage (V_{th}) for an FET is defined as the gate voltage at which a sufficient amount of carriers are induced to create a conducting channel. And for our model as discussed in chapter three sufficient amount of carriers start to be induced when minimum of subband starts falling below Fermi level. Therefore, at this instant the gate voltage is approximately equal to $E_g/2$. Hence, the threshold voltage is given by:

$$V_{th} = \frac{E_g}{2e} \tag{4.5}$$

For example for our default diameter, 1.5 nm, using equation (2.9) E_g=0.593 eV and the threshold voltage (V_{th}) is then calculated to be V_{th}=0.297 V which is evident from Figure 4.5.

Figure 4.6 shows I_{ds} versus V_{gs} in logarithmic scale for different values V_{ds}. From the figure we see unfamiliar behavior for V_{ds}=0.6 V. When V_{ds}=0.6 V the threshold current is higher than expected. This unfamiliar thing happened due to band to band tunneling effect that starts to take effect for $eV_{ds}>E_g$ as detailed in chapter three section 3.4.2. This effect is reduced by (1) using $V_{ds}<E_g/e$, (2) a stair-case doping strategy in drain lead reported by Z. Hai-liang et al [51].

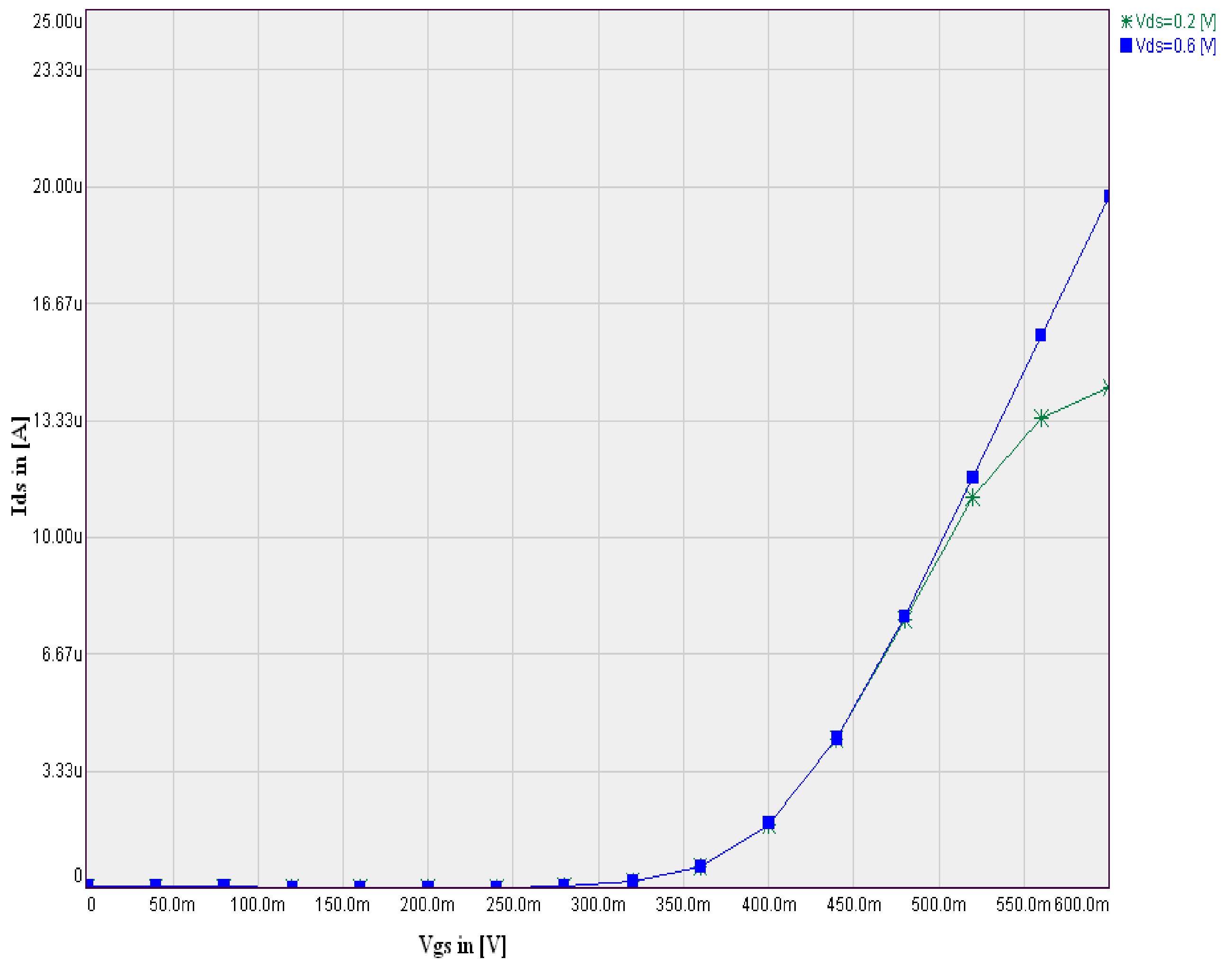


Figure 4.5 I_{ds} versus V_{gs} for V_{ds}=0.2 V and V_{ds}=0.6 V with E_f=-0.08 eV and other parameters as default. Linear scale

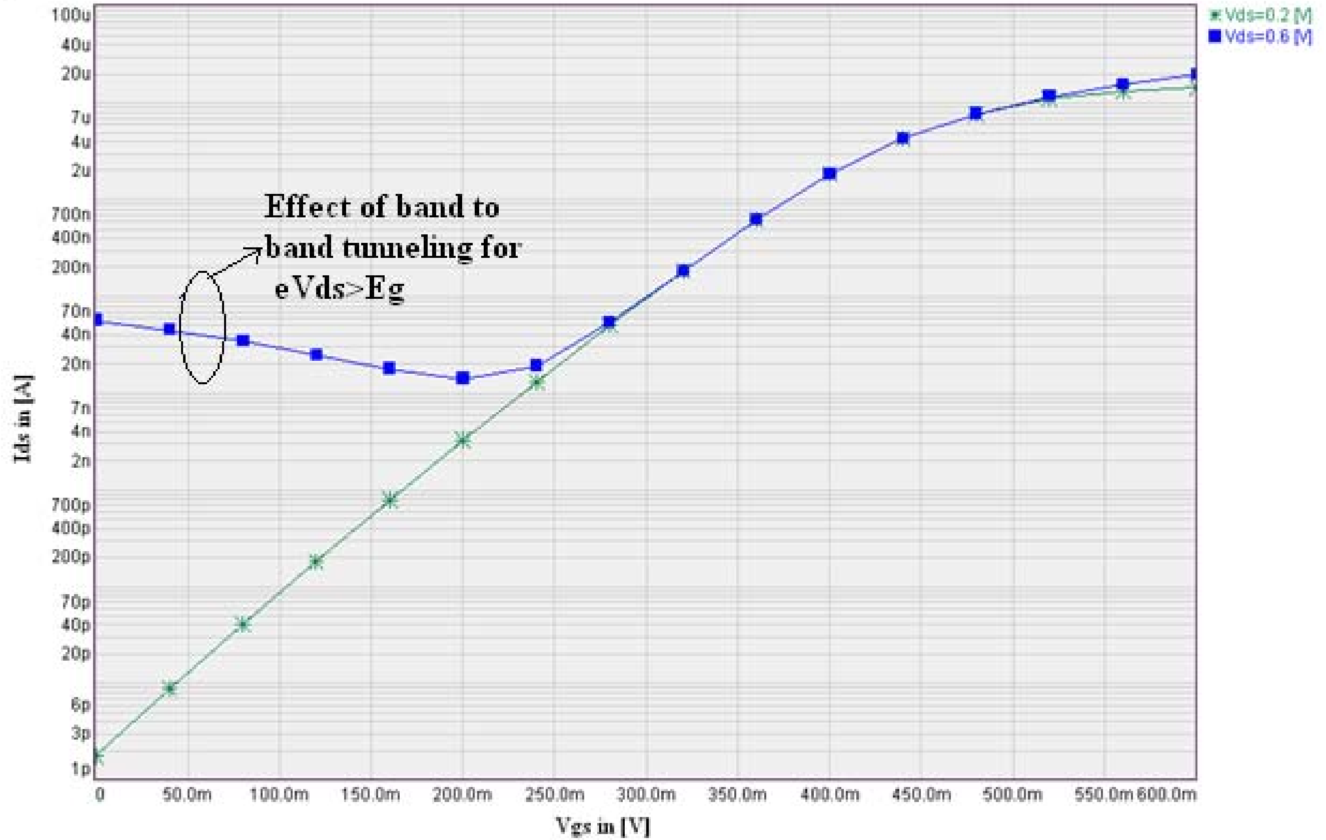


Figure 4.6 I_{ds} versus V_{gs} for V_{ds}=0.2 V and V_{ds}=0.6 V with E_f=-0.08 eV and other parameters as default. Logarithmic scale, it shows clearly the effect of band to band tunneling current.

4.2.2 Comparing with other models

We compared our model with the model developed by Frégonèse *et al* which is shown in Figure 4.7 (a) [32]. The model is relatively recent and includes electron-phonon scattering effects though it lacks to consider the effects of doped region source/drain resistances which affect saturation voltage. The two models are similar, for example, the on-current for both models is around 20 µA for V_g=0.6 V. However, the slight difference is that our model saturates above some drain voltage, for example, for V_{gs}=0.5 V and V_{ds}>150 mV and the model developed by Frégonèse et al shows slow increment. This is due to capacitance between source/drain and channel which relates V_{ds} to V_{ch}, and hence, the dependency of V_{ch} on V_{ds}. This capacitance is not calculated analytically but depends on the contact between CNT channel and source/drain lead metal, which is in turn, depends on manufacturing process. In some papers it is taken as a fitting parameter, but we neglected that

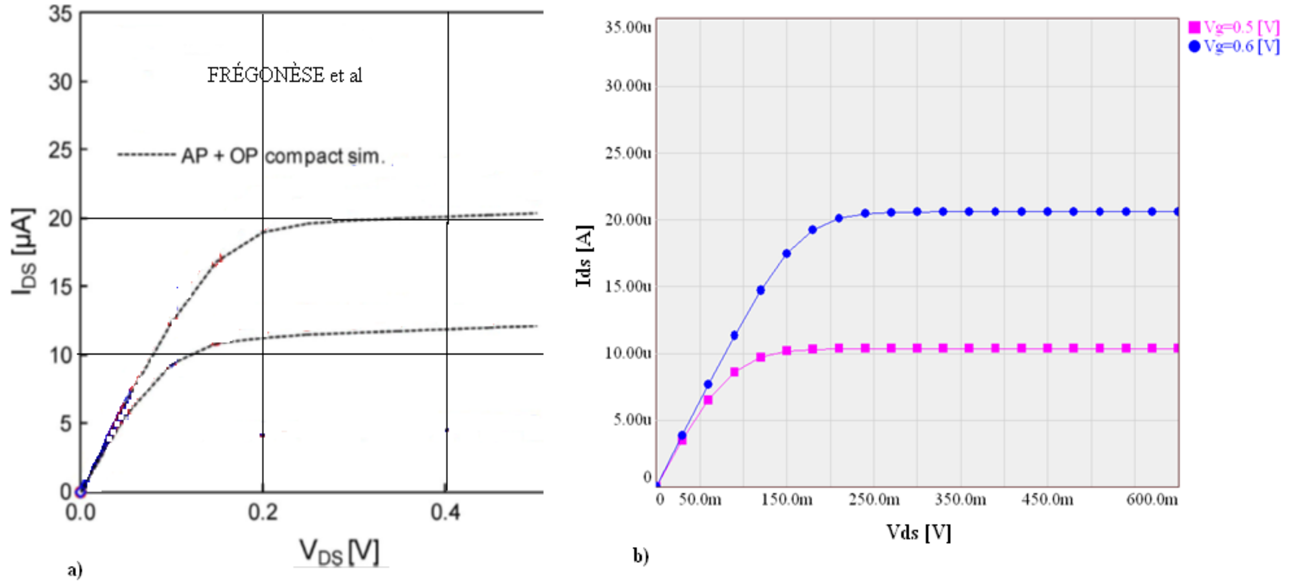


Figure 4.7 a) I_{ds} versus V_{ds} of MOSFET like CNTFET model developed by Frégonèse et al for V_g=0.5 V and V_g=0.6 V [32] b) I_{ds} versus V_{ds} of MOSFET-like CNTFET model developed for V_g=0.5 V and V_g=0.6 V

capacitance. Continuous increment of current, though slowly, is not realistic because at some point all states available will be occupied and no more empty state for more electrons i.e. number of carriers in the channel is limited which limit current.

4.2.3 Effect of insulator thickness

Now we look into the effect of insulator thickness on CNTFET performance. Figure 4.8 shows I_{ds} versus V_{gs} for V_{ds}=0.6 V and different insulator thicknesses. From the figure we see that reducing insulator thickness increases on-current without increasing off-current. Therefore, reducing insulator thickness improves I_{on}/I_{off} ratio significantly.

This effect can be seen from chapter three equation (3.6) which is rewritten here as:

$$V_{ch} = \frac{C_{ins}}{C_{ins} + C_q(V_{ch})} V_{gs} \qquad (4.6)$$

If we reduce insulator thickness (t_{ins}), C_{ins} is increased because of inverse relationship between them. And as C_{ins} increased the cofficient of V_{gs} in equation (4.6) approaches unity and hence V_{ch} increased and this means from equation (4.3) I_{on} is increased .

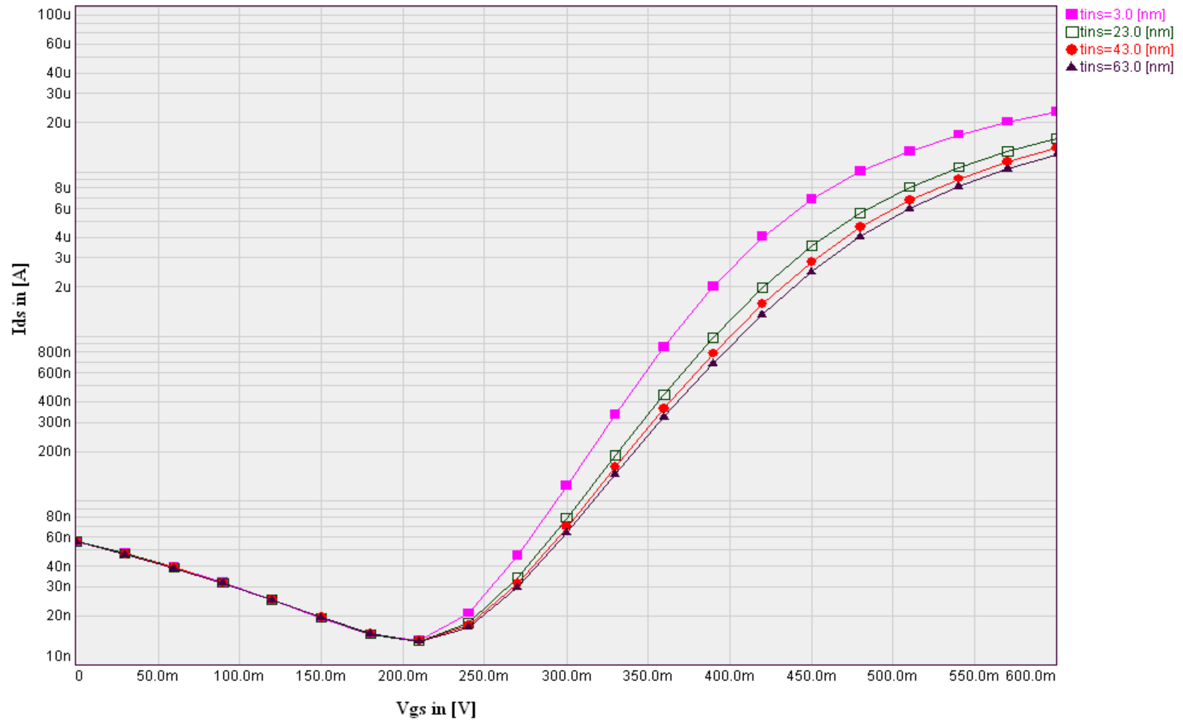


Figure 4.8 I_{ds} vs. V_{gs} for V_{ds}=0.6 V and different insulator thicknesses and shows clearly the effect of insulator thickness

4.2.4 Effect of diameter variation

Recall from section 2.1.1 band gap is inversely proportional to diameter of CNT and also from section 4.2.1 threshold voltage is half of band gap and hence threshold voltage is inversely proportional to diameter. Figure 4.9 shows this expected effect. For smaller diameter (D_{cnt}=1.0 nm) and for larger diameter (D_{cnt}=1.6 nm) the threshold voltage is 0.45 V and 0.28 V respectively. In addition, on-current is also affected for different diameters. Larger diameter means smaller band gap (E_g) which in turn implies, from equation (4.3), larger on-current. However, when we see Figure 4.9 in logarithmic scale, as in Figure 4.10, an effect that is not seen clearly in linear scale is observed. Remember that drain bias we used is V_{ds}=0.6 V and also the band to band tunneling effect starts when $eV_{ds} > E_g$. For D_{cnt} = 1.0 nm E_g=0.89 eV, for D_{cnt}=1.3 nm E_g=0.68 eV and for D_{cnt}=1.6 eV E_g=0.56 eV. From these values E_g we see that $eV_{ds}>E_g$ for only D_{cnt}=1.6 nm. And as shown on the Figure 4.10 the band to band tunneling effect seen for D_{cnt}=1.6 nm. Therefore, using CNTs with larger diameters will increase on-current and also the leakage current. This means the choice of the diameter brings to a trade-off between the need of larger diameters (as in ternary logic gates) and the on-off-current ratio.

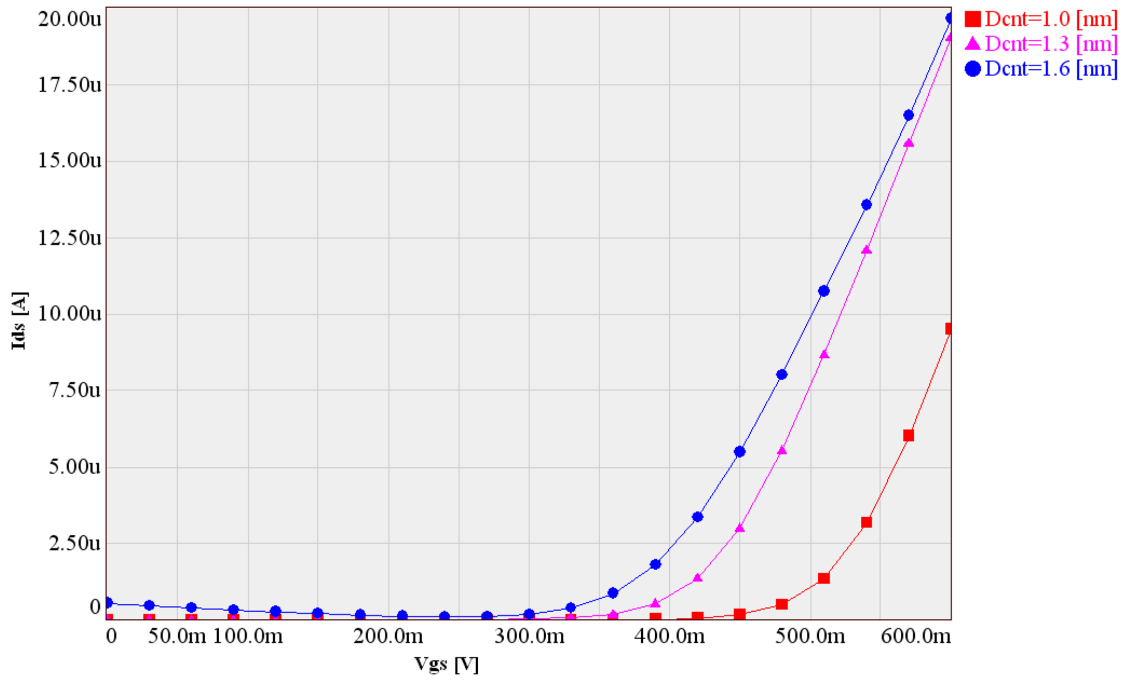


Figure 4.9 I_{ds} vs. V_{gs} for V_{ds}=0.6 V and different diameters (1.0 nm, 1.3 nm and 1.6 nm): linear scale

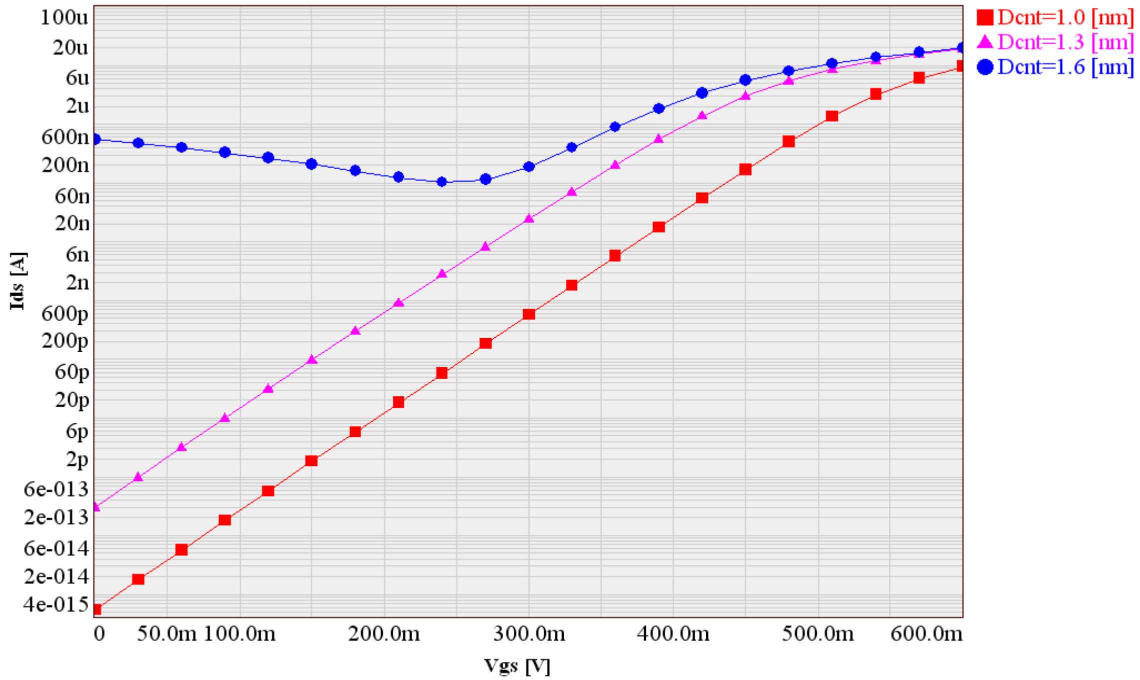


Figure 4.10 I_{ds} vs. V_{gs} for V_{ds}=0.6 V and different diameters (1.0 nm, 1.3 nm and 1.6 nm): logarithmic scale

4.2.5 Effect of dielectric constant variation

The effect of using different dielectric materials as insulator between gate and channel is seen this section. The dielectric materials considered along with their dielectric constants (k1) are listed in the following table.

Name of the insulator	Chemical formula	Dielectric constant (k1)
Zirconium Silicate [52]	$ZrSiO_4$	5
Hafnium Silicate [52]	$HfSiO_4$	11
Hafnium Dioxide [52]	HfO_2	15
Zirconium Dioxide [52]	ZrO_2	25
Titanium Dioxide [53]	TiO_2	80

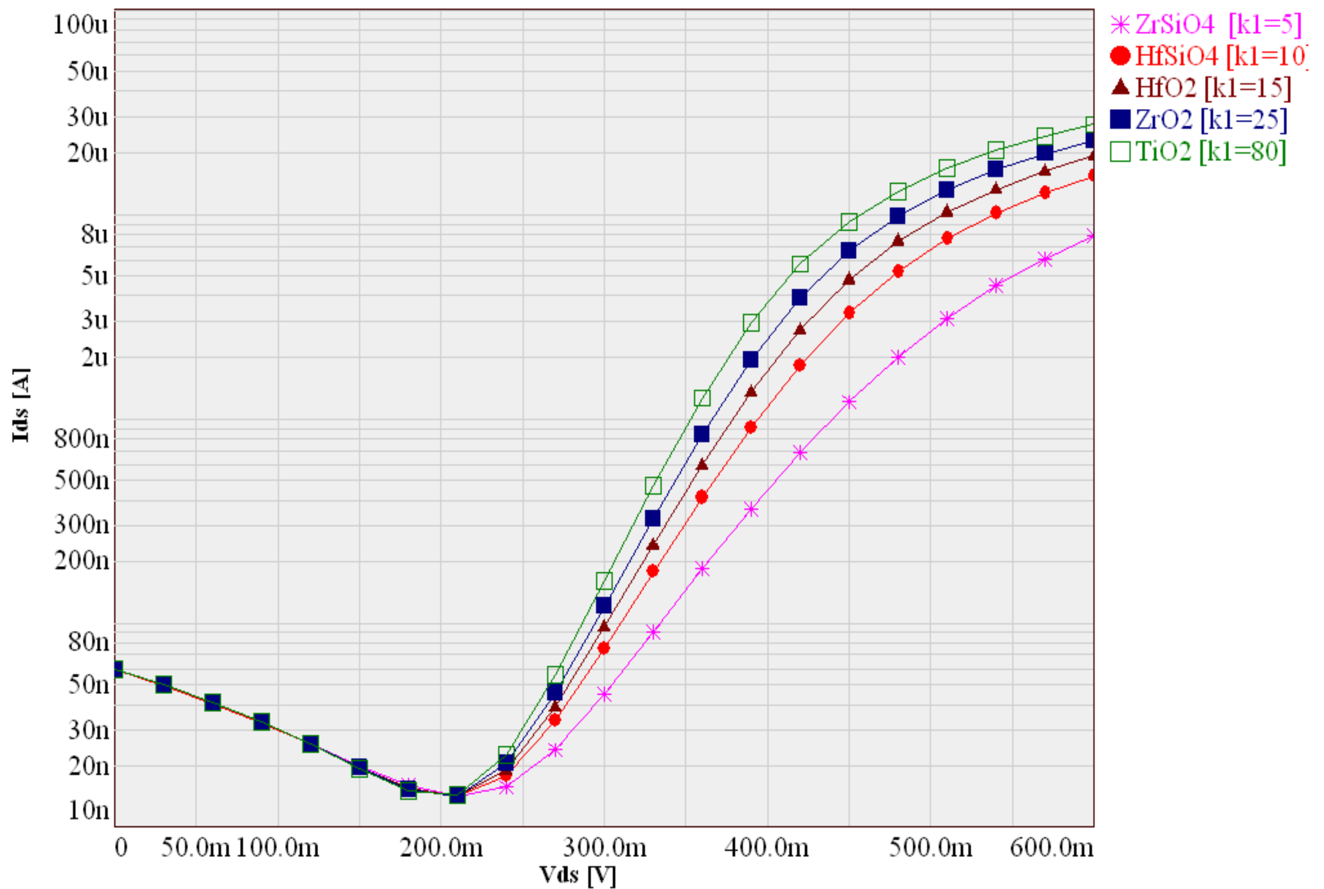


Figure 4.11 I_{ds} vs. V_{gs} for V_{ds}=0.6 V and different dielectric materials: Logarithmic scale

Simulation results are shown in Figure 4.9. It is clear from the plot is that the on-current increases for increasing dielectric constant without increasing off-current but degree of this positive effect reduces as we go for higher dielectric material. This means that as we are going for higher and higher dielectric material the increment in I_{ds} with respect to k1 reduces. For example, for Zirconium Silicate ($ZrSiO_4$) with k1=5 on-current from the plot is I_{on}= 7.876 µA and for Hafnium Silicate ($HfSiO_4$) with k1=10 on-current is I_{on}=15.462 µA which is about two times that of Zirconium Silicate. However, if we take Titanium Dioxed (TiO_2) with k1=80 the on-current is Ion=27.579 µA which is only about two times of that of $HfSiO_4$ but dielectric constant of TiO_2 is 8 times that of $HfSiO_4$.

4.2.6 Effect of channel length scaling

The influence of channel length scaling on the performances of carbon nanotube field effect transistors (CNTFETs) is studied in this section. From the plot of Figure 4.12, we observe that on-current increases as we reduce the channel length which is evident from equation (3.17). Rewriting it again here:

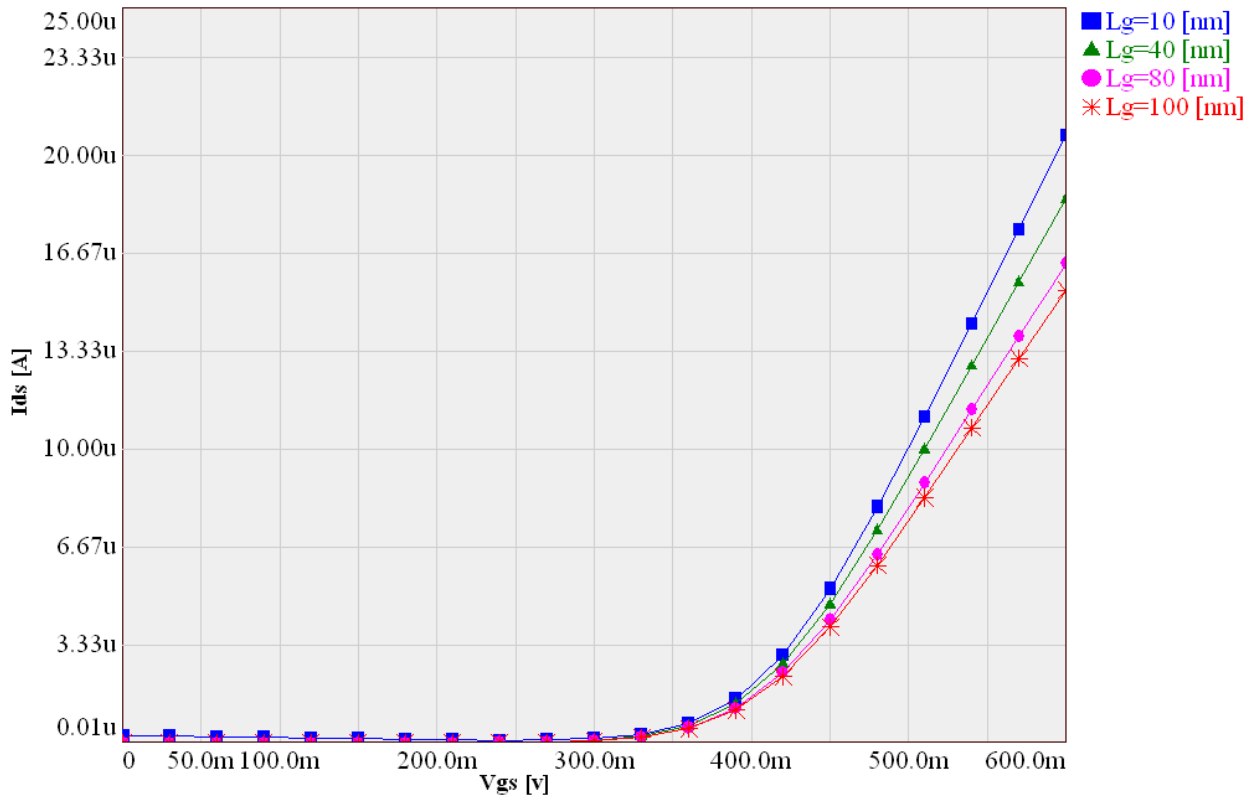


Figure 4.12 I_{ds} vs. V_{gs} for V_{ds}=0.6 V and different channel length from L_g=10.0 nm, L_g=40.0 nm, L_g=80.0 nm and L_g=100 nm: linear scale

$$T(E) = \frac{l_{eff}(E)}{l_{eff}(E) + L_g} \tag{4.7}$$

It is clear from equation (4.7) that as L_g is decreased transmission probability $T(E)$ increase which in turn increases I_{on}. This is desired effect to get two fold advantages from scaling channel length. In addition to higher on-current, scaling channel length increases number of transistors per area which is important at ultra large scale integration (ULSI). However, when we come to off-current or sub threshold current, from Figure 4.13, the advantage we got was reverted due to band to band tunneling effect stated in previous sections. Therefore, in order to keep scaling of channel of CNTFETs without degrading I_{on}/I_{off} ratio there must be a way to suppress band to band tunneling current. The two solutions proposed as stated in section 4.2.1 are (1) using drain bias voltage less than band gap and (2) using a stair-case doping strategy in drain lead reported by Z. Hai-liang et al in [51].

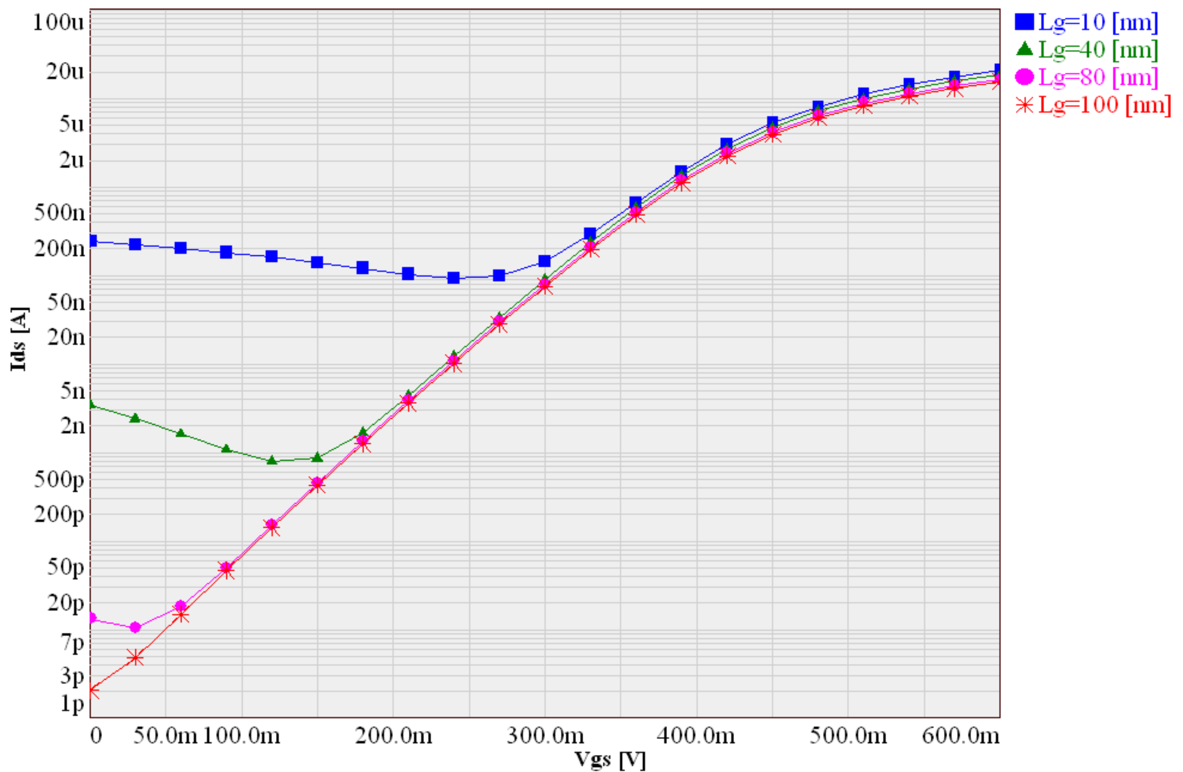


Figure 4.13 I_{ds} vs. V_{gs} for V_{ds}=0.6 V and different channel length from L_g=10.0 nm, L_g=40.0 nm, L_g=80.0 nm and L_g=100 nm: logarithmic scale

4.2.7 Effect of temperature variation

Figure 4.14 shows the plots of I_{ds} versus V_{gs} for different temperature in logarithmic scale. As it can be seen from the figure increasing temperature lowers on-current and increases off-current which hurts the I_{on}/I_{off} ratio. However, decreasing temperature increases on-current and decreases off-current. Usually working temperature for electronic device is room temperature and this is just to show the sensitivity of the device to temperature variation.

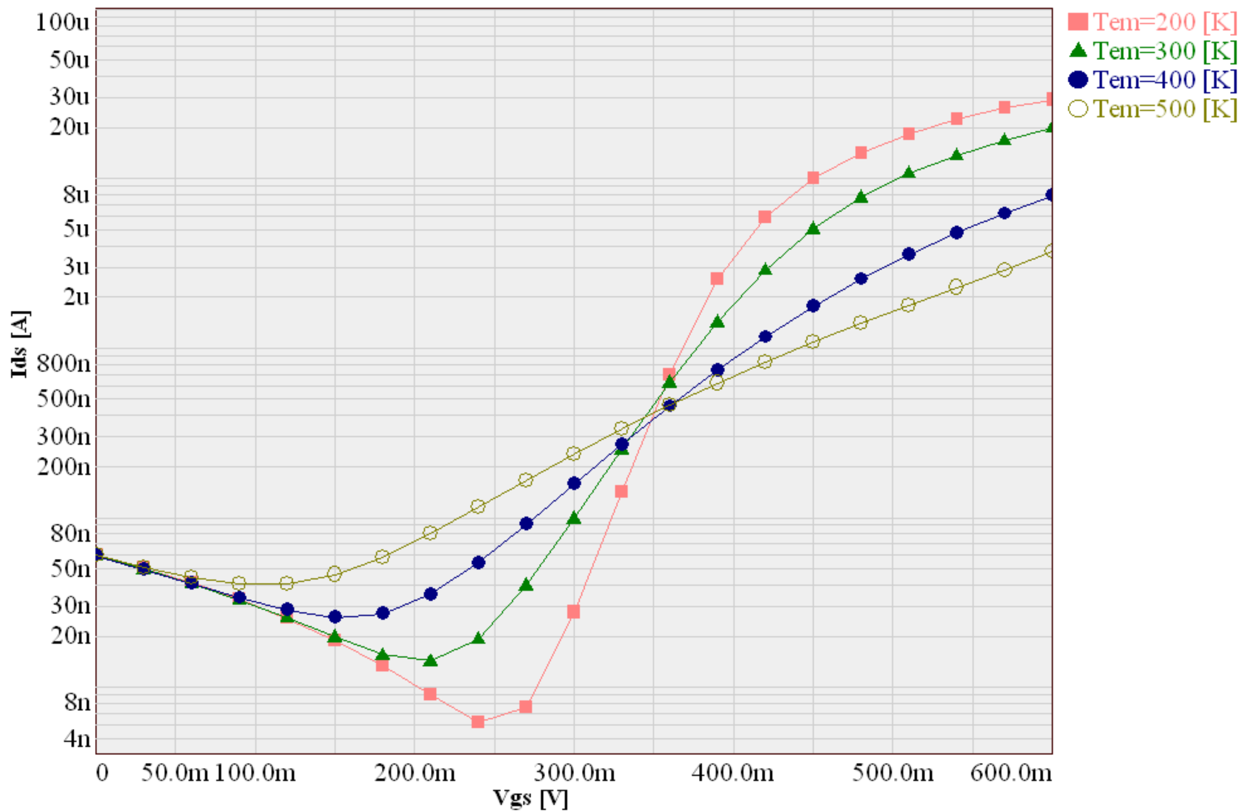


Figure 4.14 I_{ds} vs. V_{gs} for V_{ds}=0.6 V and temperature variation from Tem=100 K to 500 K with steps of 100 K: logarithmic scale

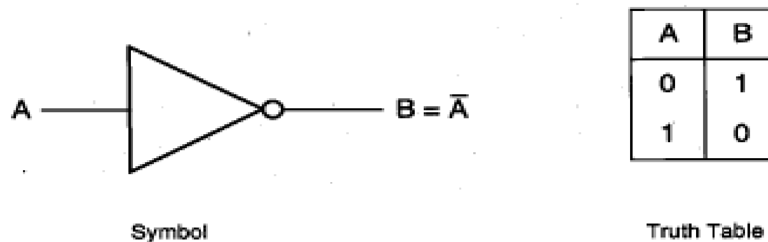
4.3 Application of the CNTFET to Digital and Analog circuits

We have analyzed dependency of the I-V characteristics on different parameters in section 4.2. In order to verify the versatility of the proposed model, we have employed it to design both digital and analog circuits. In all transient simulations, we have considered CNTFETs with default parameters

stated at the beginning of section 4.2. The first circuit demonstrated is inverter circuit which is basic digital circuit and the other circuit demonstrated in this thesis is phase shift oscillator.

4.3.1 Inverter circuit

The inverter is the most fundamental logic gate that performs a Boolean operation on a single input variable [54]. The inverter design forms a significant basis for digital circuit design. The basic principles employed in the design and analysis of inverters can be directly applied to more complex logic circuits, such as NAND and NOR gates, as well. Therefore in this thesis we demonstrate only MOS inverters. The logic symbol and the truth table of the ideal inverter are shown in Figure 4.15.



A	B
0	1
1	0

Figure 4.15 Logic symbol and truth table of the inverter is shown [54].

Common types of inverters include resistive-Load which uses only one n-type transistor and one resistor; and CMOS -inverter, which uses both n- and p-type transistors per inverter circuit. Both circuits are built with our CNTFET model. The circuits are simulated for their functionality and characteristics and results are presented.

4.3.1.1 Resistive-Load Inverter

The basic structure of the resistive-load inverter circuit consists n-type driver transistor and a series load resistance as shown in Figure 4.16. The principle of operation of the circuit is as follows. For a logic low i.e., for input voltage less than threshold, the n-type CNTFET transistor is in OFF state and the transistor does not conduct current. This means there is no current through the load resistor which in turn means no voltage drop across load resistor. In addition, V_{dd} is seen across the capacitor. For logic high i.e., for input voltage greater than threshold, the n-type CNTFET transistor is in ON state and I_{on} is through resistive load this means there is voltage drop across resistor of magnitude equal to I_{on}*R_L. And the voltage across the capacitor is V_{dd}-I_{on}*R_L which is the out put

voltage and very low compared to V_{dd}. For DC characteristic of Resistive load inverter we can write out put voltage as:

$$V_{out} = V_{dd} - I_{ds} * R_L \tag{4.8}$$

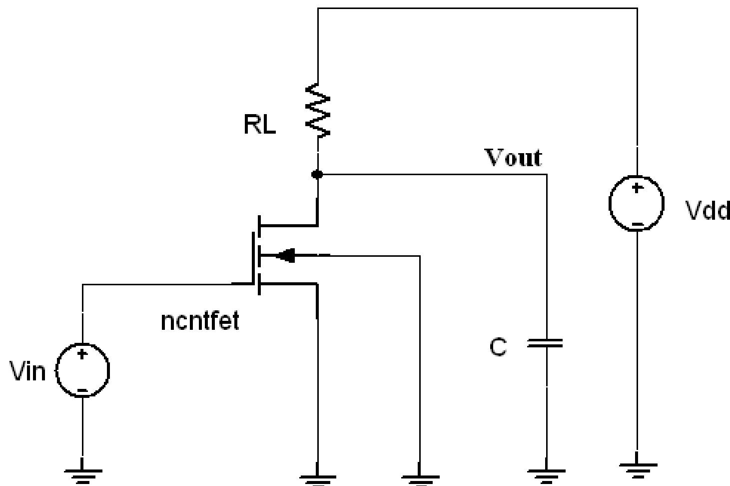


Figure 4.16 Resistive-load inverter circuit

Hence, when off state I_{ds} almost zero and V_{out}=V_{dd} and when on state I_{ds}=I_{on} and V_{out} almost zero. Figure 4.17 shows the voltage transfer characteristics (VTC) of resistive load inverter. We discuss taking primary design parameters i.e., output High voltage (V_{OH}) and Output low voltages (V_{OL}).

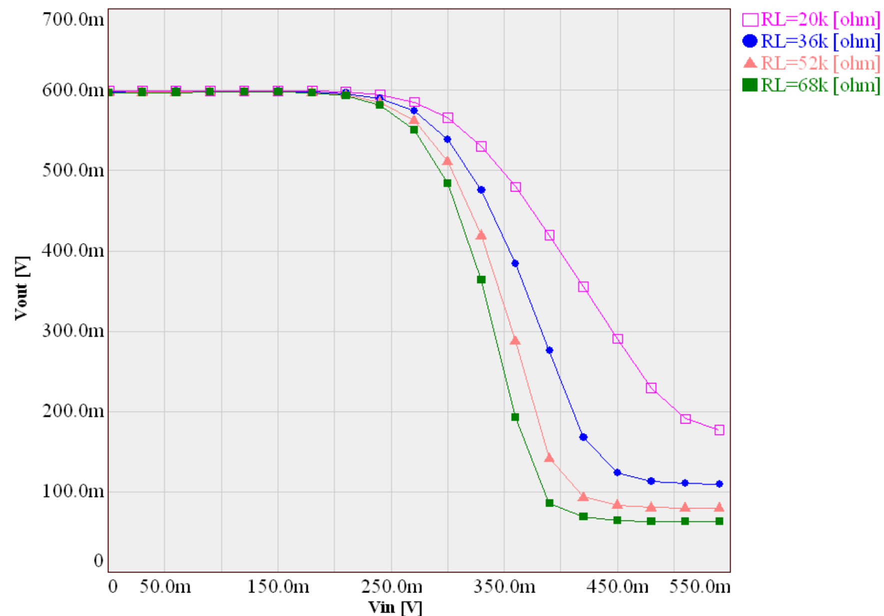


Figure 4.17 Voltage transfer characteristics of the resistive-load inverter, for different values load resistance.

From equation (4.8) it is clear that V_{OH} is determined primarily by the power supply voltage, V_{dd}. And V_{OL} receives more attention. Figure 4.17 shows the VTC of a resistive-load inverter for different values of R_L. Note that for larger R_L values, the output low voltage V_{OL} i.e. when $I_{ds}= I_{on}$, becomes smaller and that the shape of the VTC approaches that of the ideal inverter, with very large transition slope as shown in Figure 4.17 for R_L=68 kΩ. Achieving larger R_L values in a design, however, may involve other trade-offs with the area and the power consumption of the circuit [54].

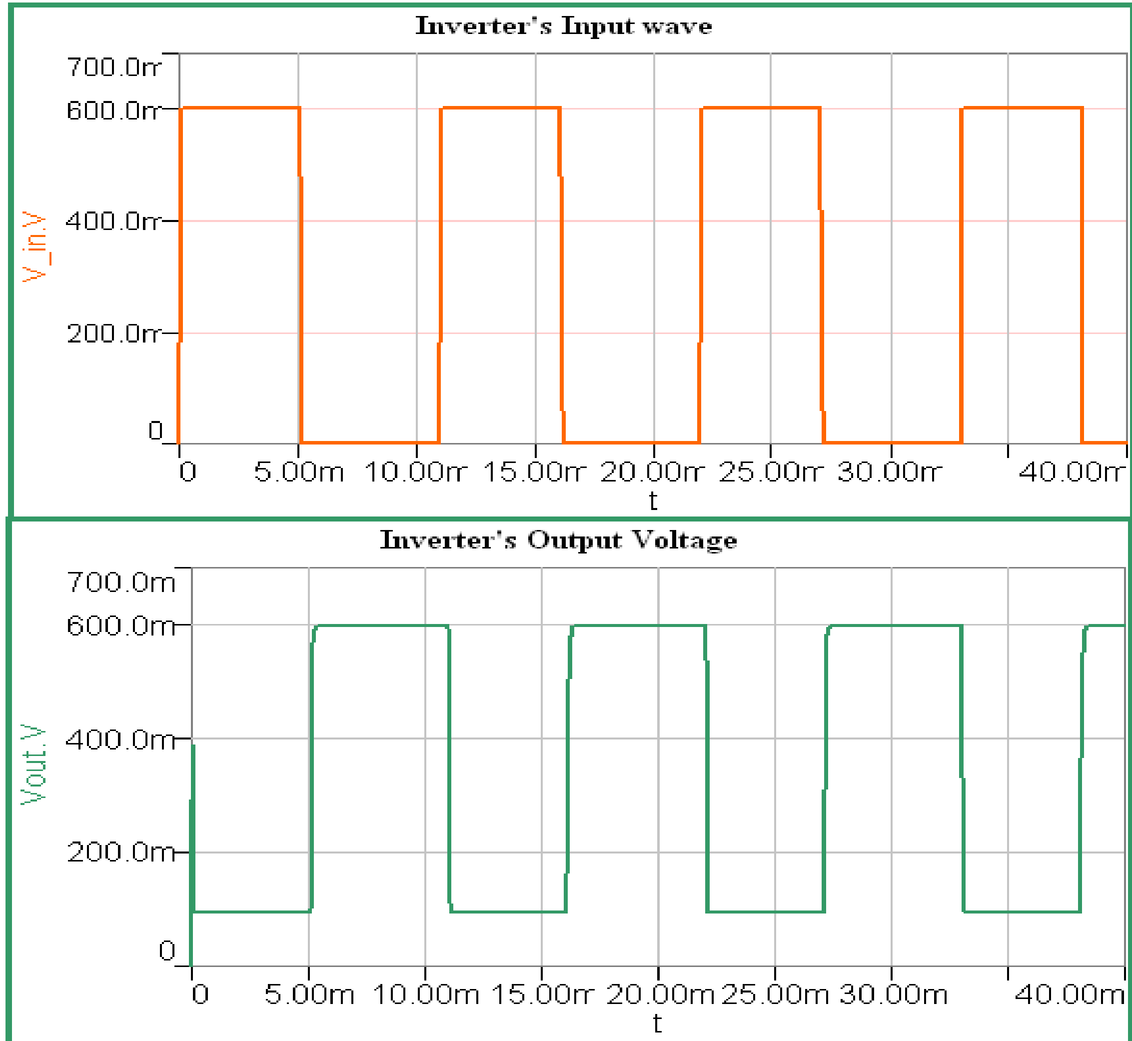


Figure 4.18 Result of a 40 ms transient simulation to validate the behavior of the CNTFET-based load resistive inverter.

Figure 4.18 shows result of 40 ms transient simulation that allowed validating the behavior of the CNTFET-based resistive load inverter. Note that from both Figures (4-17 and 4-18) V_{OL} is never zero (minimum ≈90 mV) which show there is some power consumption.

4.3.1.2 CMOS-inverter

Now, we will turn our attention to a radically different inverter structure, which consists of an nCNTFET transistor and pCNTFET transistor, operating in complementary mode shown in Figure 4.19. This configuration is called Complementary MOS (CMOS).

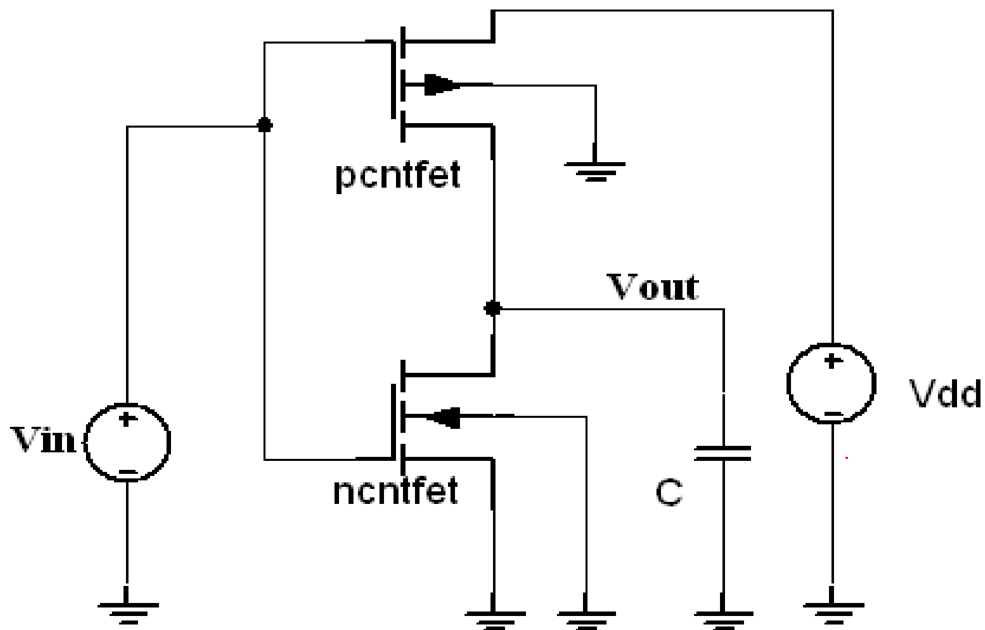


Figure 4.19 CMOS inverter circuit capacitance C=1.0 aF

The circuit topology is complementary push-pull in the sense that for high input, the nCNTFET transistor drives (pulls down) the output node to the ground while the pCNTFET transistor acts as the load, and for low input the pCNTFET transistor drives (pulls up) the output node to V_{dd} while the nCNTFET transistor acts as the load and both devices contribute equally to the circuit operation characteristics.

The CMOS inverter has two important advantages over resistive load inverter. The first and the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually. The other advantages of the CMOS configuration are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{dd}, as shown in Figure 4.20 and that the VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter

resembles that of an ideal inverter. In addition, from Figure 0.20 we see that the output voltage swing fully between 0 V and V_{dd} in about 7.0 ps which is very nice switching behavior.

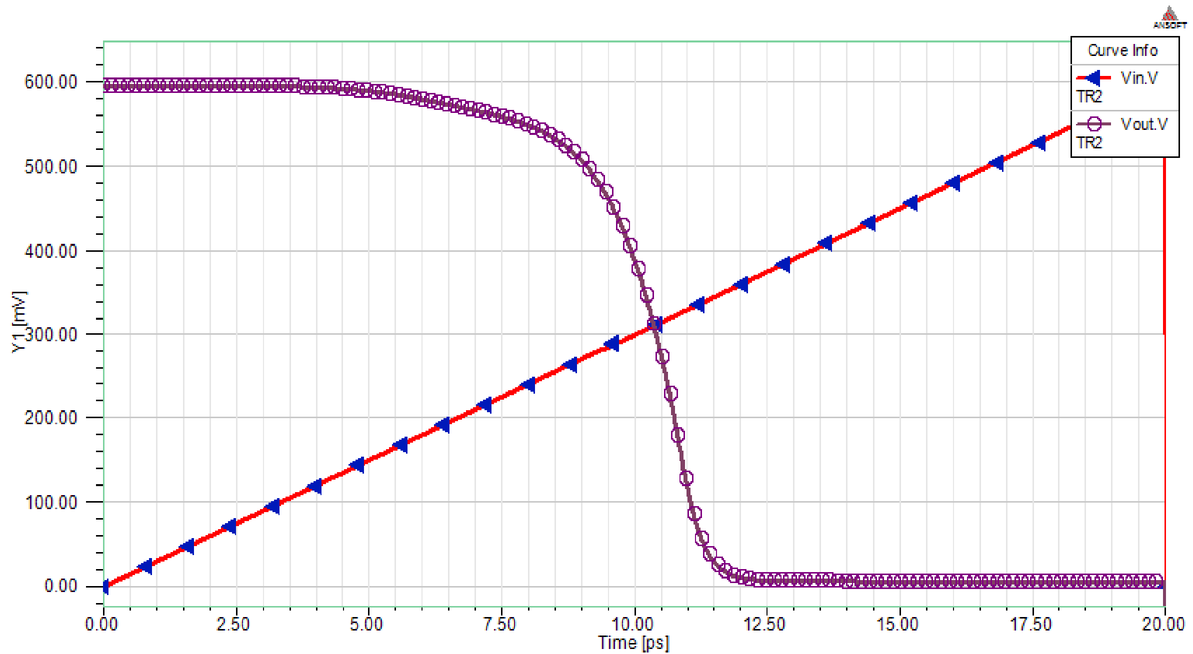


Figure 4.20 Voltage transfer characteristics of the CMOS inverter; shows steep transition and a full output voltage swing between 0 V and V_{dd}. Input voltage is ramp i.e. it increase linearly with time.

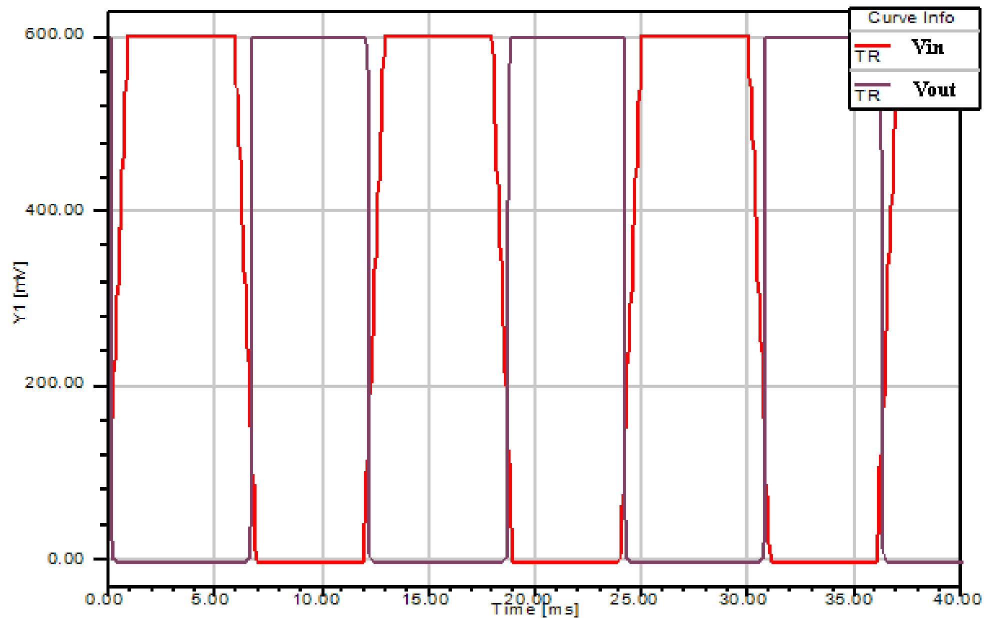


Figure 4.21 Result of a 40 ms transient simulation to validate the behavior of the CNTFET-based CMOS inverter.

4.3.2 Phase shift oscillator

Oscillators convert dc power to ac power. They provide the ac signal at the specified frequency, which is then amplified, modulated (with base band signal), and transmitted through an antenna [55]. They can also be used to down-convert the received signals to lower frequencies, where they can be decoded easily. These applications make oscillator basic analog circuit. Phase shift oscillator is a common type of oscillator. Hence, to see the application of the CNTFET model developed we choose phase shift oscillator circuits.

A phase-shift oscillator is shown in Figure 4.22. It includes three identical RC networks. Each stage provides a – 60° phase shift, resulting in the required -180° total phase shift. To achieve oscillation, the loop gain must satisfy the oscillation criterion: the phase shift must be -180° when the gain is one (0 dB).

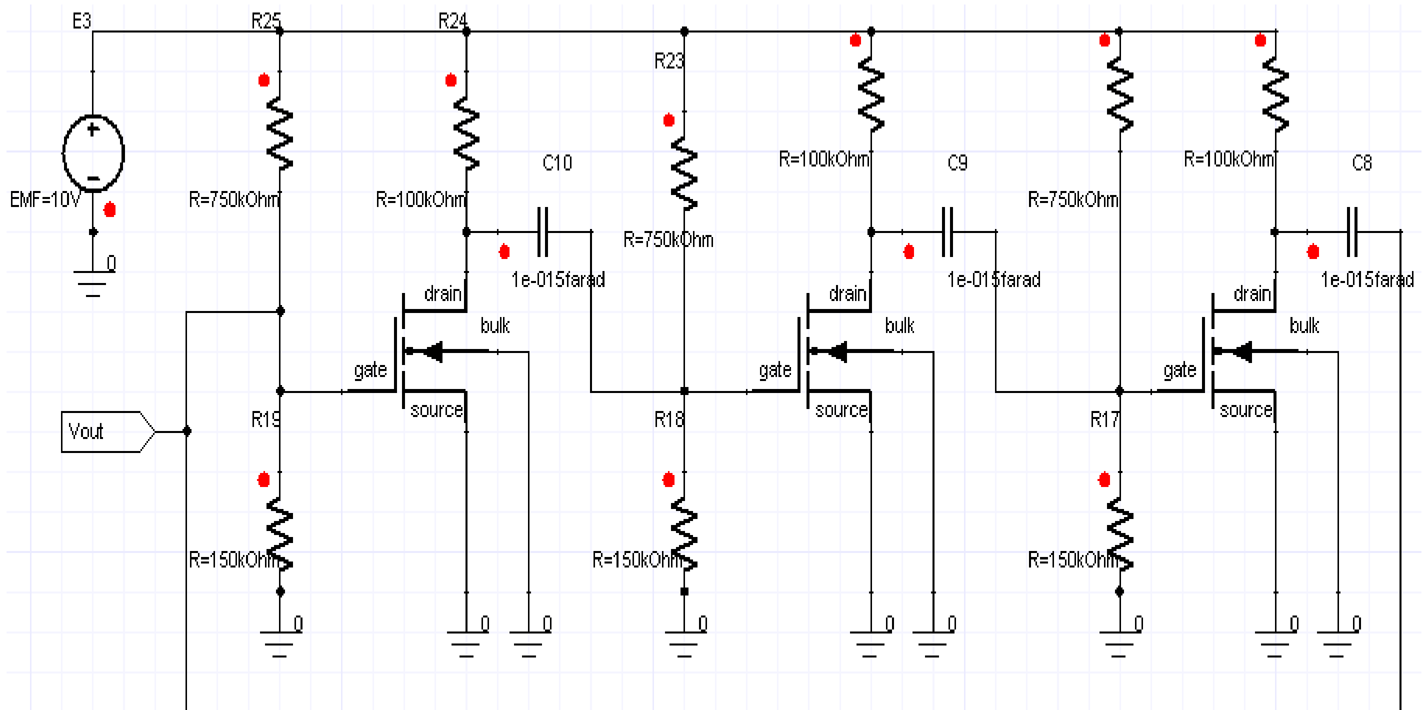


Figure 4.22 Phase-shift oscillator consisting of three nCNTFET

Figure 4-23 shows the output voltage analyzed for 80 ns. Frequency of about 270 MHz can be easily extracted output wave form.

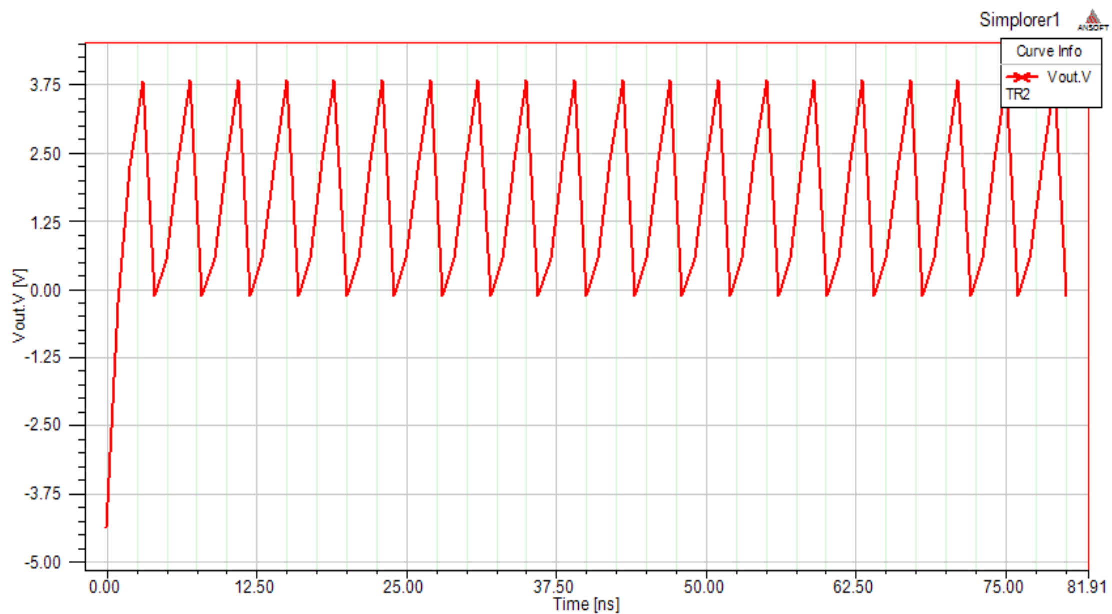


Figure 4.23 Transient Analyzed Simulation result of voltage for the phase-shift oscillator which is taken at the gate of first nCNTFET; the frequency of oscillation is around 270 MHz

CHAPTER 5

CONCLUSION AND FUTURE WORK

This chapter concludes the entire project thesis and propose/recommend some future work to make this area of research more complete and interesting.

5.1 Conclusion

The purposes of this thesis were to study electronic properties of CNTs, to model I-V characteristics of MOSFET-like CNTFET and finally to validate the model by constructing circuits. The main objectives are achieved. Basic electronic properties of CNTs are studied. Energy band structure, density of state, carrier density, carrier velocity and effective mass are investigated. A fully analytical model of MOSFET-like CNTFET is developed. The model requires no iteration or numerical simulation and thus can be used for circuit-level simulation. The model developed is unique in that it is fully analytical model that considered electron-phonon scattering effects, BTBT effects and VHDL-AMS implemented. Various parameters such as gate insulator thickness, gate insulator dielectric constant, diameter, channel length and temperature are varied to see the performance dependency. From the simulation results:

- Reducing insulator thickness improves performance significantly.
- Increasing dielectric constant of gate insulator also improves performance. However, increasing dielectric constant will not always improve performance constantly. From Figure 4.11, for example, using insulator with dielectric constant of 80 (TiO_2) rather than using insulator with dielectric constant of 10 ($HfSiO_4$) improves the on-current by only about two times.
- With uniformly doped source/drain, channel length scaling hurts I_{on}/I_{off} ratio due to BTBT effect.
- Higher temperature degrades performance.
- Threshold voltage and diameter are inversely related.

Finally, using our VHDL-AMS model we constructed circuits. Resistive-Load inverter, CMOS inverter and phase shift oscillator circuits are constructed, simulated and analyzed.

5.2 Future Work

Further improvements to the model implemented in this thesis, in order to improve the accuracy, to make more complete and interesting, may include:

- Parasitic capacitances between gate and source, gate and drain, gate and substrate, drain and substrate, and source and substrate can be incorporated.
- The model developed is based on simplified band structure which restricts the use of this model for the applications that requires a high power supply (>>1.0 eV). Using a more accurate band structure model can avoid this problem at the cost of longer run time.
- To model and predict performance of CNT-based electronics (all-CNT electronic circuit), the modeling of CNT interconnects (global), in addition to the CNTFET device model, is important.
- The resistance of heavily doped CNT source/drain extension also degrades the on-current. One way to further improve CNTFET circuit performance is to use metallic CNTs and MWCNTs as local interconnect. In addition to modeling metallic CNTs and MWCNTs, modeling of junctions between dissimilar tubes (e.g. metallic interconnect and semiconducting channel) is important.
- In this thesis the model developed was only for a channel consisting of only one semiconducting CNT. However, if higher current carrying capacity is needed we can use multiple semiconducting CNTs at a single gate. Hence, a compact modeling of such kind transistor is important.
- The semiconducting CNT used in our model was defect free. However, defects are likely in real CNTFET. Modeling effects of CNT defects on over all device performance and device reliability is important.
- CNTFET is only one application of CNTs. It is important to look into other applications such as optoelectronics and biosensors.

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APPENDICES

A-1 VHDL-AMS code for physical constants used frequently (Package)

```
PACKAGE physical_constants IS
-------- Some physical constants-----------------
     CONSTANT a: REAL: = 2.49e-10; --------lattice constant
     CONSTANT pi: REAL: = 3.14159265358979323846264338327 95;
     CONSTANT e: REAL: = 1.6e-19; ------electron charge
     CONSTANT eo: REAL: = 8.854E-12;--dielectrics of constant of -
     -free space or vacuum
     CONSTANT h: REAL: = 6.626E-34; ------Plank's constant
     CONSTANT hbar: REAL: = 1.05E-34;--reduced plank's constant
     hbar: =h/ (2*pi)
     CONSTANT m0: REAL: = 9.11E-31; ----rest mass of electron
     CONSTANT KB: REAL: = 1.380E-23; ----Boltzmann constant
     CONSTANT Vpi: REAL: = 3.033*1.6E-19;
     CONSTANT hwo: REAL: =0.16*1.6e-19;--minimum energy require --
     for phonon scattering to occur this value varies from ----
     0.16-0.2eV
END physical_constants;
```

A-2 VHDL-AMS code for channel potential calculation (Package)

```
LIBRARY ieee;
USE  ieee.math_real.ALL;
USE  ieee.electrical_systems.ALL;
LIBRARY work;
USE work.physical_constants.all;
PACKAGE channel_potential IS
     FUNCTION Vchannel(vg,vd,vs,tins,k1,k2,eg,dcnt,Tem,lg: real)
     RETURN REAL;
     FUNCTION Ct(vg,vd,vs,tins,k1,k2,dcnt,Tem,lg: real) RETURN
     REAL;
```

```
END channel_potential;
PACKAGE BODY channel_potential IS
     CONSTANT w: REAL: = 0.30;
     CONSTANT Aa: REAL: = 0.63;
     FUNCTION Vchannel(vg,vd,vs,tins,k1,k2,eg,dcnt,Tem,lg: real)
     RETURN REAL IS
          VARIABLE mEg, co, c1, No, Cins, ss, tt, vch, l1,
          archcosh, mm: REAL;
          VARIABLE z1, z2, z3, m1, m2, m3: REAL;
     BEGIN
          --Dcnt:=0.249e-9*sqrt(n*n+m*m+n*m)/pi;
          l1:=(k1-k2)/(k1+k2);
          mm:=2.0*tins/Dcnt;
          archcosh:=log(mm+sqrt(mm*mm-1.0));
          --Eg:=0.426*2.0*1.6e-19/(Dcnt*1.0e9);
          No:=8.0/a*((Eg+KB*Tem)/(Eg+4.0*vpi))*sqrt(KB*Tem/(3.0*pi
          *Eg));
          Cins:=2.0*pi*k1*eo/ (archcosh+l1*
          log((2.0*tins+2.0*Dcnt)/ (3.0*Dcnt)));
          z1:=2.0*e*e*No/(2.0*Cins*KB*Tem);
          z2:=e/(KB*Tem);
          z3:=Eg/(2.0*KB*Tem);
          mEg:=(0.250/e)*Eg;
          m1:=(Aa*exp(mEg*z2 - z3) + 1.0);
          m2:=((z2*exp(mEg*z2 - z3))/ (m1*m1) - (2.0*Aa*z2*
          exp(2.0*mEg*z2 - 2.0*z3))/ (m1*m1*m1));
          m3:=1.0 - (z1*exp(mEg*z2 - z3))/ (m1*m1) ;
          co:=z1*mEg*m2+m3;
          c1:=z1*m2;
          ss:=c1/co;
          tt:=1.0/co;
          vch:=vg/(ss*vg+tt);
```

```
    RETURN vch;
    END FUNCTION Vchannel;
    FUNCTION Ct(vg,vd,vs,tins,k1,k2,dcnt,Tem,lg: real) RETURN
    REAL IS
         VARIABLE kk, kj, Cins, No, Eg, cq, ctotal, l1, mm, vch,
         archcosh: REAL;
    BEGIN
         --Dcnt:=0.249e-9*sqrt(n*n+m*m+n*m)/pi;
         l1:=(k1-k2)/(k1+k2);
         mm:=2.0*tins/Dcnt;
         Cins:=2.0*pi*k1*eo/ (archcosh+l1*
         log((2.0*tins+2.0*Dcnt)/(3.0*Dcnt)));
         Eg:=0.89*1.6e-19/(Dcnt*1.0e9); No:=8.0/a*((Eg +
         KB*Tem)/(Eg+4.0*vpi))*sqrt(KB*Tem/(3.0*pi*Eg));
         vch:=Vchannel(vg,vd,vs,tins,k1,k2,eg,dcnt,Tem,lg);
         kk:=(2.0*e*vch-Eg)/(2.0*KB*Tem);
         kj:=1.0+0.63*exp(kk);
         cq:=e*e*No*exp(kk)/(KB*Tem*kj*kj);
         ctotal:=cq*cins/(cq+cins);
    RETURN ctotal;
    end function ct;
END channel_potential;
```

A-3 VHDL-AMS code for calculation of current contributed by 1st subband (Package).

```
LIBRARY ieee;
USE  ieee.math_real.ALL;
USE  ieee.electrical_systems.ALL;
LIBRARY work;
USE work.physical_constants.ALL;
USE work.channel_potential.ALL;
PACKAGE Ids_1 IS
```

```
      FUNCTION I_ds(vd,vs,vg,dcnt,tins,k1,k2,Tem,lg,Ef:REAL) RETURN
      REAL;
   END Ids_1;
   PACKAGE BODY Ids_1 IS
      FUNCTION I_ds(vd,vs,vg,dcnt,tins,k1,k2,Tem,lg,Ef:REAL) RETURN
      REAL IS
         VARIABLE Tbtbt, Ibtbt, lrelax, Ff, meff, kp, Io, vch,
         vgs, vds, Eg, Id, Id_thermo, TpS, TpD, ls, ld, fas, fos,
         fad, fod, T:REAL;
         VARIABLE lap_eff, lap_300, lop_300, lop_eff, l_eff_low,
         l_eff_high, T_low, vgg, T_high: REAL;
      BEGIN
         Io:=4.0*e*KB*Tem/h;
         Eg:=0.89*1.6e-19/(Dcnt*1.0e9);
         lop_300:=15.0*Dcnt;
         lap_300:=651.0*Dcnt;
         lap_eff:=300.0/Tem*lap_300/sqrt(1.0+ Eg/(1.83*KB*Tem));
         lop_eff:=lop_300;
         l_eff_low:=lap_eff;
         T_low:=l_eff_low/(l_eff_low+lg);
         l_eff_high:=lap_eff*lop_eff/(lop_eff+lap_eff);
         T_high:=l_eff_high/(l_eff_high+lg);
         --Dcnt:=0.249e-9*sqrt(n*n+m*m+n*m)/pi;
         if vg<0.0 then
            vgg:=0.0;
         else
            vgg:=vg;
         end if;
         vch:=Vchannel1(vgg,vd,vs,tins,k1,k2,eg,dcnt,Tem,lg);
         vds:=vd-vs;
         kp:=2.0/(3.0*Dcnt);
         meff:=2.0*hbar*hbar*kp/(a*vpi*sqrt(3.0));
```

```
            lrelax:=lg/2.0;
            Ff:=abs(e*(Vds+Ef/e-vch)/lrelax);
            Tbtbt:=exp((-pi*Eg*sqrt(Eg*meff))/(8.0*hbar*Ff));
            if e*vds>Eg then
                 Ibtbt:=Io*Tbtbt*(log(1.0+exp((2.0*e*vds-2.0*Ef-
                 Eg)/(2.0*KB*Tem)))-log(1.0+exp((-2.0*Ef+Eg)/
                 (2.0*KB*Tem))));
            else
                 Ibtbt:=0.0;
            end if;
            Id_thermo:=Io*(T_low*(log(1.0+exp((e*vch+ef-
            Eg/2.0)/(kb*Tem)))-log(1.0+exp((e*vch+ef-Eg/2.0-e*vds)
            /(kb*Tem))))+(T_high-T_low) * (log(1.0+ exp((e*vch+ef-
            Eg/2.0-hwo)/(kb*Tem)))-log(1.0+ exp((e*vch+ef-hwo-e*vds-
            Eg/2.0)/(kb*Tem)))));
            Id:=Ibtbt+Id_thermo;
            RETURN Id;
       END function I_ds;
END Ids_1;
```

A-4 VHDL-AMS code for calculation of current contributed by 2nd subband (Package).

```
LIBRARY ieee;
USE  ieee.math_real.ALL;
USE  ieee.electrical_systems.ALL;
LIBRARY work;
USE work.physical_constants.all;
USE work.channel_potential1.all;
PACKAGE ids_2 IS
     FUNCTION I_ds_2(vd,vs,vg,dcnt,tins,k1,k2,Tem,lg,Ef:real)
     return real;
END ids_2;
PACKAGE BODY ids_2 IS
```

```
FUNCTION I_ds_2(vd,vs,vg,dcnt,tins,k1,k2,Tem,lg,Ef:real)
return real is
     variable Tbtbt, Ibtbt, lrelax, Ff, meff, kp, Io, vch,
     vgs, vds, Eg, Id, Id_thermo, TpS, TpD, ls, ld, fas, fos,
     fad, fod, T:real;
     variable lap_eff,lap_300,lop_300,lop_eff, l_eff_low,
     l_eff_high, T_low,T_high:real;
     begin
          Io:=4.0*e*KB*Tem/h;
          Eg:=2.0*0.89*1.6e-19/(Dcnt*1.0e9);
          lop_300:=15.0*Dcnt;
          lap_300:=651.0*Dcnt;
          lap_eff:=300.0/Tem*lap_300/sqrt(1.0+
          Eg/(1.83*KB*Tem));
          lop_eff:=lop_300;
          l_eff_low:=lap_eff;
          T_low:=l_eff_low/(l_eff_low+lg);
          l_eff_high:=lap_eff*lop_eff/(lop_eff+lap_eff);
          T_high:=l_eff_high/(l_eff_high+lg);
     --   Dcnt:=0.249e-9*sqrt(n*n+m*m+n*m)/pi;
          vch:=Vchannel1(vg,vd,vs,tins,k1,k2,
          eg,dcnt,Tem,lg);
          vds:=vd-vs;
          kp:=4.0/(3.0*Dcnt);
          meff:=2.0*hbar*hbar*kp/(a*vpi*sqrt(3.0));
          lrelax:=lg/2.0;
          Ff:=abs(e*(Vds+Ef/e-vch)/lrelax);
          Tbtbt:=exp((-pi*Eg*sqrt(Eg*meff))/(8.0*hbar*Ff));
          if e*vds>Eg then
               Ibtbt:=Io*Tbtbt*(log(1.0+exp((2.0*e*vds-
               2.0*Ef-Eg) /(2.0*KB*Tem)))-log(1.0+exp((-
               2.0*Ef+Eg)/ (2.0*KB*Tem))));
```

```
          else
               Ibtbt:=0.0;
          end if;
          Id_thermo:=Io*(T_low*(log(1.0+exp((e*vch+ef-Eg/2.0)
          / (kb*Tem))) -log(1.0+exp((e*vch+ef-Eg/2.0-e*vds)/
          (kb*Tem))))+(T_high-T_low)* (log(1.0+exp((e*vch+ef-
          Eg/2.0-hwo)/ (kb*Tem)))-log(1.0+exp((e*vch+ef-hwo-
          e*vds-Eg/2.0)/(kb*Tem)))));
          Id:=Ibtbt+Id_thermo;
     return Id;
  END function I_ds_2;
END ids_2;
```

A-5 VHDL-AMS code for n-type MOSFET like CNTFET (Model)

```
---------- VHDL-AMS MODEL nCNTFET ----------
LIBRARY IEEE;
USE IEEE.math_real.all;
USE IEEE.electrical_systems.all;
LIBRARY work;
USE work.Ids_1.all;
USE work.Ids_2.all;
USE work.channel_potential.all;
USE work.physical_constants.all;
---------- ENTITY DECLARATION nCNTFET ----------
ENTITY    nCNTFET IS
     GENERIC (--MODEL PARAMETERS
          Lg: real: =2.0E-8;--channel length or gate length
          Ls: real: =1.0E-8;--doped source side length
          Ld: real: =1.0E-8;--doped drain side length
          tins:real:=8.0E-9;--Gate to channel insulator thickness
```

```
          k1:real:=16.0; --dielectric constant of gate to channel
                           insulator
          k2:real:=3.9; --dielectric constant of channel to
                           substrate insulator
          --n   : real: = 19.0;--chiral number
          --m   : real: = 0.0;--chiral number
          Dcnt: real: =1.5e-9;
          Sc: real:=0.0;--source connectivity which is 0.0 if
                         source connected to doped CNT
          Dc: real:=0.0;--source connectivity which is 0.0 if
                         source connected to doped CNT
          Tem: real := 300.0;--Temperature
          Vfb: real:= 0.0;-- flat band voltage
          Ef :real :=0.0);----Fermi level of doped regions
          PORT (TERMINAL Drain, Gate, Source, Bulk: electrical);
END ENTITY nCNTFET;
---------- ARCHITECTURE DECLARATION arch_nCNTFET ----------
ARCHITECTURE arch_nCNTFET OF nCNTFET IS
     TERMINAL D, S: ELECTRICAL;
     QUANTITY Vdrain ACROSS drain TO bulk;
     QUANTITY Vgate ACROSS gate TO bulk;
     QUANTITY Vsource ACROSS source TO bulk;
     QUANTITY Vdr ACROSS D TO bulk;
     QUANTITY Vso ACROSS S TO bulk;
     QUANTITY Irs THROUGH S TO source;
     QUANTITY Ird THROUGH drain TO D;
     QUANTITY Ids THROUGH d TO s;
     QUANTITY Igs through gate to S;
     QUANTITY Qg: real: =0.0;
     CONSTANT Leff: real: =20.0E-9;
     CONSTANT Qg: real: =6.471E3;
     CONSTANT Rs: real: =Rq*Sc+Rq*Ls/Leff;
```

```
      CONSTANT Rd: real: =Rq*Dc+Rq*Ld/Leff;
      CONSTANT roff: real: =110.0e6;
BEGIN
      brk1: break Vgate=>0.0, Vdrain=>0.0, Vsource=>0.0;
      IF (vdrain>=0.0 and vgate>=0.0) USE
            Ird== (Vdrain-Vdr)/Rd;
            Irs== (Vso-Vsource)/Rs;
            Ids==I_ds(Vdr,Vso,Vgate-vfb,dcnt,tins,k1, k2,Tem, lg,
            Ef) +I_ds_2(Vdr,Vso,Vgate-vfb,dcnt,tins
            ,k1,k2,Tem,lg,Ef);
      ELSE
            Ird== (Vdrain-Vdr)/Rd;
            Irs== (Vso-Vsource)/Rs;
            Ids== (vdr - vso)/roff;
      END USE;
      brk2: break Vgate=>0.0, Vdr=>0.0, Vso=>0.0;
      IF (domain = quiescent domain) USE
            Qg==Ct(vgate-vfb,vdr,vso,tins,k1,k2,dcnt,Tem,lg)*
            (Vgate-Vso);
            Igs==0.0;
      ELSE
            Qg==Ct(vgate-vfb,vdr,vso,tins,k1,k2,dcnt,Tem,lg)*
            (Vgate-Vso);
            Igs==Qg'dot;
      END USE;
END ARCHITECTURE arch_nCNTFET;
---------- END VHDL-AMS MODEL nCNTFET ----------
```

A-6 VHDL-AMS code for p-type MOSFET like CNTFET (Model)

```
---------- VHDL-AMS MODEL pCNTFET ----------

LIBRARY IEEE;
```

```
USE IEEE.math_real.all;
USE IEEE.electrical_systems.all;
LIBRARY work;
USE work.Ids_1.all;
USE work.Ids_2.all;
USE work.channel_potential.all;
USE work.physical_constants.all;
---------- ENTITY DECLARATION pCNTFET ----------
ENTITY    pCNTFET IS
     GENERIC (--MODEL PARAMETERS
          Lg: real:=2.0E-8;--channel length or gate length
          Ls: real:=1.0E-8;--doped source side length
          Ld: real:=1.0E-8;--doped drain side length
          tins: real:=8.0E-9;--Gate to channel insulator thickness
          k1: real:=16.0; --dielectric constant of gate to channel
                                 insulator
          k2: real:=3.9; --dielectric constant of channel to
                                 substrate insulator
          --n   : real := 19.0;--chiral number
          --m   : real := 0.0;--chiral number
          Dcnt: real:=1.5e-9;
          Sc: real:=0.0;--source connectivity which is 0.0 if
                                 source connected to doped CNT
          Dc: real:=0.0;--source connectivity which is 0.0 if
                                 source connected to doped CNT
          Tem: real := 300.0;--Temperature
          Vfb: real:= 0.0;-- flat band voltage
          Ef: Real: =0.0); ----Fermi level of doped regions
          PORT (TERMINAL Drain, Gate, Source, Bulk: electrical);
END ENTITY pCNTFET;
---------- ARCHITECTURE DECLARATION arch_pCNTFET ----------
ARCHITECTURE arch_pCNTFET OF pCNTFET IS
```

```
    TERMINAL D,S: electrical;
    QUANTITY Vdrain across drain to bulk;
    QUANTITY Vgate across gate to bulk;
    QUANTITY Vsource across source to bulk;
    QUANTITY Vdr across D to bulk;
    QUANTITY Vso across S to bulk;
    QUANTITY Irs through S to source;
    QUANTITY Ird through drain to D;
    QUANTITY Ids through d to s;
    QUANTITY Igs through gate to S;
    QUANTITY Qg:real:=0.0;
    CONSTANT Leff:real:=20.0E-9;
    CONSTANT Rq:real:=6.471E3;
    CONSTANT Rs:real:=Rq*Sc+Rq*Ls/Leff;
    CONSTANT Rd:real:=Rq*Dc+Rq*Ld/Leff;
    CONSTANT roff: real: =110.0e6;
BEGIN
    brk1: break Vgate=>0.0, Vdrain=>0.0, Vsource=>0.0;
    IF (vdrain>=0.0 and vgate>=0.0) USE
        Ird== (Vdrain-Vdr)/Rd;
        Irs== (Vso-Vsource)/Rs;
        Ids==I_ds(-Vdr,-Vso,- Vgate+vfb,dcnt,tins,k1,k2, Tem,
        lg, Ef) +I_ds_2(-Vdr, -Vso, -Vgate +vfb, dcnt, tins, k1,
        k2,Tem,lg,Ef);
    ELSE
        Ird==(Vdrain-Vdr)/Rd;
        Irs== (Vso-Vsource)/Rs;
        Ids== (vdr-vso)/roff;
    END USE;
    brk2: break Vgate=>0.0, Vdr=>0.0, Vso=>0.0;
    IF (domain = quiescent_domain) USE
```

```
        Qg==Ct (-vgate + vfb,-vdr,-vso, tins, k1, k2, dcnt, Tem,
        lg)* (Vgate-Vso);
        Igs==0.0;
    ELSE
        Qg==Ct (-vgate + vfb,-vdr,-vso, tins, k1, k2, dcnt, Tem,
        lg)*(Vgate-Vso);
        Igs==Qg'dot;
    END USE;
END ARCHITECTURE arch_pCNTFET;
---------- END VHDLAMS MODEL pCNTFET ----------
```