DESIGN OF AN IMPROVED ADPLL FOR DUAL BAND GSM

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DECLARATION

I, the undersigned, declare that this thesis work is my original work, has not been presented for a degree in this or any other universities, and all sources of materials used for the thesis work have been fully acknowledged.

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This thesis has been submitted with my approval as a university advisor.

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ABSTRACT

DESIGN OF AN IMPROVED ADPLL FOR DUAL BAND GSM

Gosa Demisie,
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All Digital Phase Locked Loop are widely used frequency synthesizers in different radio communication systems. To use analog phase locked loop in different processes is difficult due to its process sensitivity. In conventional all digital phase locked loop all blocks are defined to be digital at both input and output level. In normal all digital phase locked loop the analog parts degrade the performance of the whole system related to frequency of operation.

The new ADPLL architecture, which is the digital counter part of conventional CPPLL, is designed by discritizing conventional charge pump phase locked loop. It is designed using digital blocks in the new architecture, isolation rings and bulky loop filter components are replaced, and hence the system can become area efficient, consumes less power and low jitter. The digital block used in the design in place of analog charge pump help the application to be free of analog charge pump pitfalls like charge pump mismatch, leakage, thermal noise, aging and drift. Moreover, using the new architecture the system is made stable and hence more portable and robust operation. Higher rate clocks and huge processing time problems at the controller end is reduced using digital block used in the architecture.

In a nutshell the design of integrated circuit is targeted for 900 MHz and 1800 MHz center frequencies with tuning range of 200 MHz and is done in UMC 130 nm technology. It consumes an average current of 13mA and applicable for 1.2V supply voltage. The chip area is less than $0.12mm^2$ and the average settling time is 3.55 usec.

Keywords: *Charge pump phase locked loop, All digital phase Locked loop, discritization technique, dual-band GSM, new architecture, digitally controlled oscillator*

ACKNOWLEDGEMENTS

Designing integrated circuit is not something people living in underdeveloped world would like to do mainly because of the unavailability of resources, facilities, and shortage of expertise. To make matters very challenging, the budget system does not allow us to buy materials online as per given time and the laboratory system we have does not all the facilities needed for work. Getting even the crystal oscillator is challenging neither here nor can we buy them from abroad in a substantial manner.

In spite of all the challenges and the difficulties, the successful completion of this thesis is not a result of merely my efforts, but a combined effort and dedication of several individuals. It is well known that a comprehensive work like this which includes research and design could not be accomplished by merely an individual.

My heartfelt gratitude and thank goes to my advisor Ato Daniel Dilbie, for all the reviews and constructive comments he gave me on my work. My great gratitude goes to my friend Kinde Anlay (PHD student). He was always there to take my orders, to help me the way to sweeten my work and whatever I wanted and send over to me all the materials. I would like to thank my mother who was constantly motivating and forcing me to work hard and finish my thesis in time beside the work burden I have in my office. I would like to thank Dr. Ing. Getachew Alemu for looking my work appropriately in the process and giving constructive comments in the mean time.

I have no space here to mention all the people whom I owe my gratitude, but there are some I couldn't afford to leave out. I want to say how much thankful I am to all AAiT staffs who helped my work into completion one way or the other way for their dedication and their generous experience sharing during the various stages of design, debugging and troubleshooting. Finally I would like to thank my friends Zelalem Tamrat, Eyob Teshome, Kassaye Tafese, Misiker Tadesse and Semere Yohannis, for motivating, and giving constructive feedbacks.

TABLE OF CONTENT

List of Figures

List of Tables

About This Thesis

This document is a formal report of the thesis on Design of an Improved ADPLL for Dual Band GSM Application. The theoretical backgrounds and the physical implementations are described. The results obtained are analyzed and conclusions and inferences are made as appropriate. For more technical details, please refer to the CD ROM attached to this document.

Definitions, Abbreviations, and Acronyms

The following table defines the acronyms and abbreviations used in this document

Term	Definitions
ADPLL	All Digital Phase Locked Loop
CDR	Clock and Data recovery
C_{LSB}	Least Significant Bit capacitor
C_{MSB}	Most significant Bit capacitor
CP	Charge Pump
CPPLL	Charge pump Phase Locked Loop
DCO	Digitally Controlled Oscillator
IC	Integrated Circuit
GSM	Global System for Mobile Communication
LPF	Loop Filter
F_{DCO}	Digitally Controlled Oscillator output Frequency
F_{REF}	Reference clock Frequency

F_{OSC}	Oscillation Frequency
FSCL	Faraday Standard Cell Library
F_{VCO}	Analog voltage controlled oscillator output frequency
GND	Ground
HS	High speed
I_{sink}	Sink current
I_{source}	Source current
LC tank	Inductor capacitor tank
LL	Low leakage
LSB	Least Significant Bit
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
PCELL	Parameterized Cell
PFD	Phase frequency Detector
PLL	Phase Locked Loop
PVT	Process, Voltage and Temperature
RFCMOS	Radio Frequency Complementary Metal Oxide Semiconductor
SoC	System on Chip
SP	Standard Performance
TSPC	True Single Phase Clock

UMC	Unified Microelectronics corporation
VCL	Virtual Capacitor Library
VCO	Voltage Controlled Oscillator
Vcon	Control voltage
V_{DD}	Voltage headroom
VIL	Virtual Inductor Library

Chapter 1

Introduction

1.1. Background

A phase locked loop circuit is used to synchronize an output signal, which is usually generated by an oscillator, with a reference or input signal, in frequency as well as in phase. In the lock state, the difference between the reference and the oscillator output is zero or at least very small. Phase locked loops are found in different electronics applications mainly in communication receivers and transmitters, clock and data recovery circuits, clock synchronization circuits in complex system on chips, and many other applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors or as part of CDRs in hard-disk drivers and digital video disks. They are also used as part of frequency synthesizers which generates a range of output frequencies which are multiples of a given reference input frequency, as shown in [1]

Because a single integrated circuit can provide a complete PLL building block, the technique is mostly used in modern consumer and security electronics devices, with outputs ranging from fraction of a hertz to several gigahertzes. On the basis of their implementation, PLLs are classified into three types, namely, analog, mixed signals and all digital, as shown in [1] and [2]. Conventional charge pump PLLs which are analog in nature, consists of phase and frequency detector, charge pump, loop filter and voltage controlled oscillator, as shown in [2]. Recently all digital phase locked loop have been invented in which all building blocks are defined as digital at input and output level.

In most ADPLLs, the oscillator is controlled by digital commands as opposed to analog tuning voltage. The advantage of having access to intermediate signals in digital form is significant. Fast frequency acquisitions and low phase noise, are among the main advantages can be obtained using digital command in ADPLL. All digital PLL design can improve system-turnaround efficiency during process changes, making it good for system on chip applications.

This research addresses a new architecture driven all digital phase locked loop which is digital counter part of the conventional charge pump phase locked loop. Digital charge pump is introduced here, which completely eradicates the pitfalls of analog phase locked loop like charge pump mismatches, leakage, thermal noise, aging or drift. Unlike the conventional All Digital phase locked loop this design does not require any time to digital converter for the phase detection of input and oscillator frequencies, which generally consists of a long chain of inverters that consume lot of power. All digital blocks of this design work in synchronization with input reference clock, which eliminates the use of sample clock whose frequency is higher than the reference clock. In this design complex digital low pass filters is not used, which generally have tapped delay line like structure.

1.2. Thesis Objective

1.2.1. General objectives

- To design new architecture driven ADPLL integrated circuit for dual-band GSM application.

1.2.2. Specific objectives

- To design digital counter part of charge pump phase locked loop
- Then using the digital counterpart to replace analog components used in conventional ADPLL
- Block level design and simulation
- Integration of blocks
- Layout of the integrated block circuit
- Simulation and result analysis of the integrated block circuit

1.3. Methodology

CPPLL is a mixed signal circuit, only PFD part is digital and the others are analog. To drive completely digital phase locked loop architecture, discretization technique using pulse transformation techniques is used. A completely different ADPLL architecture from CPPLL is driven that is generally different from conventional ADPLL, which requires high rate clock for sampling. In addition, unlike the conventional ADPLL, this design does not require any time to digital conversion for the phase detection of input and oscillator frequencies. This time to digital converters generally consists of a long chain of gates, which consume lot of power. The digital counter part of CPPLL, which has more additional features than conventional ADPLL do have main parts, namely, DCO, PFD and digital controller as main parts.

1.4. Thesis organization

The thesis is organized as follows: chapter two gives a brief introduction of charge pump phase locked loop, the charge pump type we selected for discritization, and its transfer function. Chapter three illustrates descritization of charge pump phase locked loop to get the corresponding architecture. Chapter four gives a brief block level design of Dual band All Digital Phase Locked Loop. Chapter five illustrates design and simulation of synchronized phase frequency detector. Chapter six briefly illustrates design of digital controller. Chapter seven shows the integration of the cumulative All Digital Phase Locked Loop, simulation result and layout for the integrated circuit. Finally, chapter eight shows Conclusion, limitation and future work in order.

Chapter 2

Charge Pump Phase Locked Loop

2. 1. Basic Charge Pump phase locked loop

For complete illustration and understanding of the new architecture, a brief discussion on charge pump phase locked loop is discussed in the following section.

2.1.1. CPPLL Building Blocks

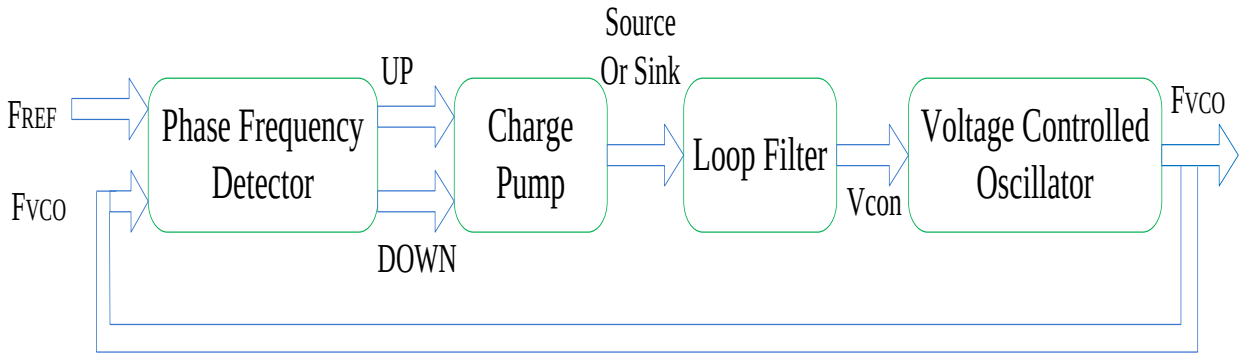

Figure 2.1.Conventional charge pump phase locked loop

The phase/frequency detector used in the charge pump PLL allows the PLL to have a pull-in range that is only limited by the VCO's tuning range. The static phase error is zero between the input reference signal and the feedback signal even if the reference signal is not equal to the center frequency of the voltage controlled oscillator.

The phase/frequency detector compares the input reference signal and the feedback signal to produce two control signals *UP* and *DOWN*. These control signals control how much error current flows into the loop filter. The loop filter consists of a minimum of one capacitor C1 in series with a resistor *R*. The charge pump current charges and discharges the loop filter to

produce the VCO control voltage. The VCO signal is then fed back to the phase/frequency detector. The charge pump PLL uses a digital phase/frequency detector that switches a charge pump's current sources/sinks to charge or discharge the loop filter respectively. The type of PFD used allows for a zero static phase error even when the input reference frequency is not equal to the center frequency of the voltage controlled oscillator.

2.1.2. Phase Frequency Detector

The phase frequency detector is a digital phase/frequency detector with a charge pump output stage. The function of the PFD is to detect the difference in phase and frequency between the reference clock and the output clock. The PFD has two outputs UP and DOWN. The UP output indicates that the reference clock is leading in phase or frequency with respect to the output clock, while the DOWN output indicates that the reference clock is lagging in phase or frequency with respect to the output clock. Both the UP and DOWN outputs are pulses whose widths are proportional to the phase difference and D inputs to the flip-flops are tied high.

The digital phase/frequency detector consists of an AND gate and two resettable D Flip-Flops, one clocked by the reference signal and the other by the output signal. When the two inputs are in phase at the same frequency AND gate resets the flip flops and starts the next turn. The schematic of the phase/frequency detector is shown below, which includes the input clocks, F_{REF} and F_{DCO}, D flip flops and the corresponding outputs.

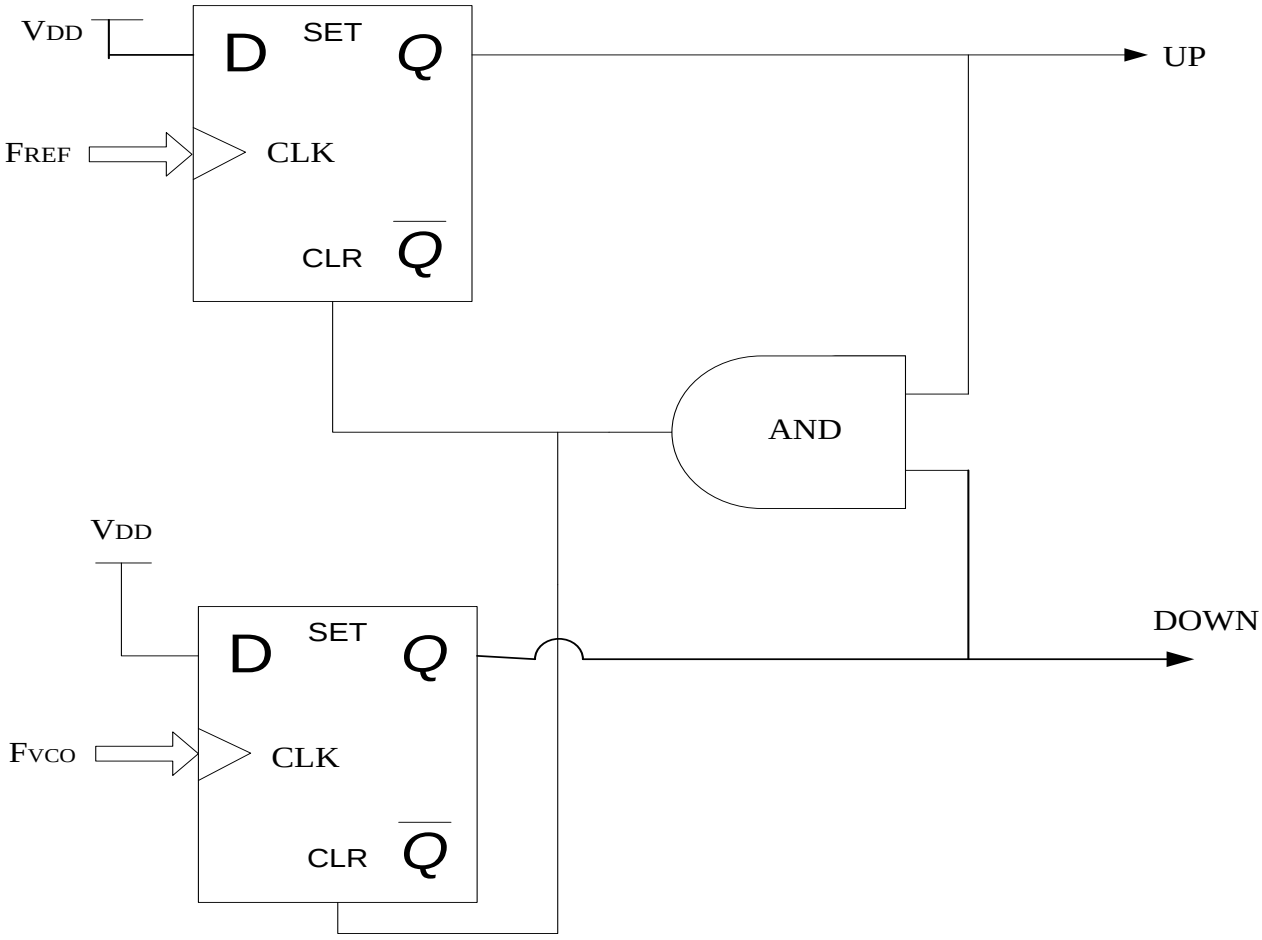

Figure 2.2.Phase Frequency Detector

2.1.3. Charge Pump

The charge pump supplies current to the loop filter to produce the VCO control voltage. The charge pump either sources or sinks a current to the loop filter based on the UP or DOWN signal. As a result, the loop filter output voltage is proportional to the phase error between the reference clock and output clock. Figure below shows the charge pump output stage of the phase/frequency detector of the charge pump phase lock loop.

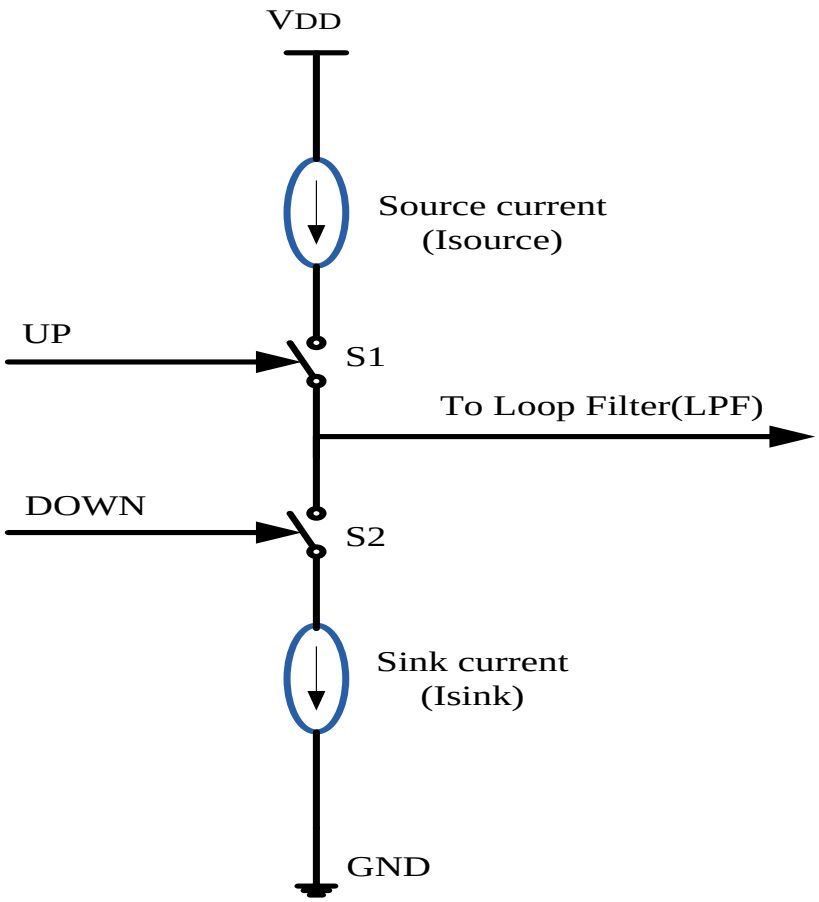

Figure 2.3.Charge Pump

The *UP* signal is high when the reference signal is operating at a higher frequency than the feedback signal. The charge pump forces current into the loop filter when the *UP* signal is high. This causes the VCO control voltage to rise, which increases the VCO frequency and brings the feedback signal to the same frequency as the reference signal.

The *DOWN* signal is high when the reference signal is operating at a lower frequency than the feedback signal. The charge pump forces current out of the loop filter when the *DOWN* signal is high. This causes the VCO control voltage to fall. This decreases the VCO frequency and brings the feedback signal to the same frequency as the reference signal.

2.1.4. Loop Filter

The loop filter produces a voltage which is equivalent to the charge added or removed by the charge pump. This voltage controls the frequency of the VCO output. The loop filter is a low pass filter with its poles determining the bandwidth of the PLL. The simplest loop filter is a capacitor which is charged or discharged by the charge pump. This has a pole at the origin and makes the PLL loop unstable.

In order to stabilize the loop, a resistor is introduced in series with the capacitor and this is the first order loop filter. However when S1 or S2 turns ON, the current injection through the resistor results in a jump in the output voltage. Even in the locked state, mismatch between I_{source} and I_{sink} can lead to voltage jumps. The resulting ripple disturbs the VCO output. To suppress the ripple a second capacitor is added in parallel to the resistor and capacitor to form the second order loop filter. This voltage controls the VCO output frequency. The VCO output is the output clock of the PLL and is fed back to the PFD. The switching interaction between the charge pump and the loop filter causes a great deal of ripple on the VCO control voltage with the series R and C1 loop filter. This ripple may be suppressed by adding a small capacitor, *C*2, in parallel with the loop filter as shown in figure 2.4. The loop filter converts the charge pump error current, I_{source} or I_{sink}, into the VCO control voltage, V_{con}.

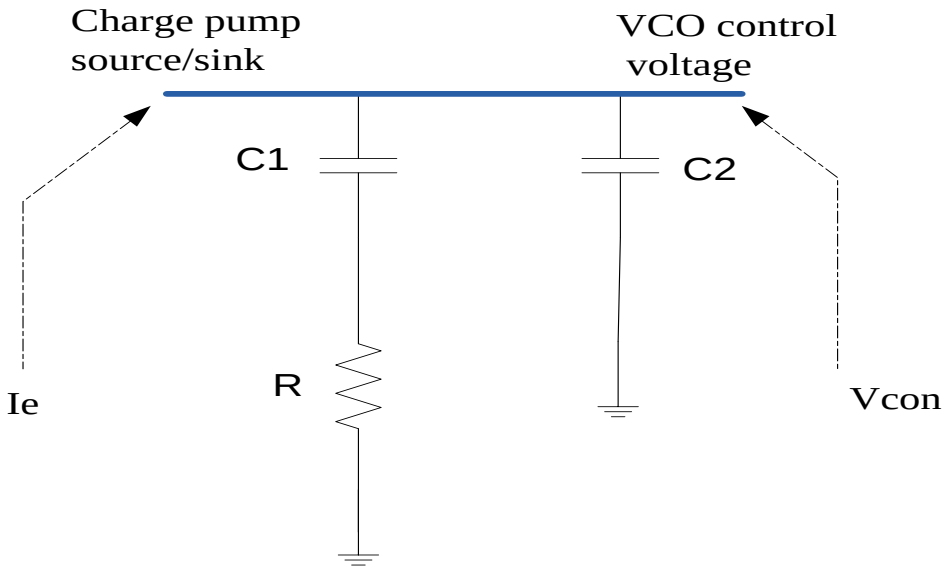

Figure 2.4. Loop filter circuit

Ignoring the smallest capacitor C2 explained earlier, the loop filter has the following transfer function, F(s), which is given as a function of charge pump error current (Ie) and VCO control voltage (Vcon),

$$F(s) = \frac{Output(s)}{Input(s)} = \frac{Vcon(s)}{Ie(s)} \tag{2.1}$$

$$= \frac{R\left(s + \frac{1}{RC1}\right)}{s} \tag{2.2}$$

The loop filter is the critical building block that determines the loop dynamics. In a charge pump phase lock loop, the natural frequency (ω_n) and the damping factor (ς) is set independently by the values of the components used in the loop filter. The capacitor, C1, sets the natural frequency, and resistor sets the damping factor.

2.1.5. Voltage Controlled Oscillator

The voltage-controlled oscillator generates an output signal with a frequency that is dependent on the input control voltage. A voltage controlled oscillator is a tunable oscillator whose frequency is a function of the input control voltage. For an ideal VCO, the output frequency is a linear function of the control voltage.

$$Fvco = Fo + KvcoKcon \quad (2.3)$$

Where F_{VCO} (the VCO output voltage), F_0 (center frequency), K_{VCO}, VCO output constant and K_{con} loop filter control constant of the entire voltage controlled oscillator.

The main performance parameters for the voltage controlled oscillator are the center frequency, F_0, tuning range and tuning linearity. Generally, K_{VCO} is not constant and this affects the settling of the phase locked loop. So it is desirable to have minimum variations in K_{VCO} across the tuning range. Two different families of voltage controlled oscillators are used, ring oscillator and LC tank oscillator. LC tank oscillator uses passive LC tank circuits while ring oscillator consists of a series of inverters connected as a loop. LC tank voltage controlled oscillators have better noise performance and a narrow tuning range, while the ring oscillator has small delay and settling or response time.

2.2. Transfer function model

The second order charge pump phase locked loop consists of the complete combined figure of Figures 2.2, 2.3, 2.4, with the voltage controlled block added at the output stage of the loop filter. Figure 2.5 gives the schematics for the complete charge pump phase locked loop schematic diagram.

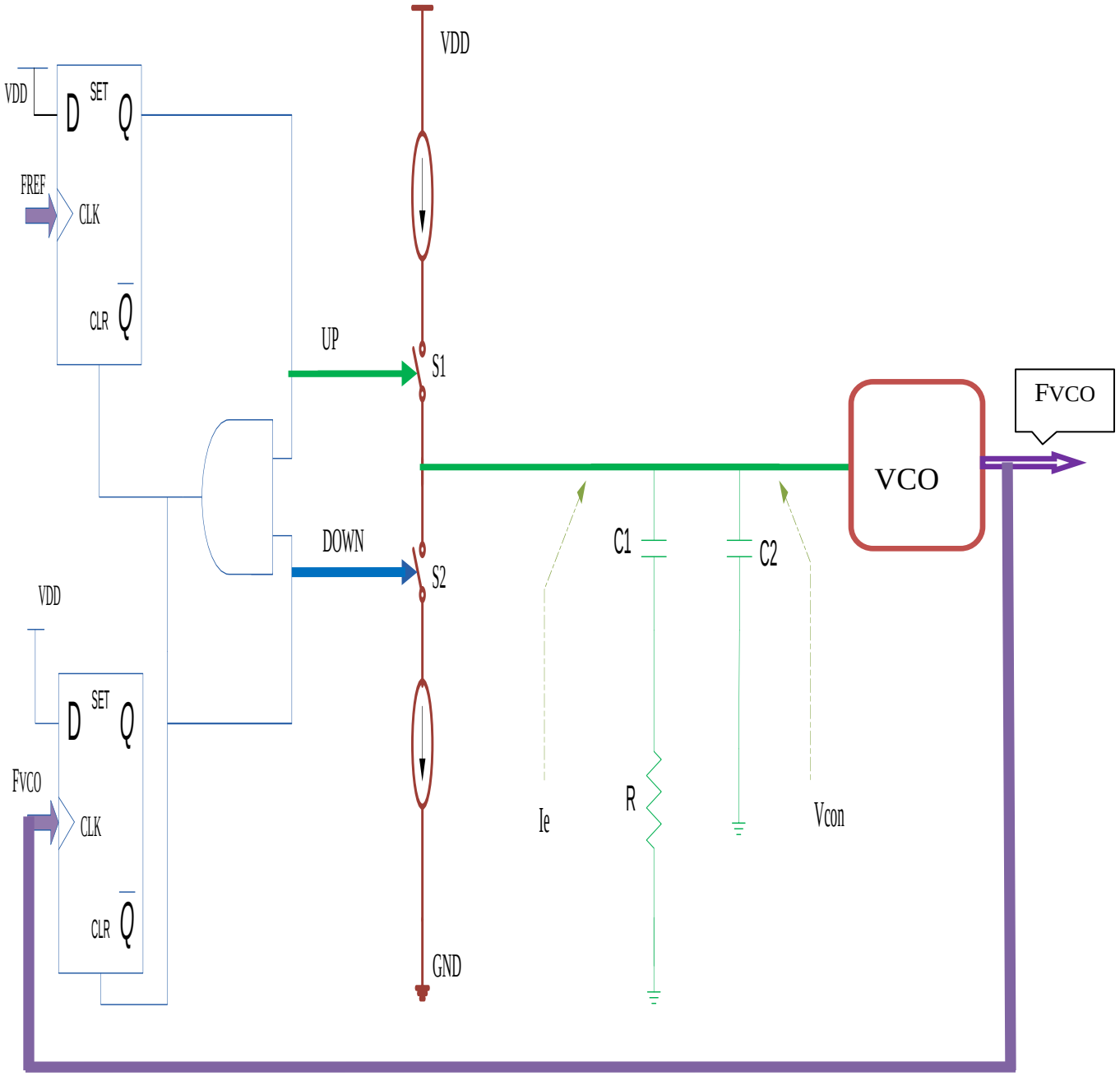

Figure 2.5.Second order charge pump phase locked loop schematics

The following figure illustrates the corresponding charge pump phase locked loop linear model

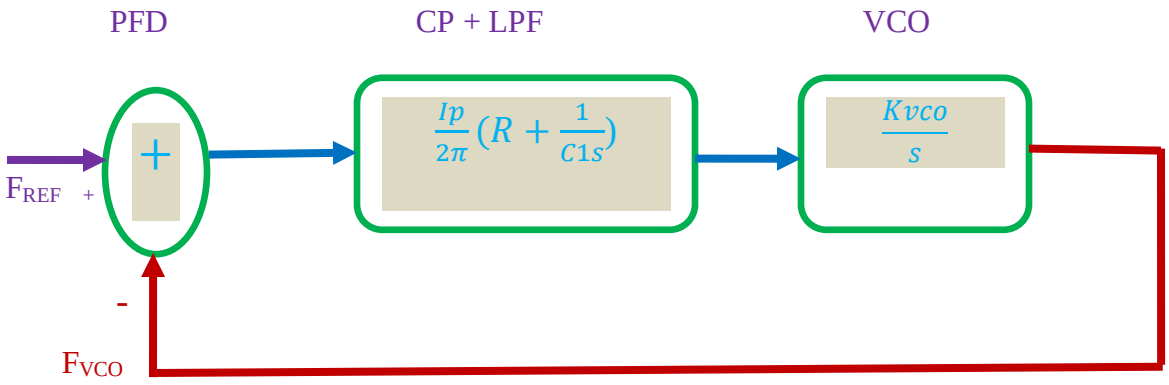

Figure 2.6.Charge pump phase locked loop linear model

Hence the transfer function model will be given by;

$$G(s) = \frac{H(s)}{1+H(s)} \tag{2.4}$$

$$= \frac{KpKvco(1+sC1R)}{s^2[(C1+C2)+sC1C2R]+KpKvco(1+sC1R)} \tag{2.5}$$

Where,

$$Kp = \frac{Ip}{2\pi} \tag{2.6}$$

Generally the capacitor C2 is small compared to C1 and can be neglected. Then the loop filter becomes first order and the resultant second order PLL loop equation is;

$$G(s) = \frac{KpKvco(1+sC1R)}{S^2C1+KpKvco(1+sC1R)} \tag{2.7}$$

$$= \frac{\frac{KpKvco}{C1}(1+sC1R)}{S^2+sKpKvcoR+(KpKvco/C1)} \tag{2.8}$$

Chapter 3

Discritizing Charge Pump Phase Locked Loop

3.1. Basic discritizing technique

The new ADPLL architecture, which is the digital counterpart of the conventional charge pump phase locked loop, derivation is the focus of this chapter. The only completely digital part in the conventional charge pump phase locked loop is phase frequency detector. To get digital phase locked loop architecture of charge pump phase lock loop counterpart, discritization technique used in control systems can be applied. The following continuous time control system block diagram is the way to discritizing charge pump phase locked loop.

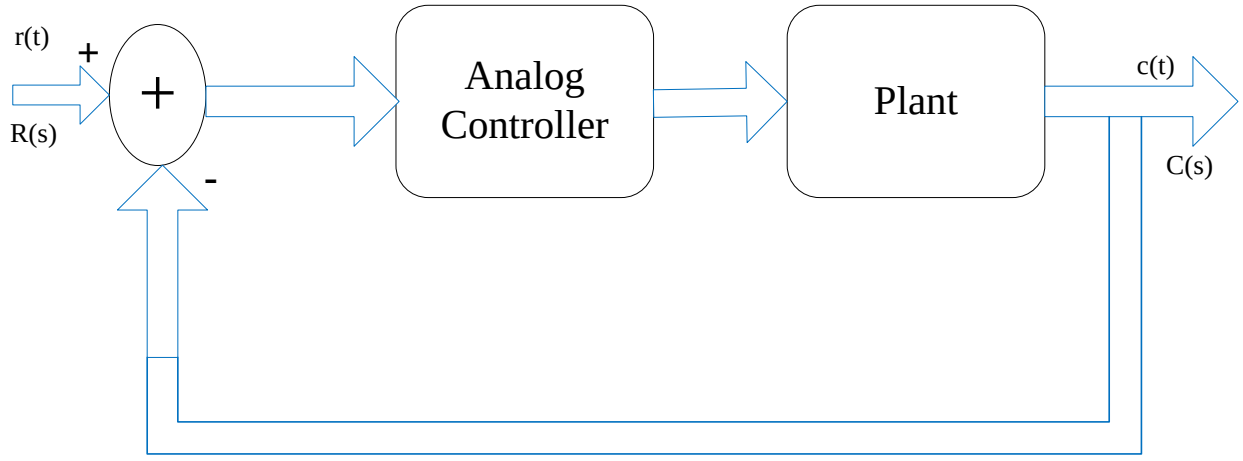

Figure 3.1.Continuous time control system

From the above figure the analog controller, which satisfies a given performance specification, has to be transformed to its digital equivalent. There has to be a sampler before the summing point and also hold circuit between the controller and the plant block. As given in the

conventional charge pump phase locked loop block diagram, the VCO is analogous to the plant, and the charge pump and loop filter acts as controller.

The equivalent digital system of figure 3.1 is given below, which has sample and hold in addition to the analog block digital counterpart and plant.

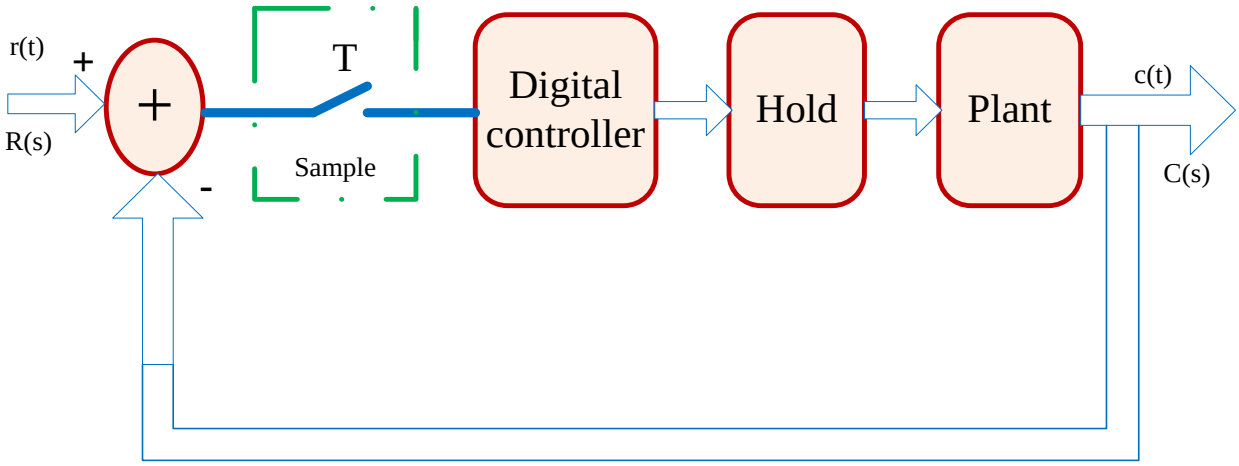

Figure 3.2.Digital controller system

3.2. Charge pump and loop filter digitization

The transfer function for first order loop filter and charge pump phase locked loop is given by,

$$\frac{Vcon(s)}{Ie(s)} = \frac{Ip}{2\pi}\left(R + \frac{1}{C1s}\right) \qquad (3.1)$$

As given in the previous charge pump block diagram and equations, I_P is directly dependent on the UP and DOWN signals, and takes positive or negative values. For matched current sources, the positive and negative values of I_P are same in magnitude. Hence the above transfer function can be equivalently expressed as follows,

$$\frac{Vcon(s)}{Ie(s)} = \frac{Ip}{2\pi}\left(R + \frac{1}{C1s}\right) \quad (3.2)$$

$$= \pm\frac{Ip}{2\pi}\left(R + \frac{1}{sC1}\right) \quad (3.3)$$

$$= \underbrace{\left(\pm\frac{Ip}{2\pi}R\right)}_{\text{Gain stage}} + \underbrace{\left(\pm\frac{Ip}{2\pi}\left(\frac{1}{sC1}\right)\right)}_{\text{Integrator}} \quad (3.4)$$

As shown in the above equation, the first term represents the gain stage which can be implemented as a digital multiplier, with a multiplier coefficient of,

$$C = \frac{IpR}{2\pi} = KpR \quad (3.5)$$

The second term represents an integrator which can be implemented as a digital accumulator. The input to both of these units takes either +1 or -1 depending on the UP and DOWN signals respectively.

3.3. Sample and Hold

In simultaneous with digitizing the controller, the sample and hold functions need to be introduced before and after the controller. The sample circuit will intake the UP and DOWN signals from phase frequency detector and gives out sampled version of UP and DOWN signals. The sampling can be done with respect to the reference clock frequency for simplicity.

This will result in phase frequency detector with UP and DOWN signal pulses being changing with reference clock edges. The hold circuit will require the controller output being held for a clock cycle. This can be achieved by registering the controller output with the reference clock. After completing digitization of the controller, the output end needs to be digital, which is analog. This cannot be applied directly to voltage controlled oscillator. Rather the voltage controlled has to be replaced with its digital counterpart, Digitally Controlled Oscillator. The new All Digital Phase Lock Loop architecture after digitization is given in figure 3.3,

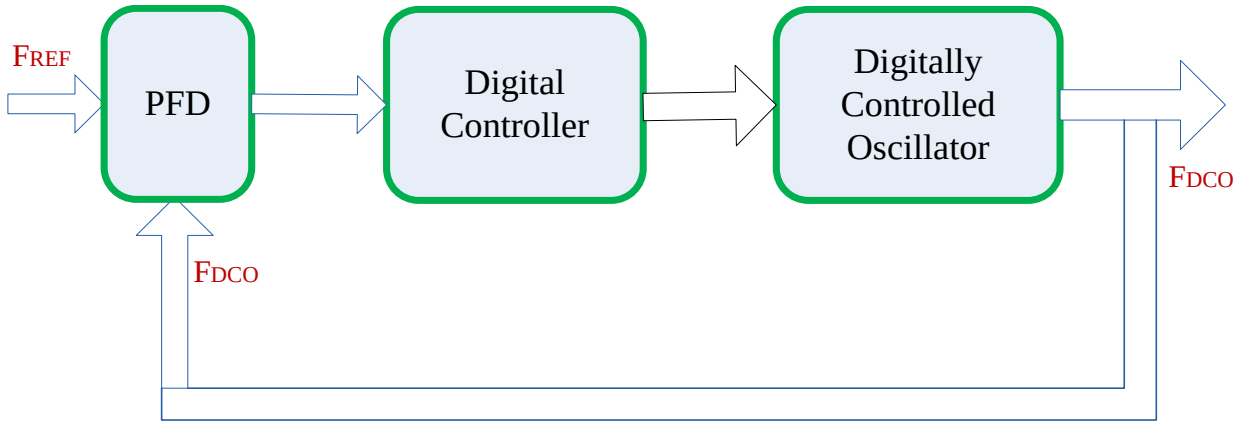

Figure 3.3.Improved ADPLL architecture

3.4. Transfer function model

After having the new architecture for conventional all digital phase locked loop, it needs to have transfer function model so that we can analyze the stability of the system. This analysis provides insight into poles and zeros of the system, and also gives the design equation for the phase locked loop. The equivalent function model is given below,

,

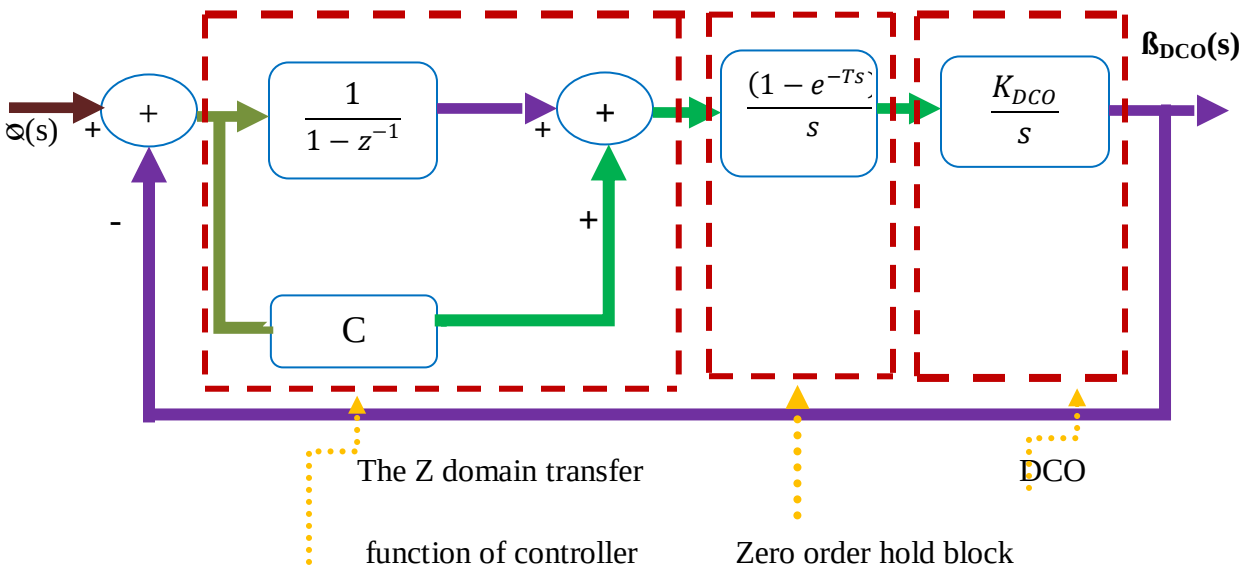

Figure 3.4.Equivalent transfer function model

The accumulator is replaced with its z domain transfer function. The z domain transfer function for the controller will be given by,

$$H_1(z) = C + \frac{1}{1 - z^{-1}} \tag{3.6}$$

The DCO can be replaced with ideal integrator in s domain. A zero order hold is introduced between the DCO and the controller for transforming from discrete domain to continuous domain. The z domain transfer function for the zero order hold followed by DCO can be obtained by the convolution integral method discussed in [3]. Hence the combining transfer function is given by,

$$H_2\,(s) = \frac{(1 - e^{-Ts})H'(s)}{s} \tag{3.7}$$

$$= (1 - e^{-Ts})H_3(s) \tag{3.8}$$

Where H(s) is the DCO transfer function model,

$$H'(s) = \frac{K_{DCO}}{s} \tag{3.9}$$

$$H_3(s) = \frac{H'(s)}{s} \tag{3.10}$$

$$= \frac{K_{DCO}}{s^2} \tag{3.11}$$

Let Y(s) represent the following expression,

$$Y(s) = e^{-Ts}H_3(s) \tag{3.12}$$

Since Y(s) is the product of two Laplace transformed functions, the inverse Laplace transform is given by,

$$y(t) = \int_0^t (h_4(t-T)h_3(t))dt \tag{3.13}$$

$$h_4(t) = L^{-1}[e^{-Ts}] = \delta(t-\tau) \tag{3.15}$$

$$h_3(t) = L^{-1}[H_3(s)] \tag{3.16}$$

Hence,

$$y(t) = \int_0^t (\delta(t-\tau-T) * h_3(t))dt \tag{3.17}$$

$$= h_3(t-T) \tag{3.18}$$

Then by finding the z transform of $h_3(t)$, we can get its corresponding H(z) and finding z transform of y(t), we can have the following equation,

$$Z[y(t)] = Z[h_3(t-T)] \tag{3.19}$$

$$Y(z) = z^{-1}H_3(z) \tag{3.20}$$

Then sorting out equation (3.8) we can get,

$$H_2(z) = Z[H_3(s) - e^{-Ts}H_3(s)] \tag{3.21}$$

$$= Z[h_3(t) - y(t)]$$

$$= H_3(z) - z^{-1}H_3(z)$$

$$= H_3(z)(1 - z^{-1}) \tag{3.22}$$

But H_3 (z) is given by,

$$H_3(s) = Z\left[\frac{K_{DCO}}{s^2}\right] \tag{3.23}$$

$$= Z[\left[\frac{1}{s}\right] * \left[\frac{K_{DCO}}{s}\right]] \quad (3.24)$$

$$= K_{DCO} \frac{Tz^{-1}}{(1-z^{-1})^2} \quad (3.25)$$

Then using the above equation, we can have the following, and the previous expression for H_2 (z), can be given as follows,

$$H_2(z) = (1-z^{-1})H_3(z) \quad (3.26)$$

$$= \frac{K_{DCO}Tz^{-1}}{1-z^{-1}} \quad (3.27)$$

After all we need to get the feed forward transfer function for H (z), which is given as follows,

$$H(z) = H_1(z) * H_2(z) \quad (3.28)$$

$$= \frac{K_{DCO}Tz^{-1}}{1-z^{-1}} \ (C + \frac{1}{1-z^{-1}}) \quad (3.27)$$

$$= \left(Cz - C + \frac{z}{z-1}\right)\frac{K_{DCO}Tz^{-1}}{1-z^{-1}} \quad (3.28)$$

The total transfer function is given by,

$$G(z) = \frac{H(z)}{1+H(z)} \quad (3.29)$$

$$= \frac{(z(C+1)-C)TK_{DCO}}{(z^2+z[(C+1)\mathrm{TKDCO}-2]+(1-\mathrm{TKDCO})} \quad (3.31)$$

The above transfer function given in equation 3.31 has three parameters, namely, T, C and K_{DCO}, where T is the reference clock period and is constant for a given reference clock specification. K_{DCO} is DCO constant which is fixed by the DCO characteristics. C is the feed forward gain and

is the only parameter which can be varied to tune the system response. The two poles of the total transfer function is given by,

$$Z = \frac{(1-(C+1)TK_{DCO}}{2} \pm \sqrt{(\frac{(C+1)TK_{DCO}-2)^2-4(1-CTK_{DCO})}{4}} \quad (3.32)$$

For damping ratio, ς and natural frequency, ω_n, the poles in s domain is given by,

$$s = -\varsigma\,\omega_n + j\,\omega_n\sqrt{(1-\varsigma^2)} \quad (3.33)$$

But $z = e^{Ts}$, and the respective point in the z plain is given by basing the above equation,

$$z = e^{[T(-\varsigma\,\omega_n + j\,\omega_n\sqrt{(1-\varsigma^2)})]} \quad (3.34)$$

But for a critically damped system, $\varsigma = 1$, then the above equation simplifies to,

$$z = e^{-T\omega_n} \quad (3.35)$$

And the imaginary part of the pole becomes zero. From phase locked loop point of view, the imaginary part for the phase locked loop to be critically stable is given by,

$$((C+1)TK_{DCO} - 2)^2 = 4(1 - CTK_{DCO}) \quad (3.36)$$

Then solving for C,

$$C = \frac{2}{\sqrt{TK_{DCO}}} - 1 \quad (3.37)$$

By approximating the total transfer function of the ADPLL for critically damped case, we get the following simplified equation,

$$G(z) = \frac{CTK_{DCO}(z-1)}{z^2 - 2z + 1}$$

$$G(z) = \frac{CTK_{DCO}}{z-1}$$

$$G(z) = \frac{CTK_{DCO}\,z^{-1}}{1 - z^{-1}} \quad (3.38)$$

As you can see equation 3.38, it is a low pass transfer function. The response of the system is low pass which means that the phase locked loop track has slow variations in phase variation accurately, while fast variations are filtered out. Using equation 3.38 we can get the following plots using matlab, for a constant given values. Replacing the constant values of C=188, T=1.1 ns, and K_{DCO} =100 KHz for band one; we get the following graph shown in figure 3.5. In the same manner, replacing C=267, T= 0.56 and K_{DCO} =100 KHz for band two, we get the plot shown in figure3.6.

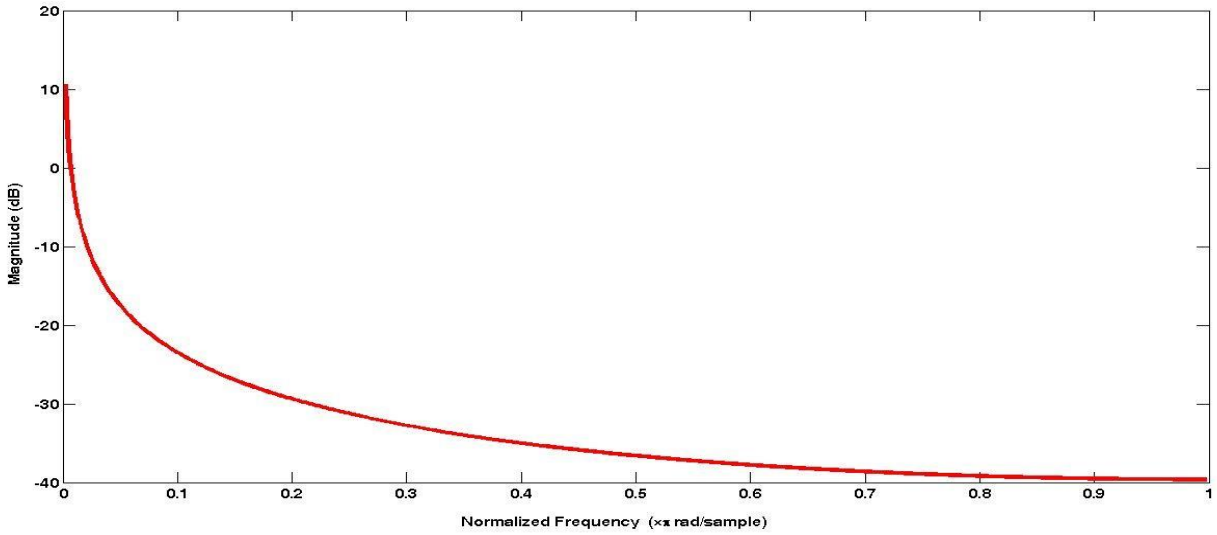

Figure.3.5. Low pass response system for band one

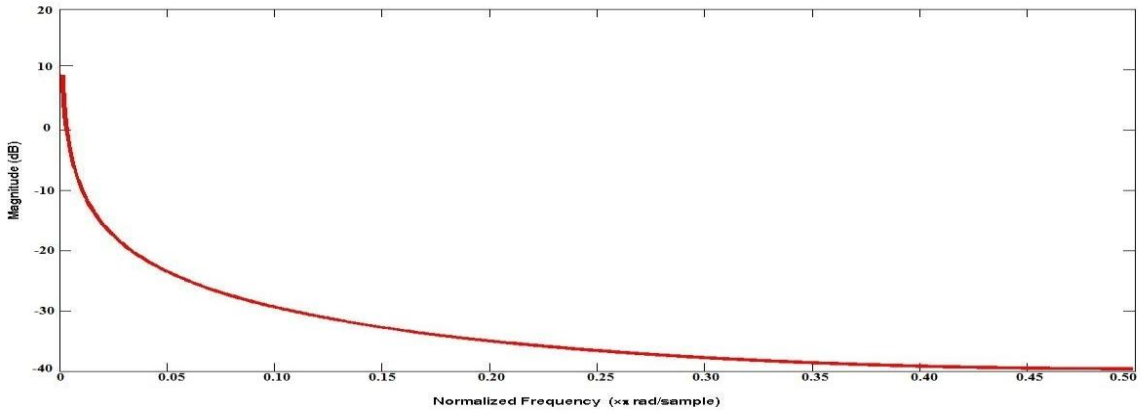

Figure 3.6.Low pass response system for band two

Chapter 4

Block Level Design of Dual Band All Digital Phase Locked Loop

4.1. Specification of ADPLL

Design of ADPLL begins with specifying the specification required for the targeted dual-band Global System for Mobile Communication application. The ADPLL design discussed here is targeted for GSM band-1 and GSM band-2 application with center frequency of 900MHz and 1800MHz respectively. The entire specification for GSM band-1 and GSM band-2 is given below,

No.	Parameter	GSM bands	
		Band-1	Band-2
1.	PLL center frequency	900MHz	1800MHz
2.	Tuning range	800MHz – 1000MHz	1700MHz – 1900MHz
3.	DCO sweep frequency	200 MHz	200 MHz
4.	Clock crystal oscillator	800 MHz – 1 GHz	1.7 GHz – 1.9 GHz
5.	Average settling time	4 usec	4 usec
6.	DCO frequency resolution	100KHz	100KHz
7.	Power supply	1.2V	1.2V
8.	Technology	UMC 0.13μm	UMC 0.13μm

Table 4.1.Specification of ADPLL for GSM-900 and GSM-1800

4.2. Design Methodologies

Based on the specifications given before, the specific value of C is fixed as per equation 3.38 for both bands. Doing so will make the system to be critically damped and hence will result in the best settling time. Using equation 3.38 the specific value of C comes out to be 188 and 267 for band-1 and band-2 respectively. As previously stated in chapter two, C is dependent on the parameters K_{DCO} which is process, voltage and temperature dependent.

The control word width of the DCO is used to fix the digital word length for the multiplier, adder and accumulator. The DCO control word should be able to sweep the DCO frequency across the 200MHz with step size of 100 KHz for both band-1 and band-2. Hence the maximum control word size should be 200MHz divided by 100 KHz, which is equivalent to 2000. This leads for control word width of 11 bits. With this amount of bits, the control word can go up to 2048, and for tuning range of 200MHz, the actual frequency resolution is approximated to be 97.66 KHz for both band-1 and band-2.

4.3. Features of Unified Microelectronics Corporation technology

RFCMOS applications have major requirement for SoC design. UMC provides a logic compatible process for RF solutions and offers many advanced features to optimize the passive devices such as inductors and capacitors. The frequency range of UMC's scalable models range up to 20 GHz. Key features of UMC technology are high Q inductors on the thicker top copper metal, high density MIM capacitors, cost effective Metal Oxide Metal capacitors, precision poly resistors, deep N-well for noise isolation, multiple Vt devices for optimized circuit performance, wide tuning range varactors and diodes.

UMC's innovative Fusion process allows different transistor devices, such as high speed and low leakage to be combined on the same design. This creates a single chip solution that offers the advantage of high performance without sacrificing energy efficiency, ideal for today's 3G,

wireless, and portable communication products. RFCMOS products success at UMC for GSM ranges from 0.18um to 0.09um. From process baseline comparison we can get the following,

RFCMOS technology	Process baseline			
	Low power	Standard performance	High speed	General Enhancement
0.09um	yes	yes	-	-
0.13um	yes	-	yes	-
0.18um	-	-	-	Yes

Table 4.2 Comparison of GSM applicable UMC technologies

UMC 0.13um supports its standard cell library with low power design features, including multiple Vt, clock gating, level shifter and other features to complement the complete low power SoC solution. Its SoC solution begins with a flexible technology design platform. Customers are able to choose from a variety of process device options optimized for their specific application, such as High Speed, Standard Performance, Low Leakage, or the unique Fusion process. It has Virtual Inductor Library and Virtual Capacitor Library, which will enable RFCMOS designers to create and simulate custom inductor and capacitor geometries that are compatible with UMC's process. UMC's mainstream 0.13um technology is in volume production for a wide range of consumer electronics and security communication sector.

4.4. Circuit Level Design of various Components of ADPLL

4.4.1. Introduction

After all the circuit level design of various components of ADPLL is the main task. As shown in chapter three the whole structure involves the design of the DCO, the PFD and the Controller. Since DCO is a vital block of the ADPLL, it is one of the viable approaches to the implementation of other radio frequency portions which are compatible with digital portions. The performance of the DCO, such as the frequency resolution and phase noise, has a significant impact on those of the ADPLL. The phase noise of DCO is a function of the frequency resolution that is limited by the value of unit switchable capacitor. Since DCO determines the exact specifications required for the controller, the design of DCO is discussed first.

4.4.2. Design of Digitally Controlled Oscillator

I). Deciding DCO architecture type

Before designing DCO, fixing the architecture of DCO is a fore coming task. The architecture can be ring oscillator based or LC oscillator based. Ring oscillator based architecture uses a series of inverter stages connected as a ring, with the delay of the inverters controlled by the control word. LC oscillator architecture consists of an LC tank which oscillates at a fixed resonant frequency. The frequency can be made variable by adding or removing capacitances from the tank, based on the control word.

LC oscillators contain passive inductors and capacitors which are highly susceptible to process and temperature variations. The tuning ranges of LC oscillators are limited. The inductors will occupy large area and the power dissipation is very high. Compared to LC oscillators, ring oscillators occupy less area and consume less power. But the noise performance of ring oscillators is poor compared to LC oscillators. Based on the *superior noise performance*, LC oscillator based DCO architecture is selected. The tuning range for the targeted application is limited and can be achieved with a LC digitally controlled oscillator.

II). DCO Oscillator Core

The aggressive cost and power reduction of high-volume mobile wireless solutions can only be realistically achieved by highest level of integration with the digital back-end onto a single silicon die, and this favors digitally intensive approach in the most aggressive deep-sub micrometer process.

The DCO used in the design is based on the design proposed in [6]. The DCO is derived from the widely used LC VCO circuits. In LC VCO, the capacitance in the LC tank circuit is tunable with control voltage, and varies continuously with the input control voltage. Unfortunately, the design flow and circuits techniques needed are quite analog intensive and utilize process technologies that are incompatible with the digital baseband, in which it is built in a low-voltage deep sub micrometer digital CMOS process with almost no extensions and very limited voltage headroom.

In order to address the various deep-sub micrometer RF integration issues for frequency synthesis, digitally intensive techniques need to be developed such that analog imperfections are compensated for by using advanced signal processing techniques. The equivalent of LC digitally controlled oscillator of LC voltage controlled oscillator has an array of binary weighted varactors, instead of the single varactor in LC voltage controlled oscillator. Its equivalent for the LC digitally controlled oscillator is given figure 4.1.

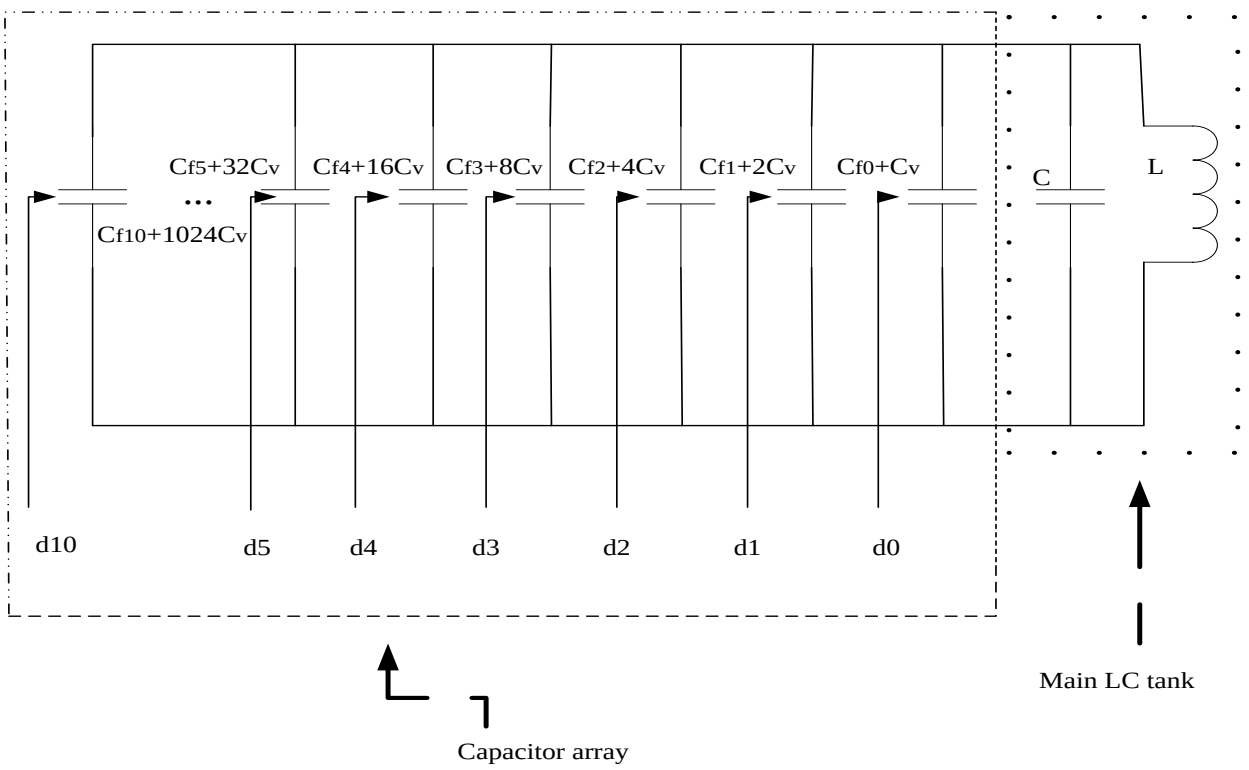

Figure 4.1 Distributed binary weighted LC DCO equivalent circuit

The circuit given in figure 4.1 contains an inductor and constant capacitor in parallel with an array of varactors of the binary weighted tank. The control voltage to these varactors are digital and the varactors can be switched between a high capacitance mode and a low capacitance mode as stated in [5]. An array of varactors could be switched into a high-capacitance mode or low capacitance mode individually by a two level digital control voltage bus, thus giving a very coarse step control for LSB.

In order to achieve a very fine frequency resolution, the LSB bit could possibly be operated in analog fashion. Each varactor could be allowed to stay in only one of the two regions where the capacitance sensitivity is the lowest and the capacitance difference between them is the highest. The control word lines connected to the larger varactor act as the MSB and have coarse step control, while the lines connected to the smaller varactors act as LSB and have a finer step control. The varactor will have fixed capacitance component and a variable capacitance component. The detailed schematics for the DCO core is given figure 4.2 which is the same as

the circuit used in [5], except for the inverting drivers for the varactors. These drivers are not needed since the output driver strength of the controller is sufficient enough to drive the varactor.

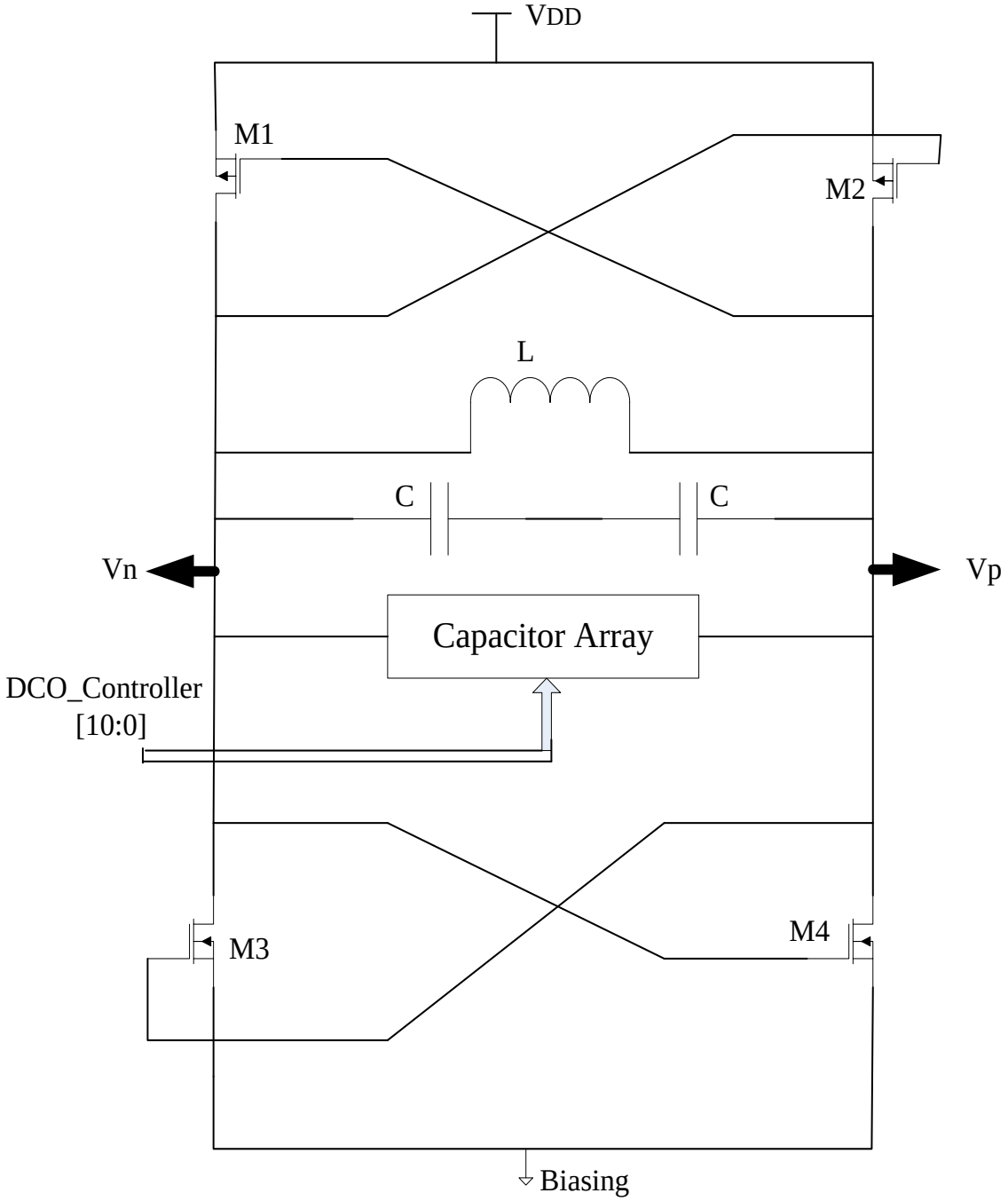

Figure 4.2 Digital Controlled Oscillator core circuit

III). DCO Varactror Array

Frequency tuning of a low-voltage deep-sub micrometer CMOS oscillator is quite a challenging task due to its highly nonlinear frequency versus voltage characteristics and low voltage headroom. The varactor array added to the basic LC tank circuit consists of scaled capacitances, which can be switched added and removed using the digital control bus connected to the circuit. But if the control word is in binary format, the MSB lines should add larger capacitors compared to the LSB. These forces the capacitors to be made binary weighted, with the capacitance in the ratio of powers of two. But at 130nm technology, the lengths, widths and oxide thickness varies from one MOSFET to another MOSFET, and this results in variations in the capacitance values in the circuit. Hence it is impossible to get exact ratios between the capacitors. In the binary weighted scheme, changes in capacitance ratios can lead to immense nonlinearity in DCO characteristics, which is undesirable as shown in [6] and [8].

In the work of [8], it uses a unit weighted scheme instead of binary weighted capacitors scheme. In unit weighted scheme all the capacitors are of same dimensions and hence better matching is possible. In addition, the switching order is also predetermined, and this results in excellent monotonocity and linearity. Moreover a unit weighted scheme has the advantage of small changes in the control word which results in smaller switching transient, since the number of capacitors to be switched is not greater that the code change. In addition, all the bit lines are connected to the same load which guarantees similar switching delays on all the lines in the circuit. The total delay depends only on the changes in routing length, which can be reduced by careful layout.

As illustrated in chapter three, the design needs a binary control word of 11 bits, which transforms to a unit weighted word of 2^{11} -1=2047 lines. This requires a thermometer encoder of 11 to 2047. But the resultant thermometer encoder will occupy large area and will dissipate large dynamic and leakage power. Also for a maximum reference frequency of 1 GHz and 1.9 GHz for band-1 and band-2 respectively, the decoder has to be timing closed to less than 1nsec and 0.526 nsec respectively without any pipelining. Table 4.3 shows comparison of total cell area and worst case dynamic and leakage power with respect to the bandwidth for thermometer encoder.

Encoder Configuration	Delay(ns)	Area(μm^2)	Dynamic Power(mW)	Leakage Power(μW)
11 bit	0.7	122146	81.62	41.78
7bit(LSB) + 4bit(MSB)	0.7	5663	4.63	2.29
5 bit(LSB) + 6bit(MSB)	0.59	3258	2.71	1.303

Table.4.3. Comparison of differential thermometer encoder configuration

The segmented scheme has a better matching than non segmented scheme, which helps to reduce the complexity of the thermometer encoder as shown in [6]. The 5 bits of the LSB of the binary control word is thermometer encoded and connected to 2^5-1=31 unit weighted capacitors. Each of these capacitors has the same capacitance of C_{LSB} as required for the minimum frequency change. The 6 bits of the MSB of the binary word are thermometer encoded and connected to 2^6- 1= 63 identically connected capacitors of C_{MSB}. But the C_{MSB} are 32 times that of C_{LSB}. These results in a smaller area, lower power and shorter circuit critical path compared to the non-segmented 11 bit encoder configuration. To improve poorer matching and switching delay of the segmented scheme, instead of using a capacitor with a large dimension for C_{MSB}, 32 capacitors of capacitance C_{LSB} are connected in parallel. Figure 4.3 shows the complete segmented scheme.

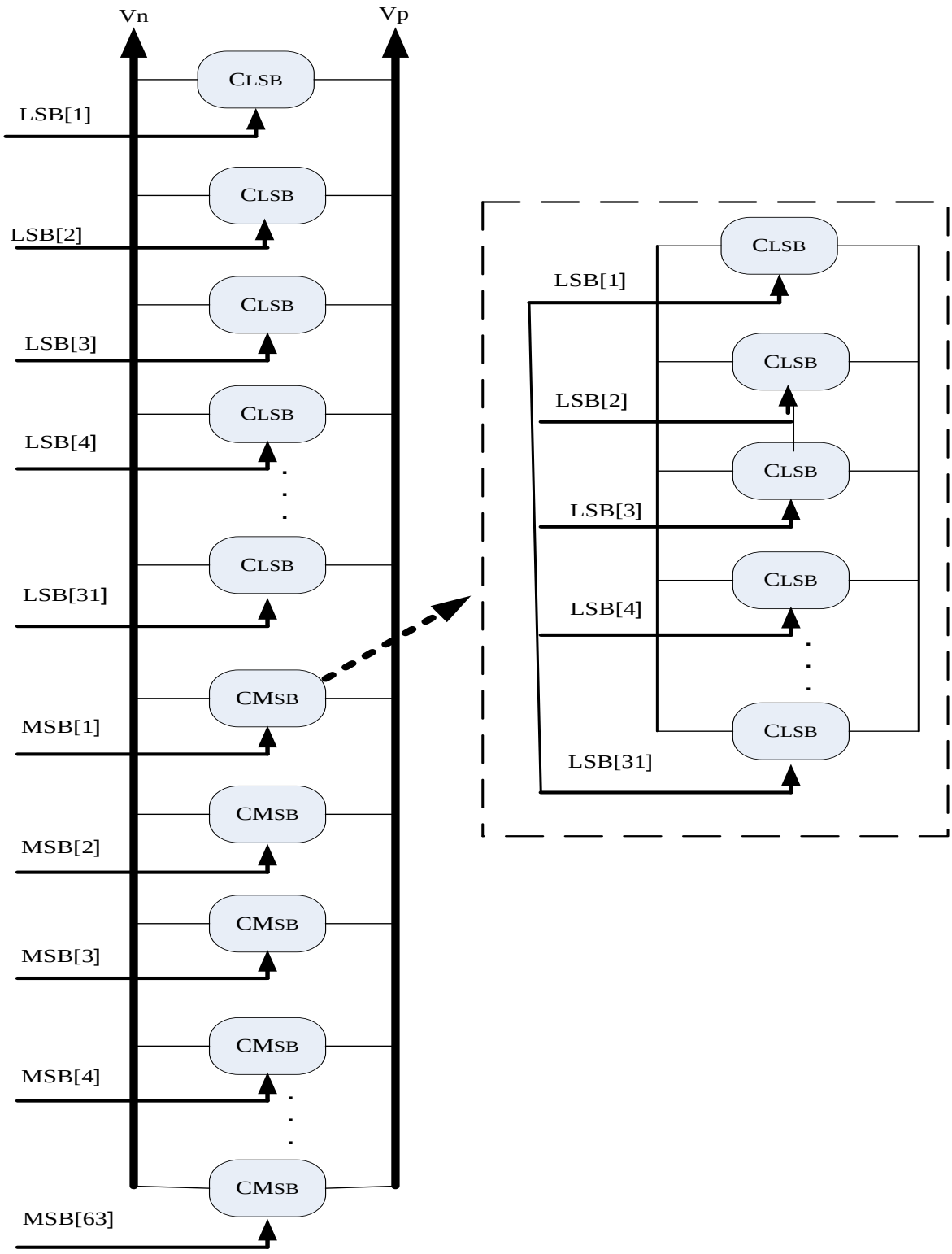

Figure 4.3 the complete segmented scheme of unit weighted varactor array

The frequency of oscillation for LC oscillator is given by,

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

Let F_{OSC1} be the oscillation frequency with a capacitor of C1. And let ΔC be the capacitance added to decrease the frequency by, ΔF, i.e.

$$F_{OSC1} = \frac{1}{2\pi\sqrt{LC1}} \tag{4.2}$$

$$F_{OSC1} - \Delta F = \frac{1}{2\pi\sqrt{L(C-\Delta C)}} \tag{4.3}$$

Using binomial approximations, equation 4.3 can be simplified to,

$$F_{OSC1} - \Delta F = \frac{1}{2\pi\sqrt{LC1}}\left(1 - \frac{\Delta C}{2C}\right) \tag{4.4}$$

$$F_{OSC1} - \Delta F = F_{OSC1}(1 - \frac{\Delta C}{2C}) \tag{4.5}$$

$$\Delta F = F_{OSC1}\frac{\Delta C}{2C} \tag{4.6}$$

Hence the change in frequency with the addition of fixed capacitance value is higher at higher frequency. As per specifications given, the tuning ranges are 800 MHz to 1000MHz for band-1 and 1.7 to 1.9GHz for band-2. The stacked inductor from the UMC 130nm RFCMOS library can be used. The minimum inductance value available as a PCELL in the library is 29.208 nH, and this cell will be used in the design.

Using equation 4.1, the corresponding capacitor values are 1355fF and 867.24fF for band-1. Taking 11 bit control word, the required capacitance resolution is,

$$Capacitance\ resolution = \frac{1355fF - 867.24fF}{2^{11}} \cong 238aF \qquad (4.6)$$

So when all the 2047 control word lines are zero, the total capacitance will be 1355fF and when all lines are one, it will be 867.24fF.

In the same way using equation 4.1, the corresponding capacitor values are 300.082fF and 240.232fF for band-2. Taking all 11 bit control word, the required capacitance resolution is,

$$Capacitance\ resolution = \frac{300.082fF - 240.232fF}{2^{11}} \cong 29.22aF \qquad (4.7)$$

So when all the 2047 control word lines are zero, the total capacitance will be 300.082 fF and when all lines are one, it will be 240.232 fF.

IV). MOSFET Varactror in UMC 0.13um Technology

As shown in [5], due to the well isolation properties in the N-well process, the PMOS device is a better candidate for a MOS varactor. It was experimentally assured that in the process the ppoly/nwell inversion type varactor features more distinctly defined operational regions that do the accumulation type varactor. Advanced CMOS process lithography today allows the creations of extremely small-size, but well-controlled varactors.

The UMC 0.13um technology provides varactor diodes and Metal Insulator Metal capacitors as parameterized cells, which include schematic driven layout to provide an automated and complete design flow. But the minimum capacitance value available with these PCELLs is 8.85fF. To achieve a frequency resolution close to 100 KHz, the minimum change in capacitance can be calculated as around 200aF. Such low capacitances can be obtained by using the gate capacitances of MOSFETs directly.

In [5], the basic MOSFET structure consists of a MOSFET with gate as one terminal, and drain, source and substrate shorted together to form the second terminal. The MOSFETs can be either PMOS or NMOS. But NMOS requires a twin-well structure since the substrate has to be isolated, and hence PMOS is preferable. The capacitance offered by this structure will be the gate oxide capacitance and scales with width and length of MOSFETs. Two PMOS capacitances are connected in series with the substrate terminal shorted together to get the differential configuration. The common terminal acts as the control terminal. A high voltage at the control terminal gives a low capacitance between the two gate terminals and a low voltage gives a high capacitance. Figure 4.4 shows differential varactor, schematics using PMOS.

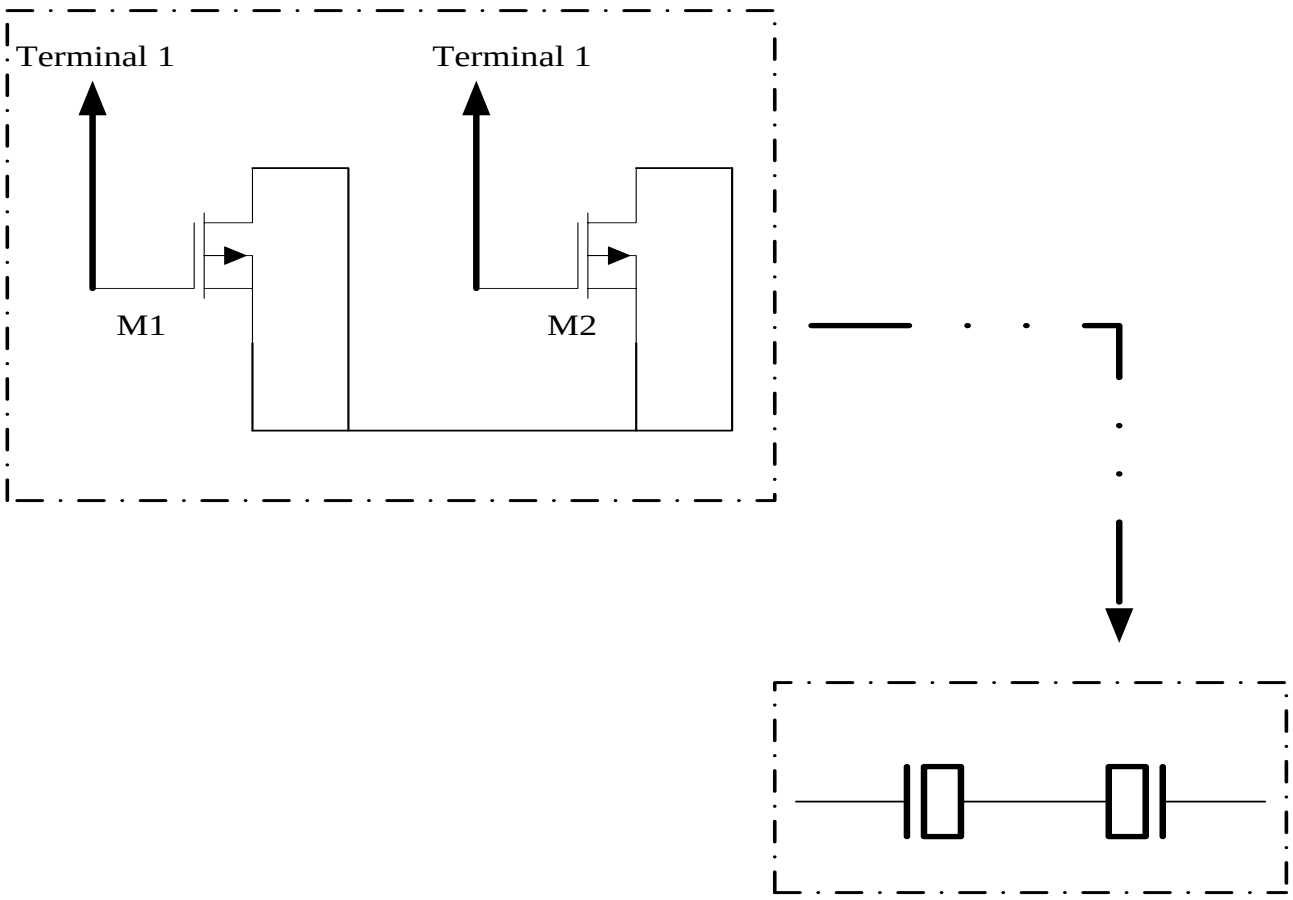

Figure 4.4 Differential varactor using PMOS pairs

4.4.2. DCO Design Implementation

As shown partly in [8] and [11] the oscillator core output will be sinusoidal in nature and will not give full rail to rail swing. Also there will be variations in the amplitude, with frequency of oscillations and process change. To obtain full swing output clock, the V_P and Vn outputs has to be followed by output drivers. A chain of inverters is used as the output driver. The clock output from the drivers will have rail to rail swing and have improved rise time. Figure 4.5 shows the digitally controlled oscillator circuit.

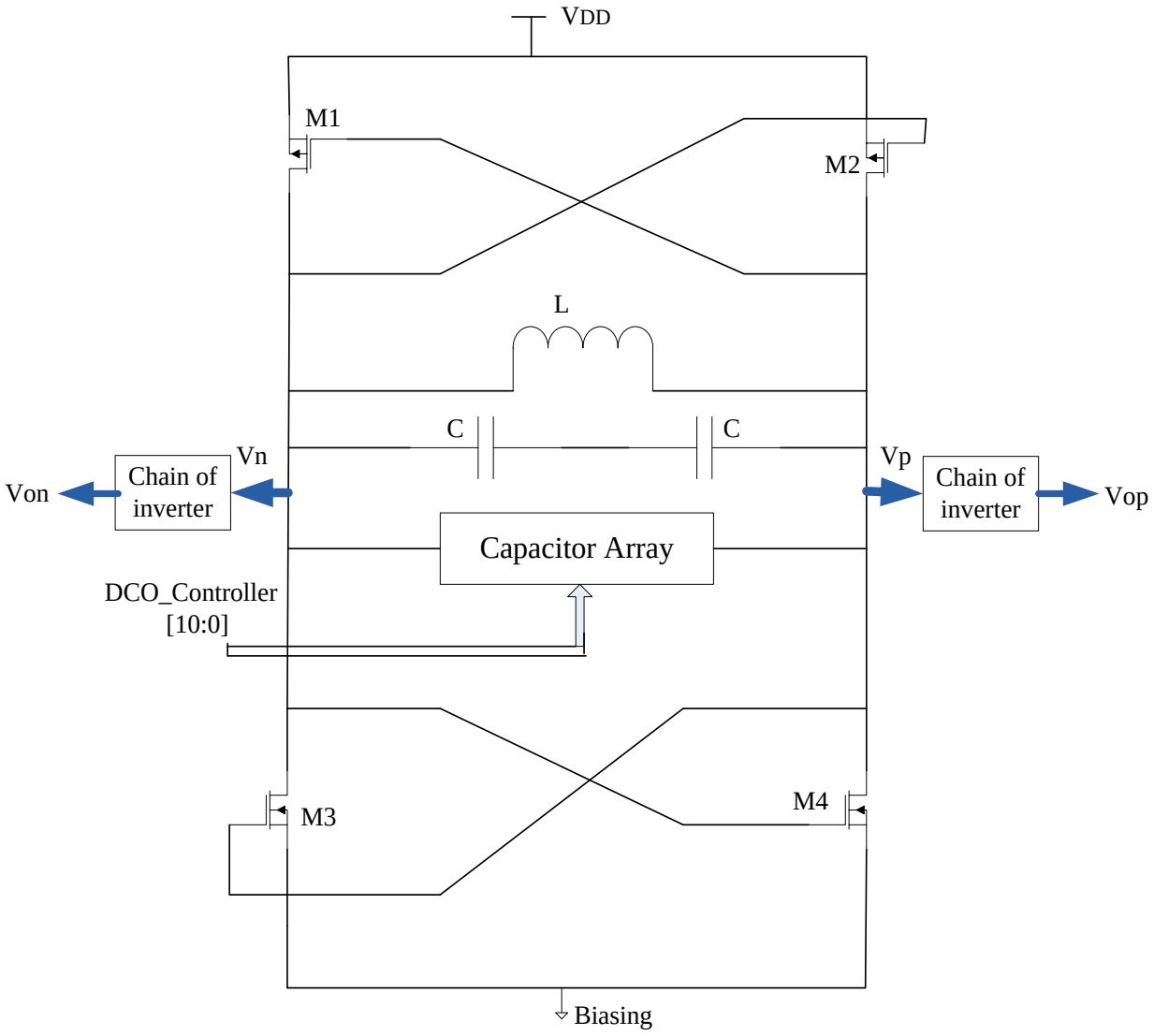

Figure 4.5.Distributed Digital Controlled Oscillator implementation circuit

As described in section 4.2, control word is given by,

$$Control\,Word(CW) = \frac{Change\,infrequency}{Resolution} = (F_{max} - F_{min})\frac{1}{R} \qquad (4.8)$$

$$\rightarrow F_{max} = F_{min} + CWR \qquad (4.9)$$

Using the above equation we can get the plots shown in figure 6.6 and 4.7 for band one and band two respectively.

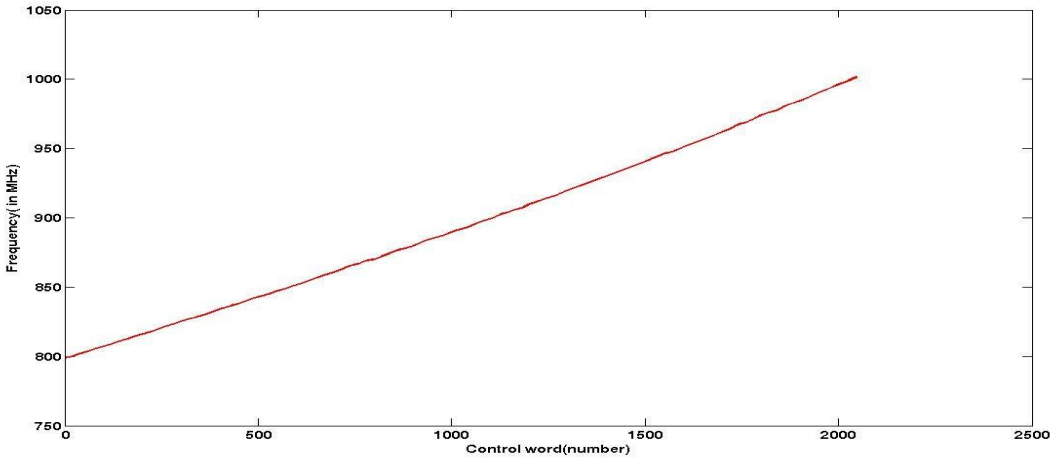

Figure 4.6.DCO characteristics for band one

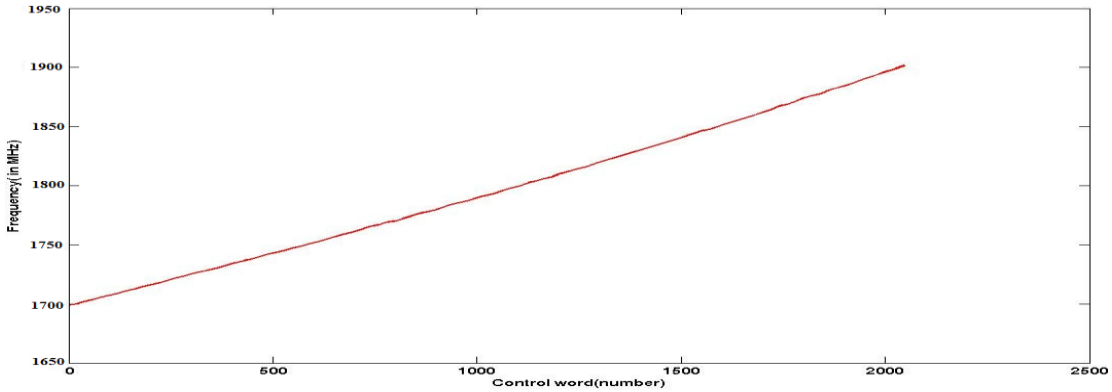

Figure 4.7.DCO characteristics for band two

Chapter 5

Design of Synchronous Phase Frequency Detector

5.1. Introduction

Phase frequency detector is one of the key component in the ADPLL circuits, because its characteristics strongly affects the whole performance, such as jitter and lock time. A synthesizer with capability of high operating frequency, low jitter and fast locking time has become the trend to achieve. Phase frequency detector is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the DCO output signal and the reference signal. PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals. Figure 5.1 shows a PFD with its inputs and outputs.

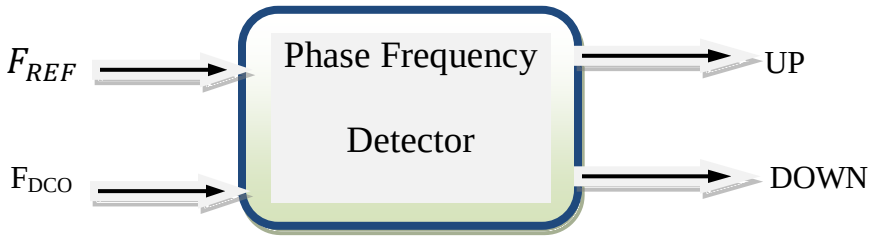

Figure 5.1 conventional phase frequency detector with its inputs and outputs

Sensitivity of the PFD means the smallest difference the PFD can detect and produce UP or DOWN signals that will affect the controller, this lead to the conclusion that the higher the sensitivity the better the PFD. One of the disadvantages that PFD suffers is dead-zone.

5.2. PFD architecture for high speed and high frequency application

Traditional PFD architecture, which consists of state machine such as flip flops, and NOR gates to provide reset path when both UP and DOWN outputs go high at the same time. But due to the reset path this design suffers from large dead zone. There are many topologies moving towards simplifying the circuit and reducing the dead zone. AND gate PFD and dynamic D-flip flop PFD, and dynamic D-flip flop with embedded reset NAND gate are the two mostly used topologies. In these topologies to reduce further the reset propagation time, the reset NAND gate was built-in the dynamic D-flip flop. Inverters are used as delay circuit to reduce dead zone in the NAND gate PFD.

A modified pre-charge type PFD is designed using TSPC to facilitate high speed and high frequency operation. TSPC D-flip flop is mostly used in designing D-flip flop of PFD for supporting high speed operation. To facilitate high speed and high frequency operation more, a simple CMOS with negative edge PFD is used. Since failing edge PFD uses less number of transistors, it preserves the main characteristics of the conventional PFD, consumes less power, has low dead zone, low blind zone and it can be effectively used in low power and high speed application, which makes it preferable for the targeted application of our design.

5.3. Making PFD outputs in synchronous with reference clock signal

As discussed before, the reference and DCO clocks are inputs to the PFD, and the PFD gives out UP and DOWN signals in synchronous with reference clock signal. If both **up** and **down** signals are high, the reset signal is activated and thus the error information is determined. The pulse width of the error information represents the phase difference of the two inputs. Figure 5.2 shows basic schematics of synchronous PFD.

In the figure, the clock inputs are inverted before applying to the conventional PFD so that the phase detection is done at the negative edge. Then the phase error is held till the next positive edge of the reference clock is sampled. During the transient state i.e. when both outputs are high, gates AG_3 and AG_4 removes this transient state. AG_4 output will be high only when up phase frequency detector block output and down phase frequency detector block output are high and low respectively. In the same way gate AG_3 output is high only when down phase frequency detector block output and up phase frequency detector block output are high and low respectively.

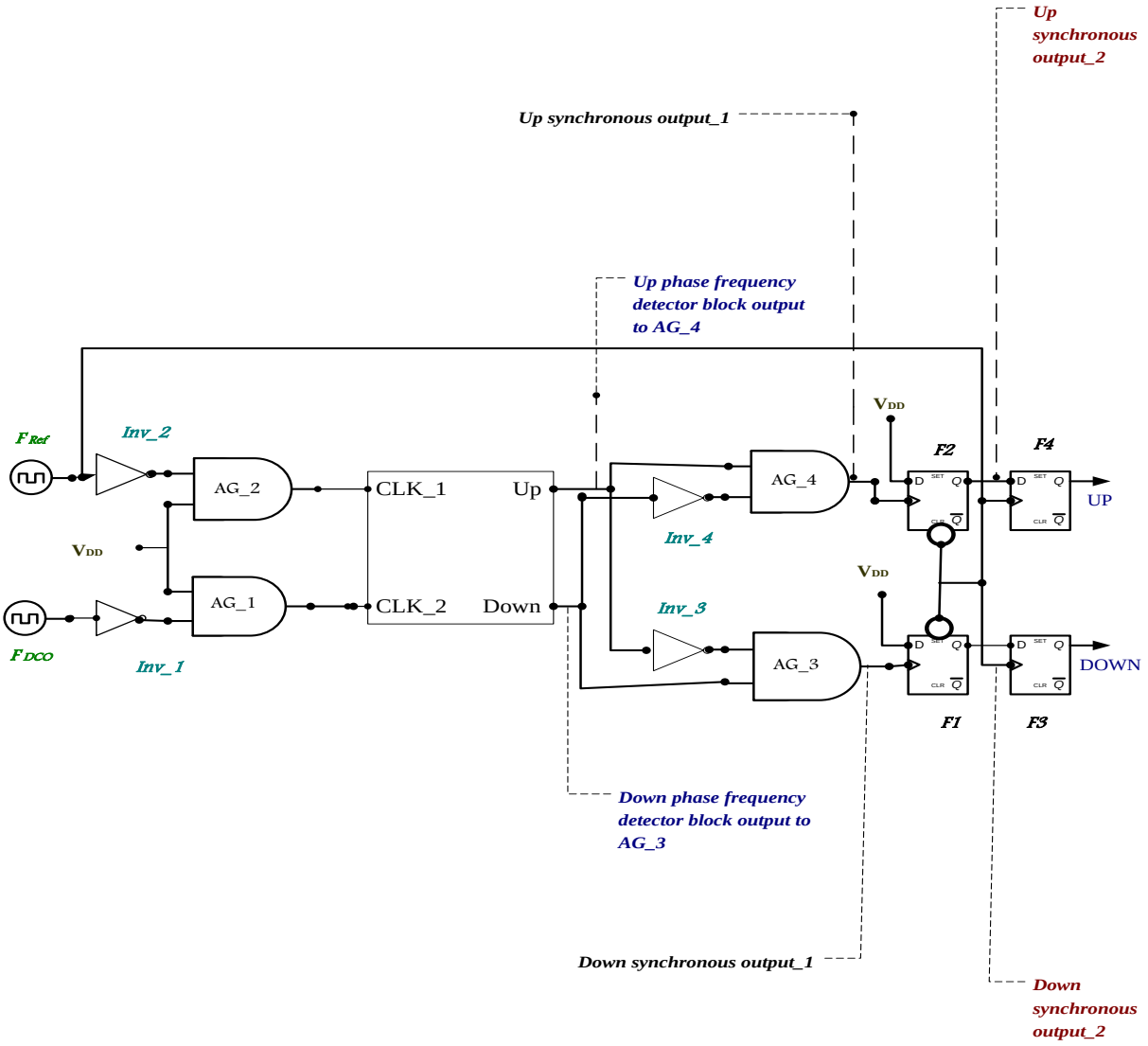

Figure 5.2 Basic schematics of synchronous phase frequency detector

With the negative feedback mechanism, PFD can control the output signal to be synchronized with a given reference input. At the condition of '11', the UP and DOWN are both high and hence no feasible condition in the state diagram. The following figure gives the state diagram of the previously shown synchronous PFD.

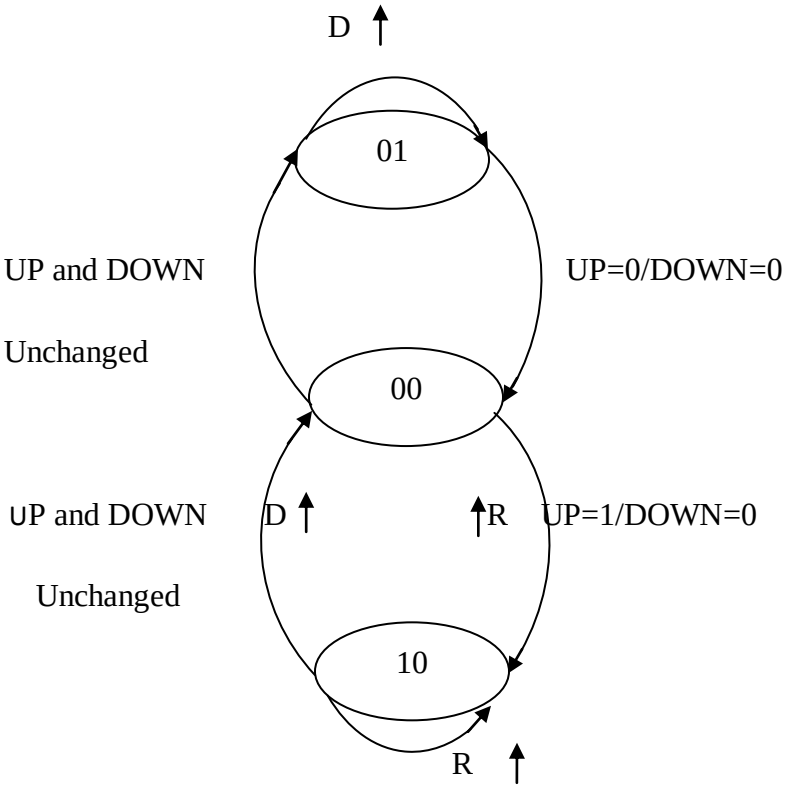

Figure.5.3.State diagram of synchronous phase frequency detector

In figure 5.2 flip flops F1 and F2 extends the outputs of AG_3 and AG_4 respectively to the negative edge of the reference clock. They are being reset by the negative edge of the reference clock. The output of F2 becomes high at the positive edge of up phase frequency detector block output and is held till the next positive edge of the reference clock. In the same manner output of F1 is an extended version of down phase frequency detector block output. Flip flops F3 and F4 samples the outputs of F1 and F2 respectively with respect to the reference clock and outputs DOWN and UP in synchronous with the reference clock.

5.4. Synchronous PFD implementation circuit

The synchronous PFD implementation circuit is designed in UMC 130 nm technology and the gates and flip flops from the Faraday Standard Cell Library are used. Figure.5.4 shows the complete schematics of synchronous PFD implementation circuit. But the setup time cannot be reduced considerably by the normal flip flop circuit. Since the D input to F1 and F2 are permanently tied high, the circuit can be simplified further. A True Single Phase Clock flip flop with only clock and reset inputs is designed to achieve a very low setup time. The TSPC flip flop circuit shown in figure.5.4 consists of 8 transistors.

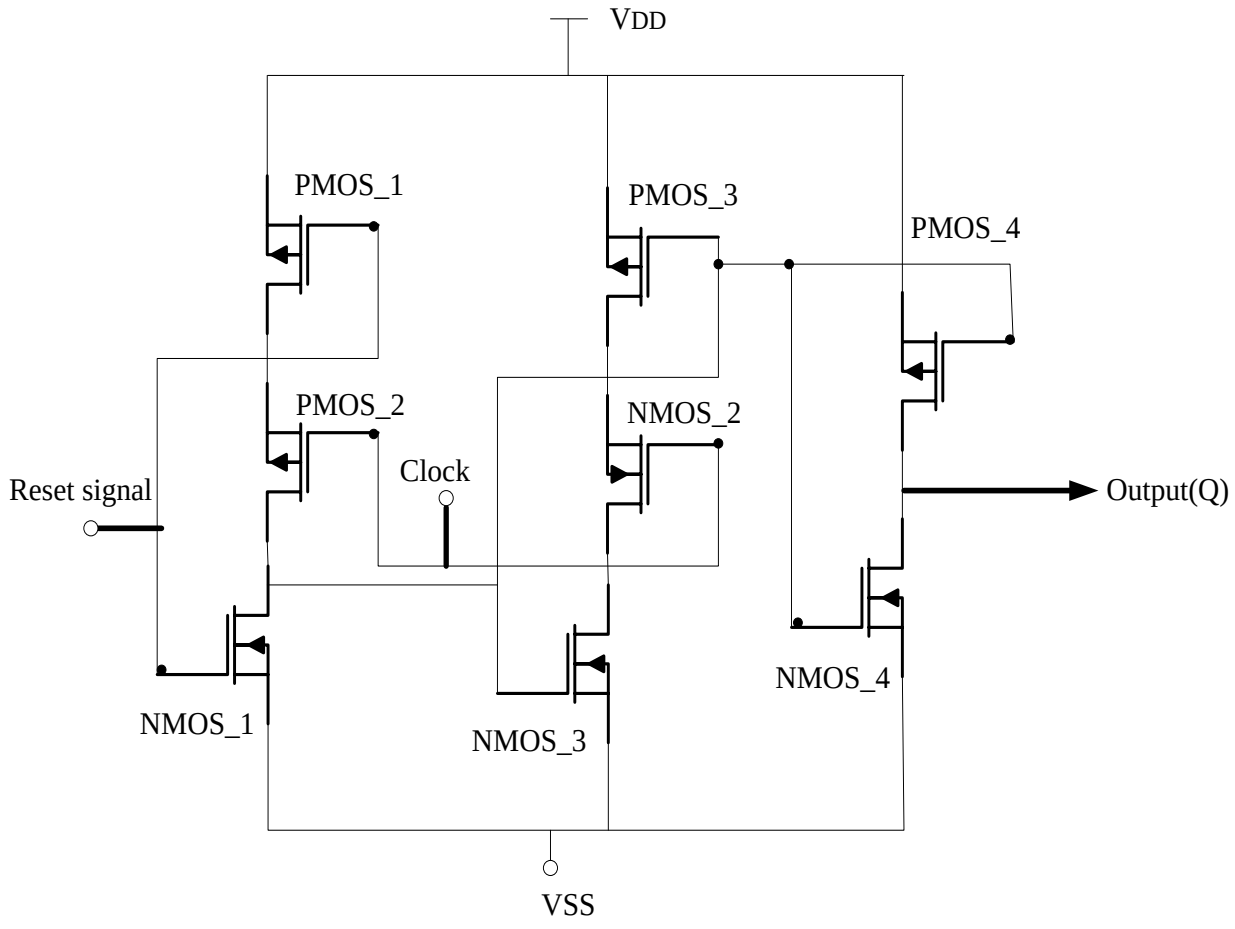

Figure.5.4. Shows true Single Phase Clock

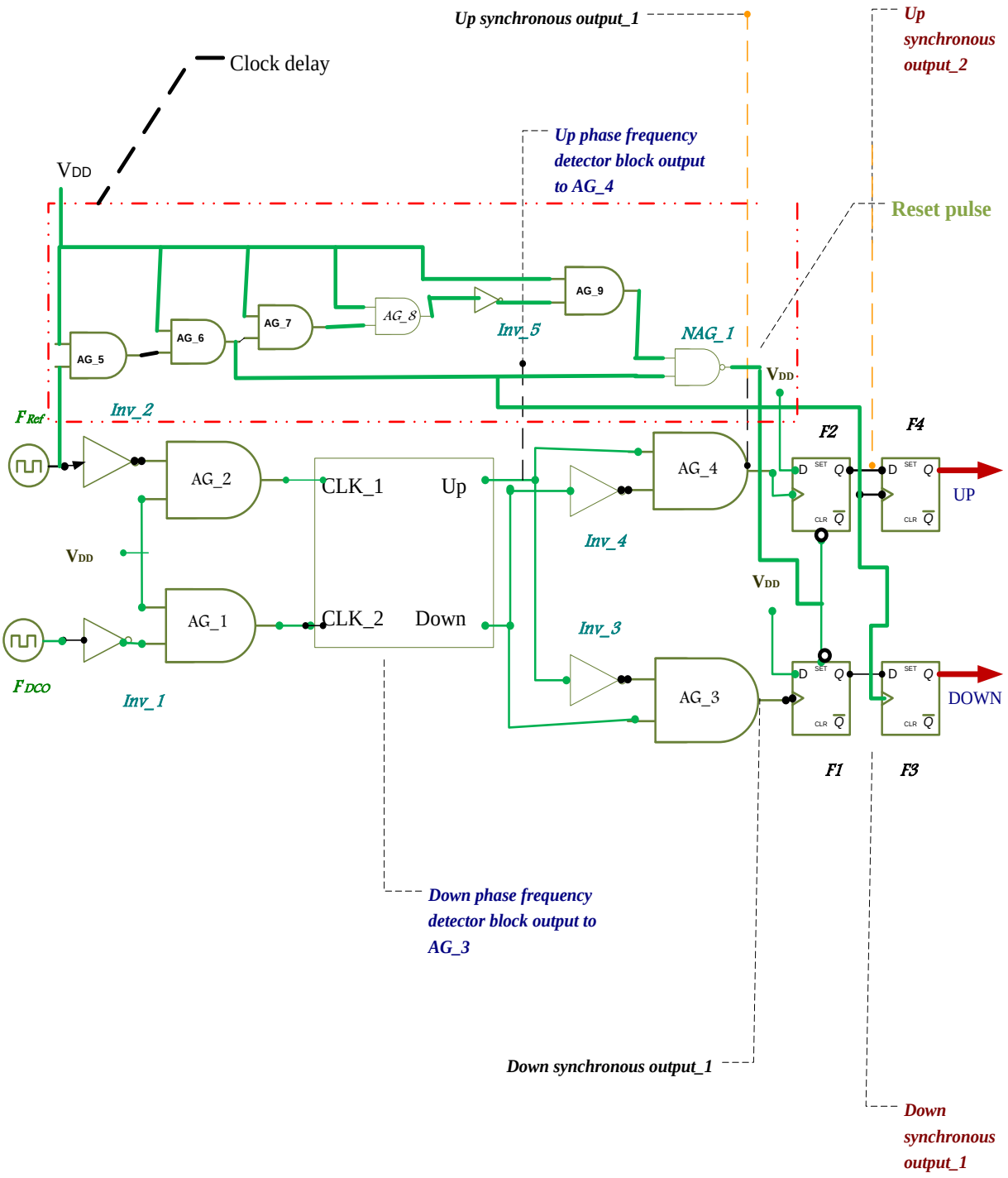

Figure 5.5.Basic schematics of synchronous phase frequency detector

To simplify further the PFD block, we need to show its gate level equivalent circuit. Figure 5.6 shows the gate level equivalent circuit of PFD block, which is implemented using NOR gates of identical drive strength.

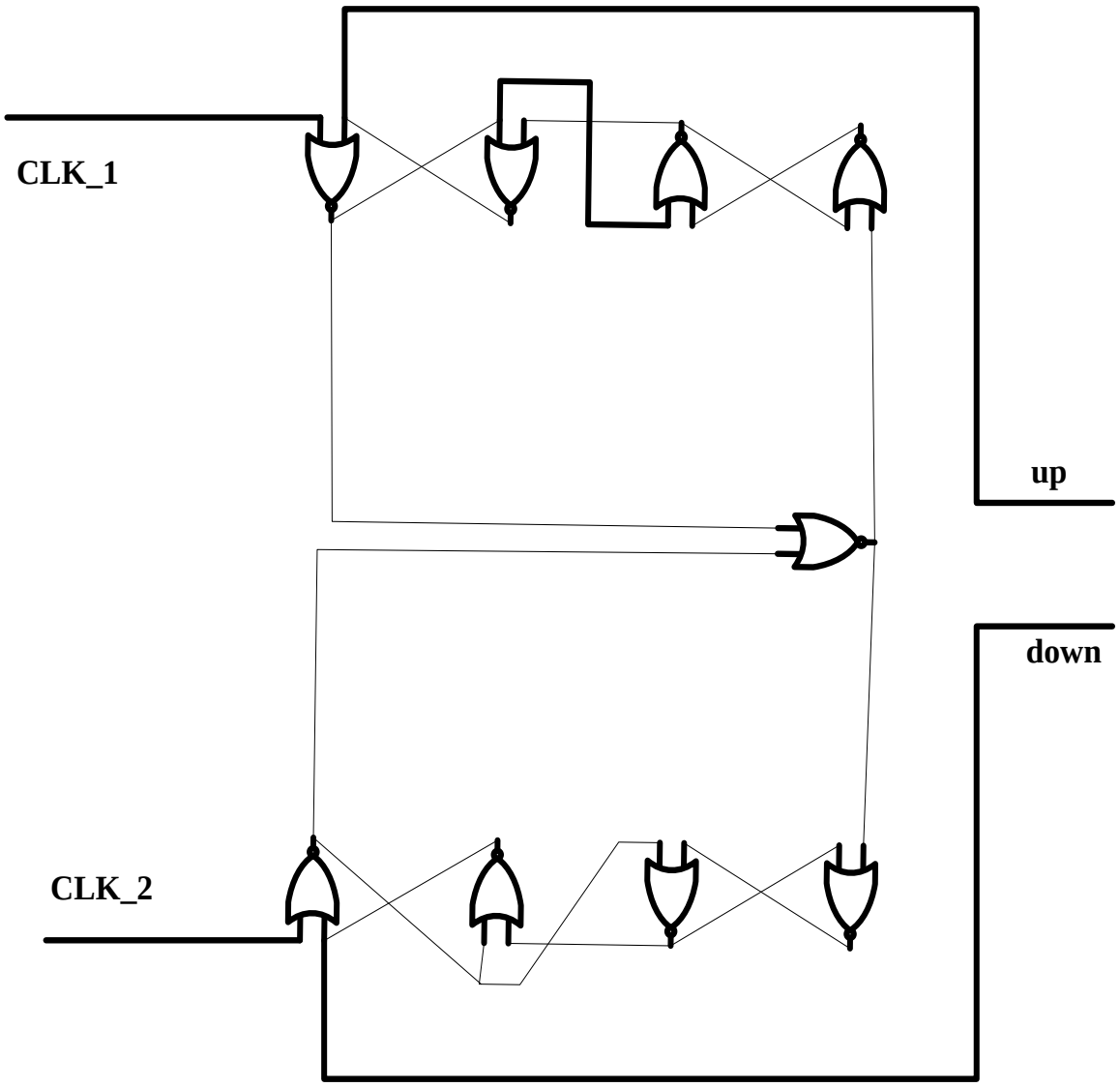

Figure.5.6. Gate level equivalent circuit of PFD block

In figure 5.5 flip flop F1 and F2 needs to be being reseted by the positive edge of the reference clock. But in the FSCL cells with simultaneous edge triggered clock and reset does not exist. To achieve this pulse of small width is generated at the reference clock edge using gates AG_5 to AG_9, and is applied to the reset input of F1 and F2. But because of the delays associated with AG_1, AG_2, AG_3 and AG_4, output signals of F1 and F2 are delayed with respect to the reference clock. To compromise this delay, the gates AG_5 and AG_6 are used. The delayed version of the reference clock is used to clock the flip flops F3 and F4.

5.5. Dead zone

As we mentioned before, dead-zone occurs due to small phase error. The reason of this problem is the delay time of the internal components of the flip-flop and the reset time that needs the AND gate to reset both flip flops. When the two clocks are very close to each other (small phase error), due to the delay time of the reset delay, the output signals UP and DOWN fail to charge and no output signal which lead to lose this small difference.

To mitigate the dead-zone issue, the reset signal inside the tri-state PFD can be designed to trigger pulses with a constant width at the PFD outputs when the phases of the inputs are aligned. However, since the circuits cannot work during the reset process, a blind zone, where the PFD cannot react to any transitions on the input signals, is inherent in the circuits. If the phase difference falls into the blind zone during the frequency acquisition, the PFD delivers incorrect phase information to the controller and shifts the phase toward the opposite direction, which aggravates cycle slips and elongates the frequency pull in time. The increased chance of cycle slips adversely affects the ADPLL frequency acquisition time and is undesirable in systems that require fast frequency transition.

During the reset process, the PFD cannot detect the leading signal, so it treats the next following lagging signals as the leading one and generates reversed phase information, which is called blind zone. To mitigate blind zone the widely adopted compensation technique using input delay cells is used.

5.6. Simulation of synchronous PFD implementation circuit

The final synchronous phase frequency detector implementation circuit is show in figure 5.7. In the circuit, TSPC and gate level implementation of PFD block is added. Simulation is done using spice simulation software. For convenience the simulation is done first by delaying the DCO clock. FDCO and FREF are given signals of same period and the delay between the two signals is varied. For each delay the value of UP and DOWN signals are measured. The dead zone is indicated by the absence of UP and DOWN signal even with phase error. Since the PFD measures phase difference at the negative edge and samples at the positive edge of the reference clock signal, the output is valid only after the second positive edge. Simulation result using Synopsys Design compiler shows that the total area is 360 um^2, leakage power and dynamic power, is 200nWand 2 mW and timing slack 0.42 psec.

By varying frequency or delay between the reference and DCO clock, simulation is done for four *scenarios*. *The first scenario* is DCO clock is made to lag the reference clock, but at the same frequency, which is shown in figure 5.9. In this case the DOWN output is high while the UP output is low. *In the next scenario* the reference clock is made to lag DCO but at the same frequency, as shown in figure 5.10. The result in this case is the UP output is high while DOWN output is low. In t*he third scenario* is the reference clock signal is made higher frequency, as shown in figure 5.11. The respective output of the UP signal is higher for more number of cycles compared to DOWN signal. In *the last scenario* the DCO clock is made higher frequency, as shown in figure 5.12. As shown in the figure, the respective output of the DOWN signal is higher for more number of cycles compared to UP signal.

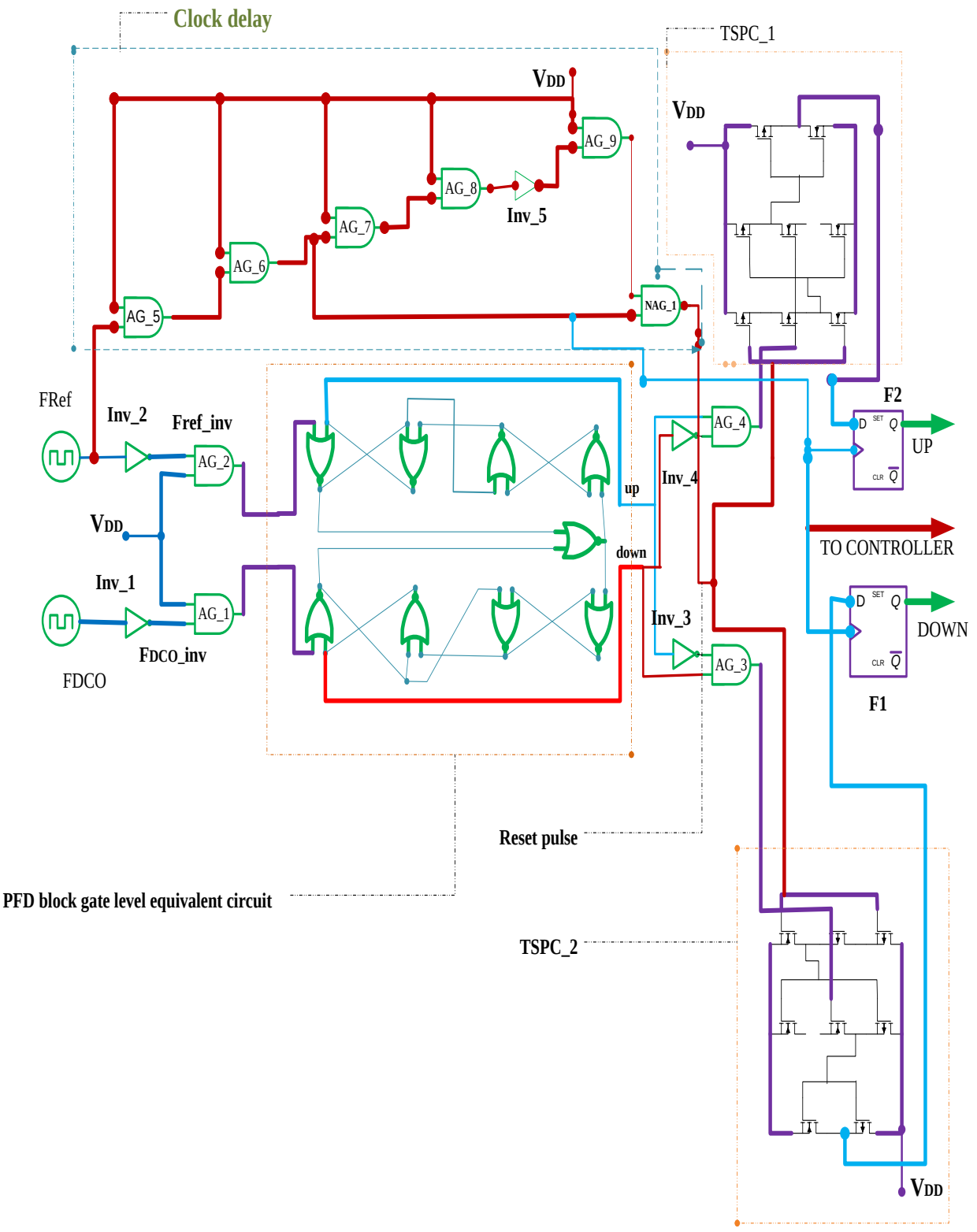

Figure.5.7. Final implementation circuit of synchronous phase frequency detector

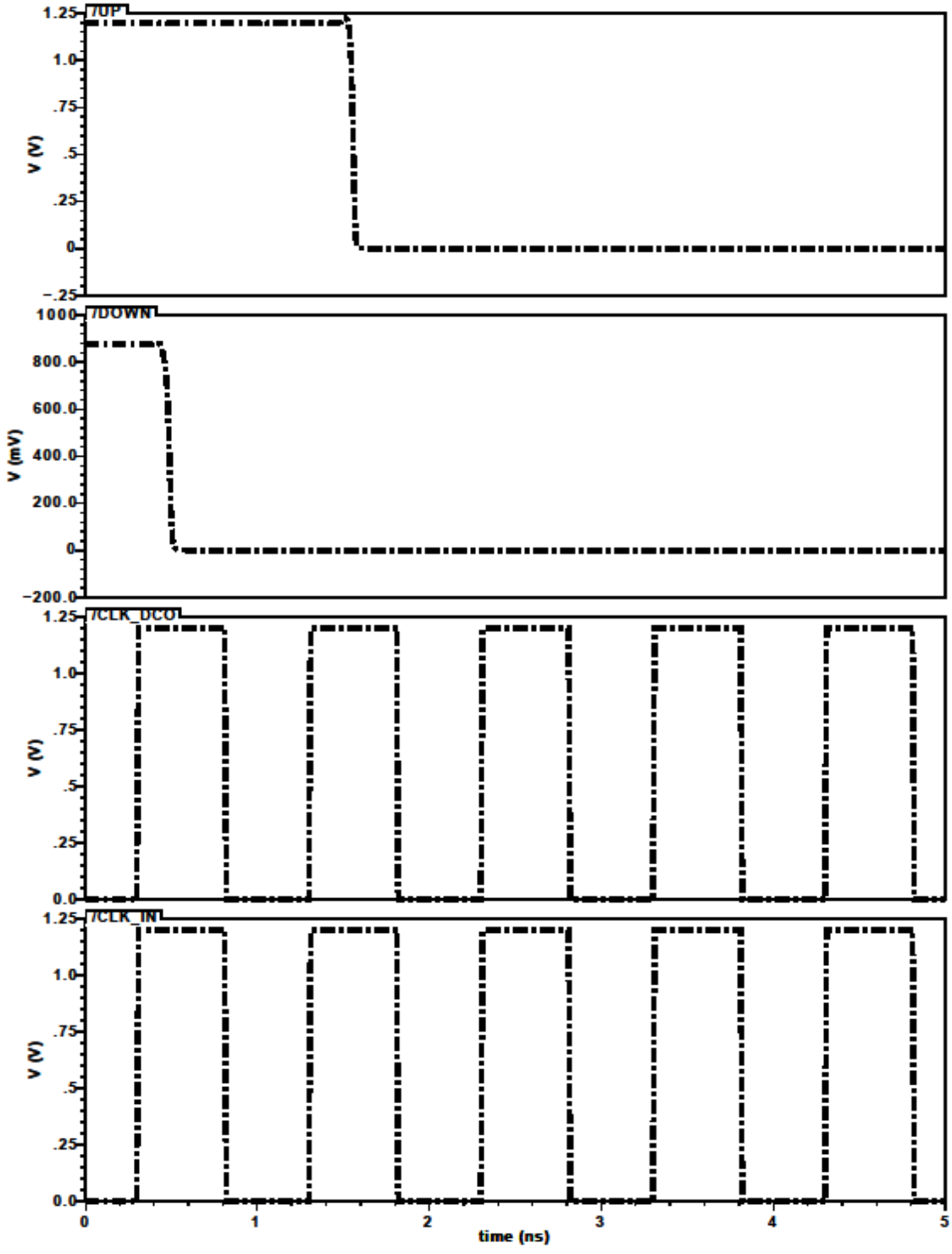

Figure.5.8 Phase frequency detector output for reference and DCO clock phase aligned

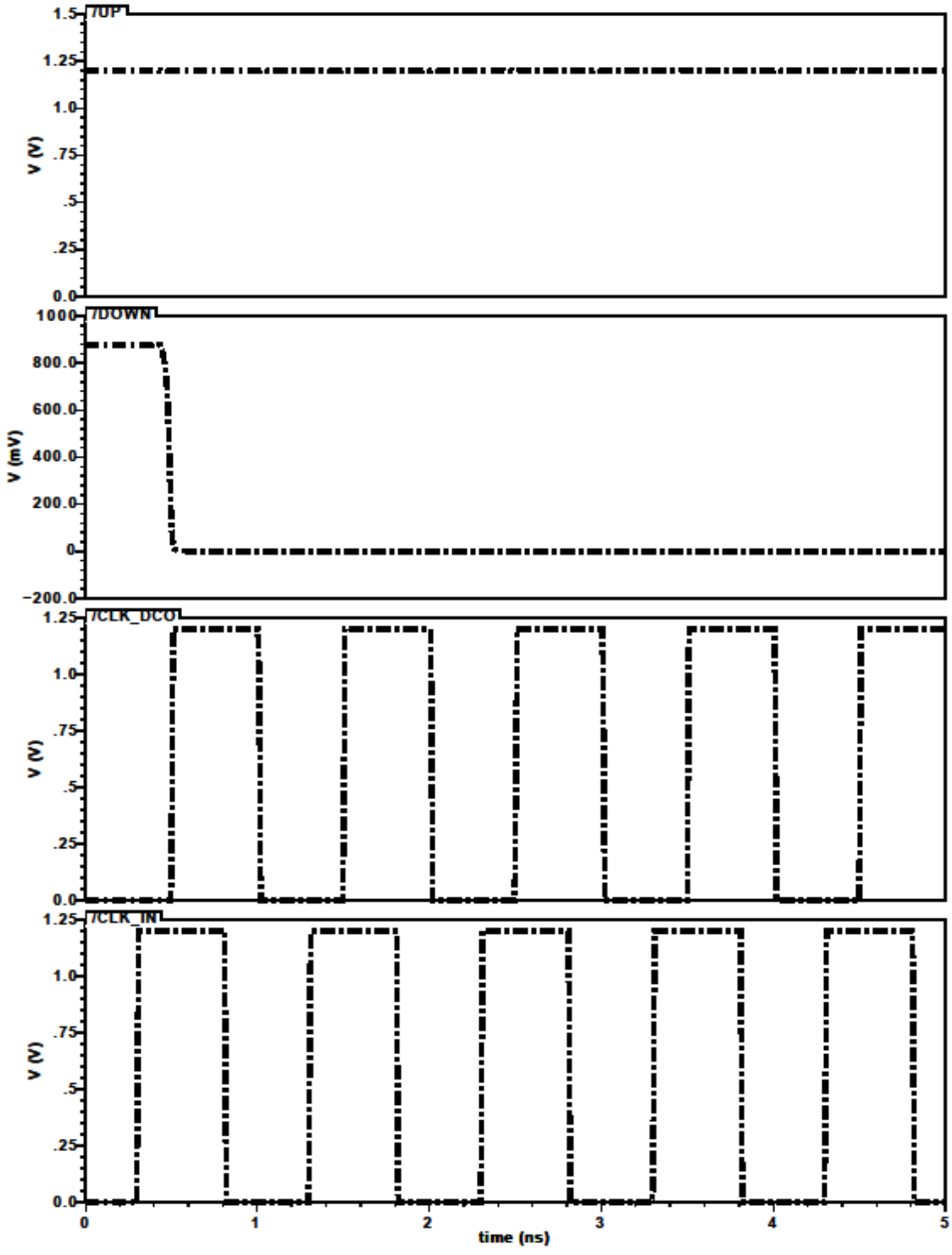

Figure.5.9 Reference clock leading DCO clock but same frequency

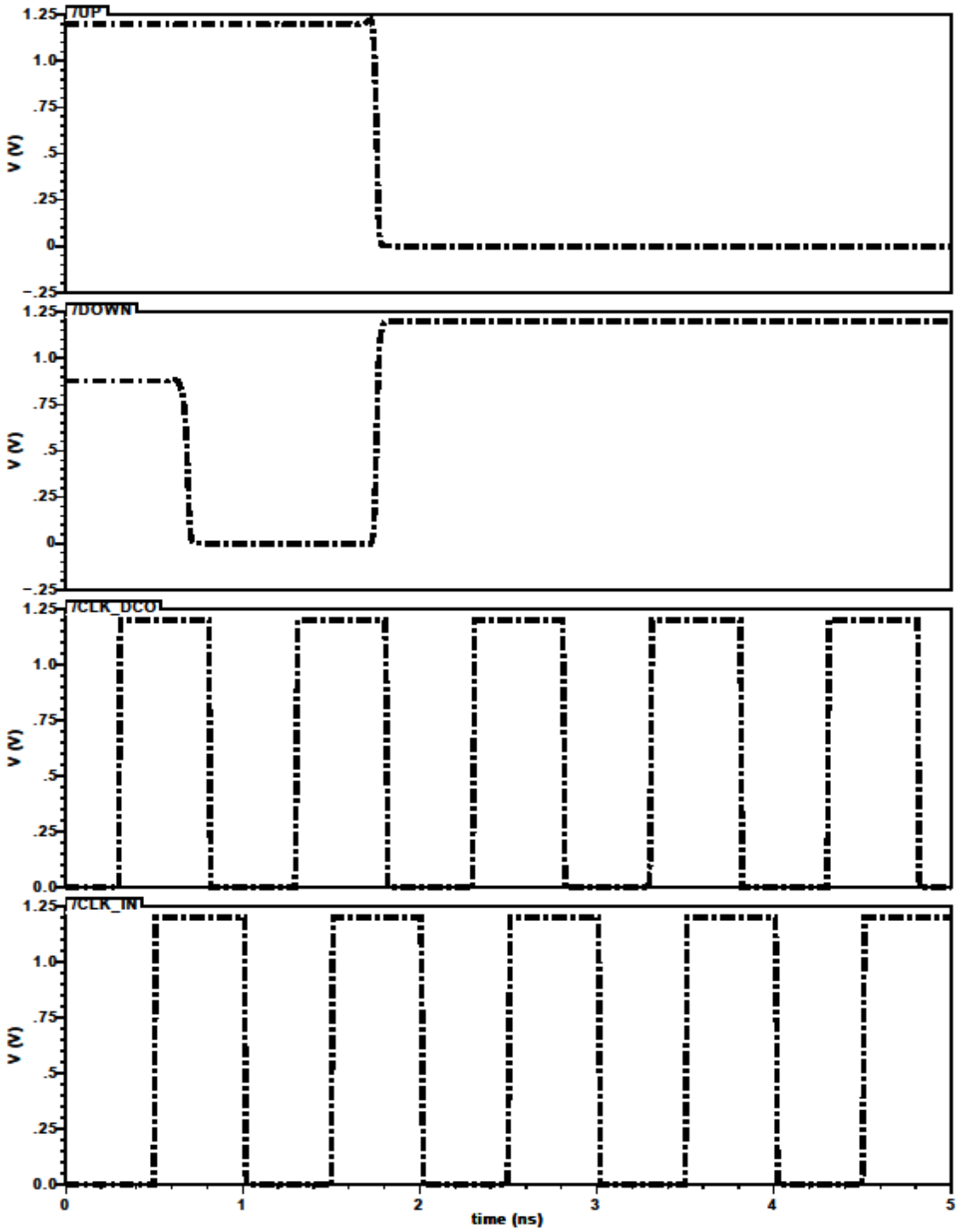

Figure.5.10 DCO clock leading reference clock but same frequency

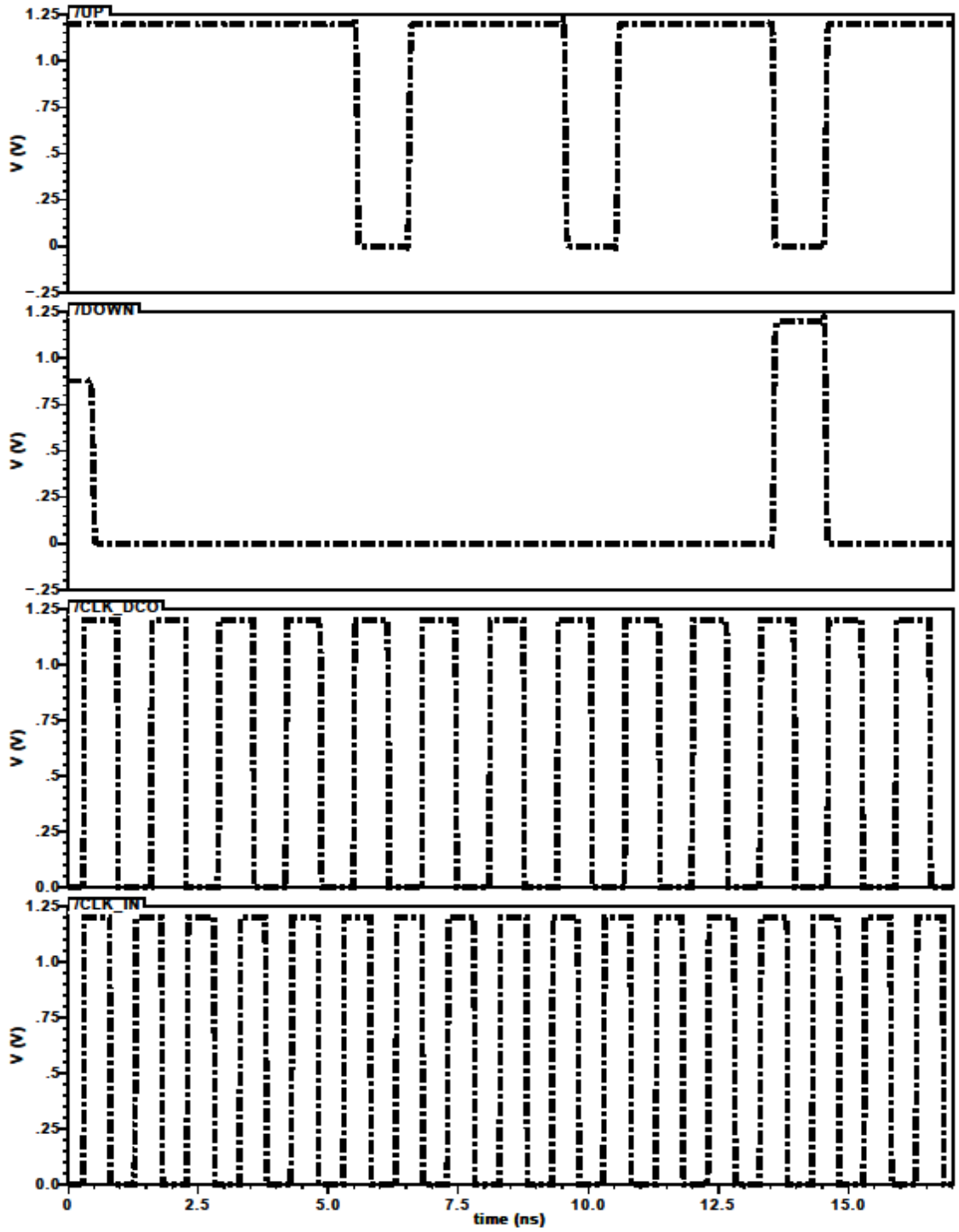

Figure.5.11 Reference clock at higher frequency

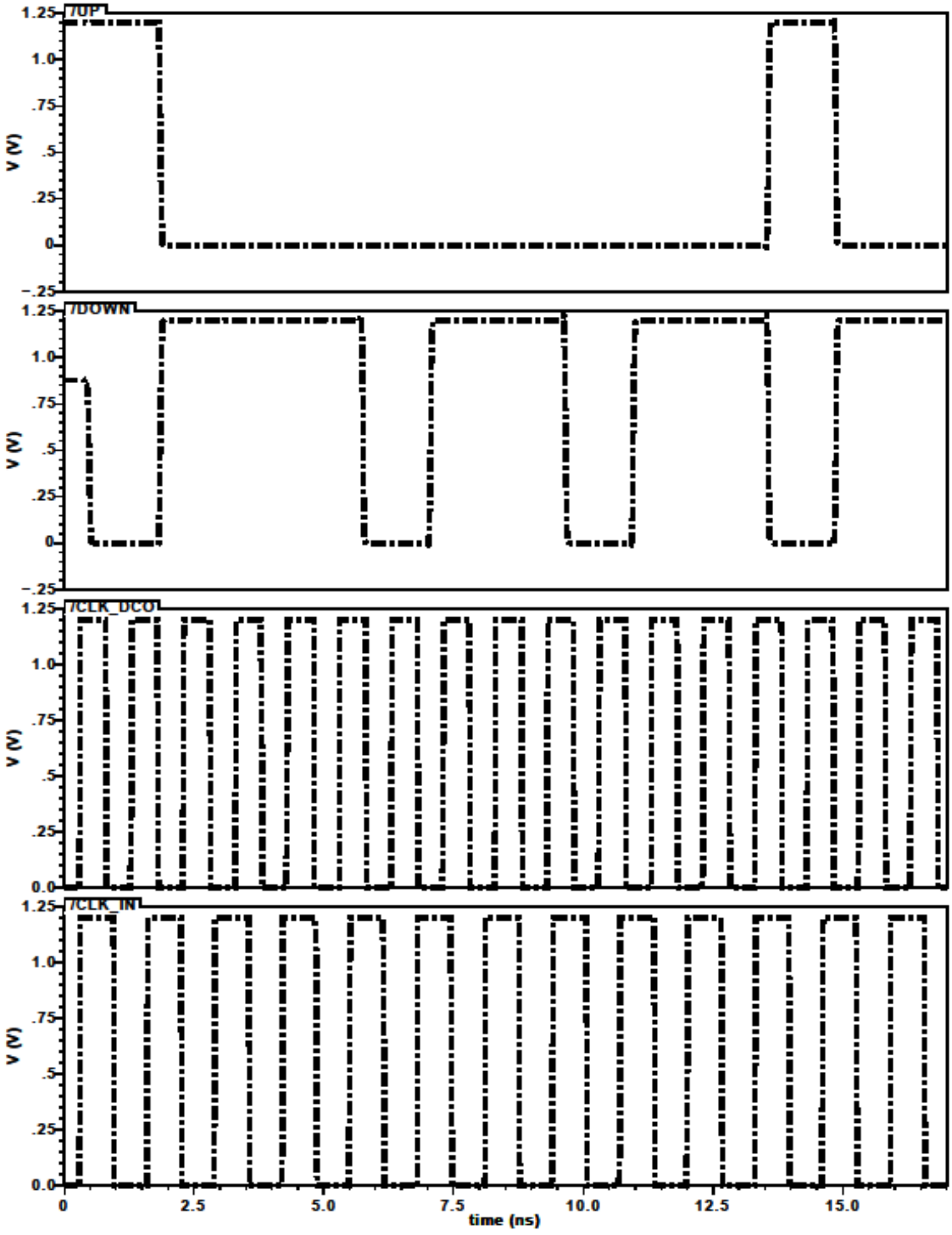

Figure.5.12 DCO clock at higher frequency

Chapter 6

Design of Digital Controller

6.1. Introduction

The digital controller used in the all digital lock loop provides the digital control access in the circuit. It takes UP, DOWN and CLK_OUT_BUF as input signals, which are the final out puts of the synchronous phase frequency detector, as shown in figure 6.1.

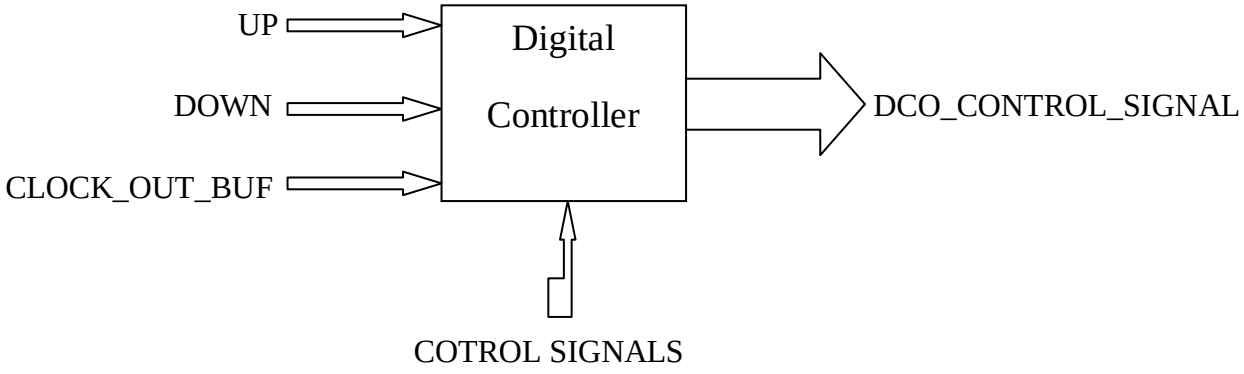

Figure.6.1. Digital controller block illustration

In addition, serial clock and data inputs are provided to set the parameter C during testing. The active low RESET signal given to the circuit is used to clear the part outputs. Figure 6.2 shows the digital controller schematics.

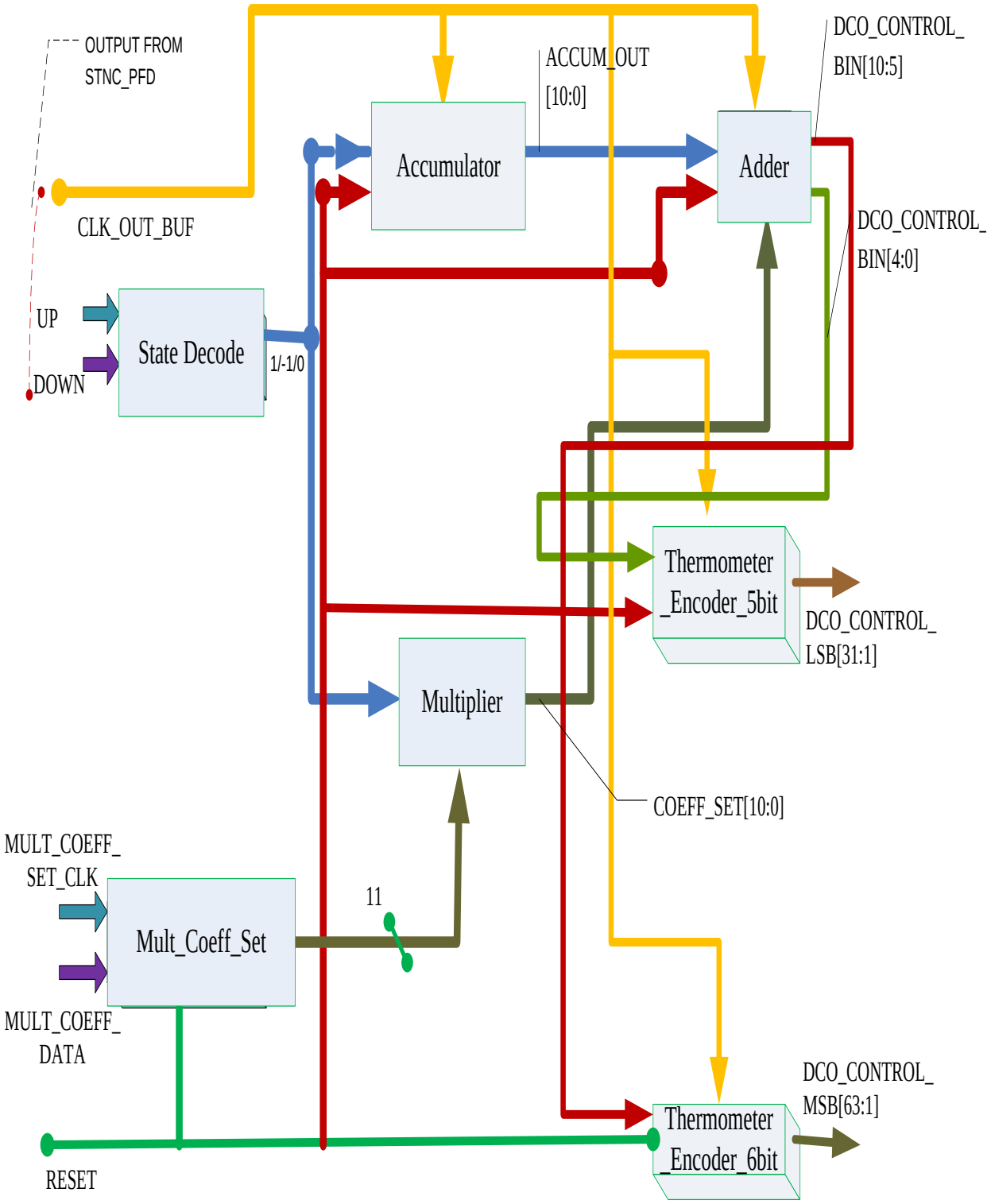

Figure 6.2 Digital controller schematics

6.2. Digital building blocks used in the Digital Controller

In this design the digital controller contain the following parts to achieve its full and desired functionality

6.2.1. Accumulator

The accumulator part essentially composed of a register, which stores the previous clock outputs, and an adder, which adds the current input to the values stored in the register. When UP is high, the accumulator output increments by one in every clock cycle. In the same way, when the DOWN signal is high, the accumulator decrements by one. Moreover, if both UP and DOWN are zero, the accumulator output remains unchanged. This can be implemented as eleven (11) bit UP/DOWN counter with the UP and DOWN signals determining the counter mode. The possible occurrence of overflow or underflow when the counter reaches 2047 or 0 respectively results in sudden undesirable jumps or dips in the accumulator output at the extremes. To overcome the underflow, once the counter reaches zero, the output is held to zero even if further DOWN signal arrives. Similarly for overflow, the counter doesn't increments after 2047 with UP signal.

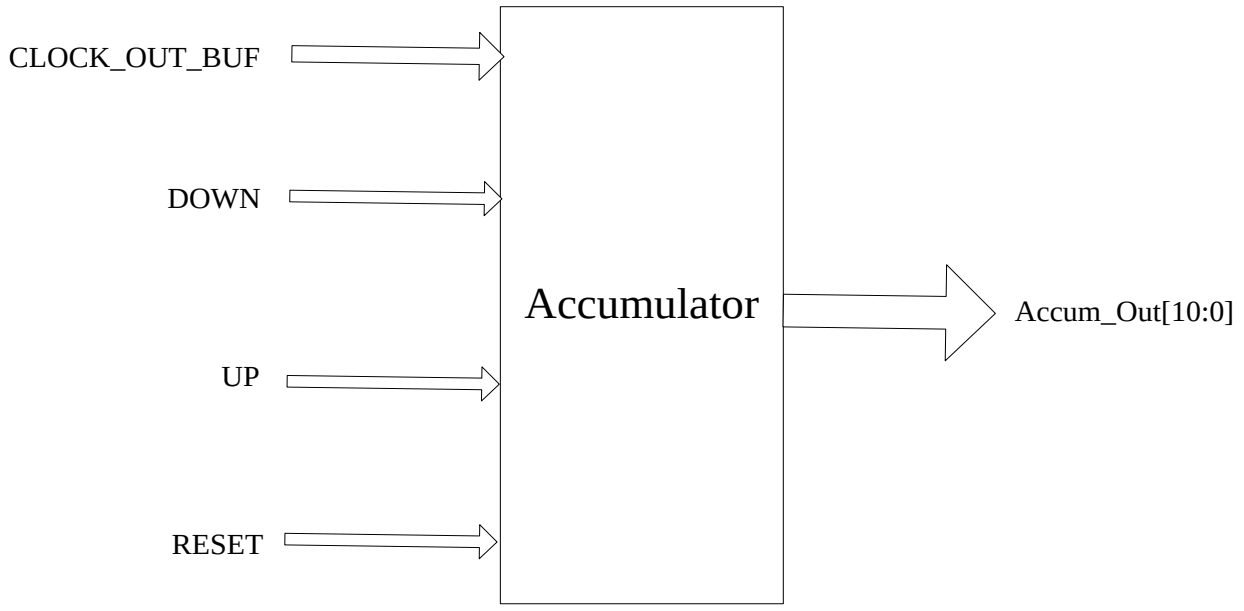

Figure 6.3.Accumulator block input outputs

6.2.2. Adder and Multiplier

The multiplier takes UP and DOWN as inputs, and gives out C, two's complement of C or zero at the respective inputs. When the UP signal is high, the multiplier should output C. When the DOWN is high, the output will be two's complement of C. When both UP and DOWN are low, the output is zero. The adder takes as inputs and sums the multiplier output and accumulator output to generate the eleven (11) bit digital controlled oscillator control word. As like in the accumulator, the possible occurrence of overflow or underflow leads to unstable control word. So if the adder output is greater than 2048 or less than zero, the control word should be held to 2048. The carry bit from the adder is used to check for overflow as well as underflow. The following figure shows the implementation schematics;

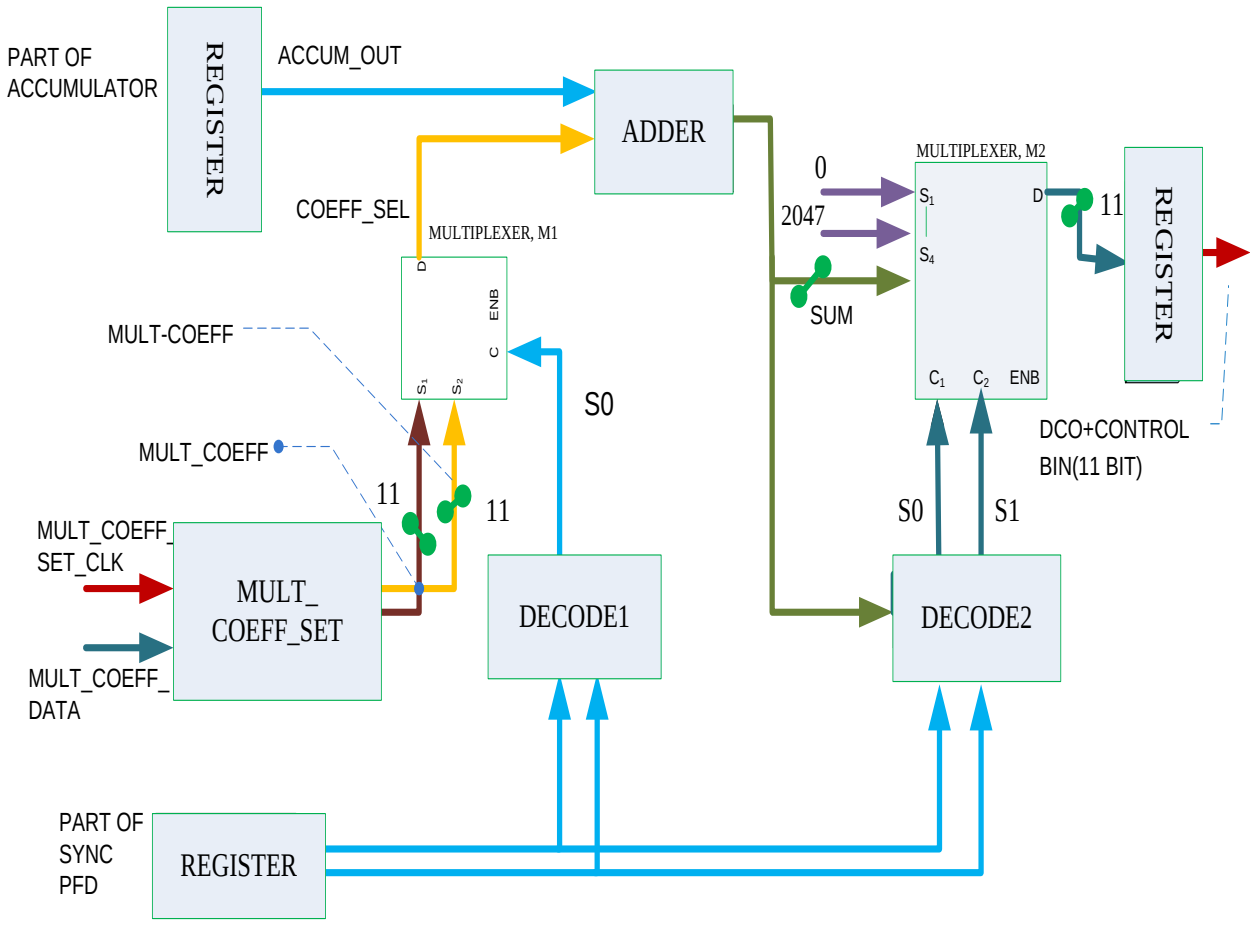

Figure.6.4 the implementation schematics of adder and multiplier

As shown in the implementation schematics of adder and multiplier, the critical path includes multipliers, M1 and M2, adder and the two registers, R1 and R2. The critical path delay is close to one nano second and can lead timing violations during the routing stage. So to overcome this problem, the actual implementation is given below.

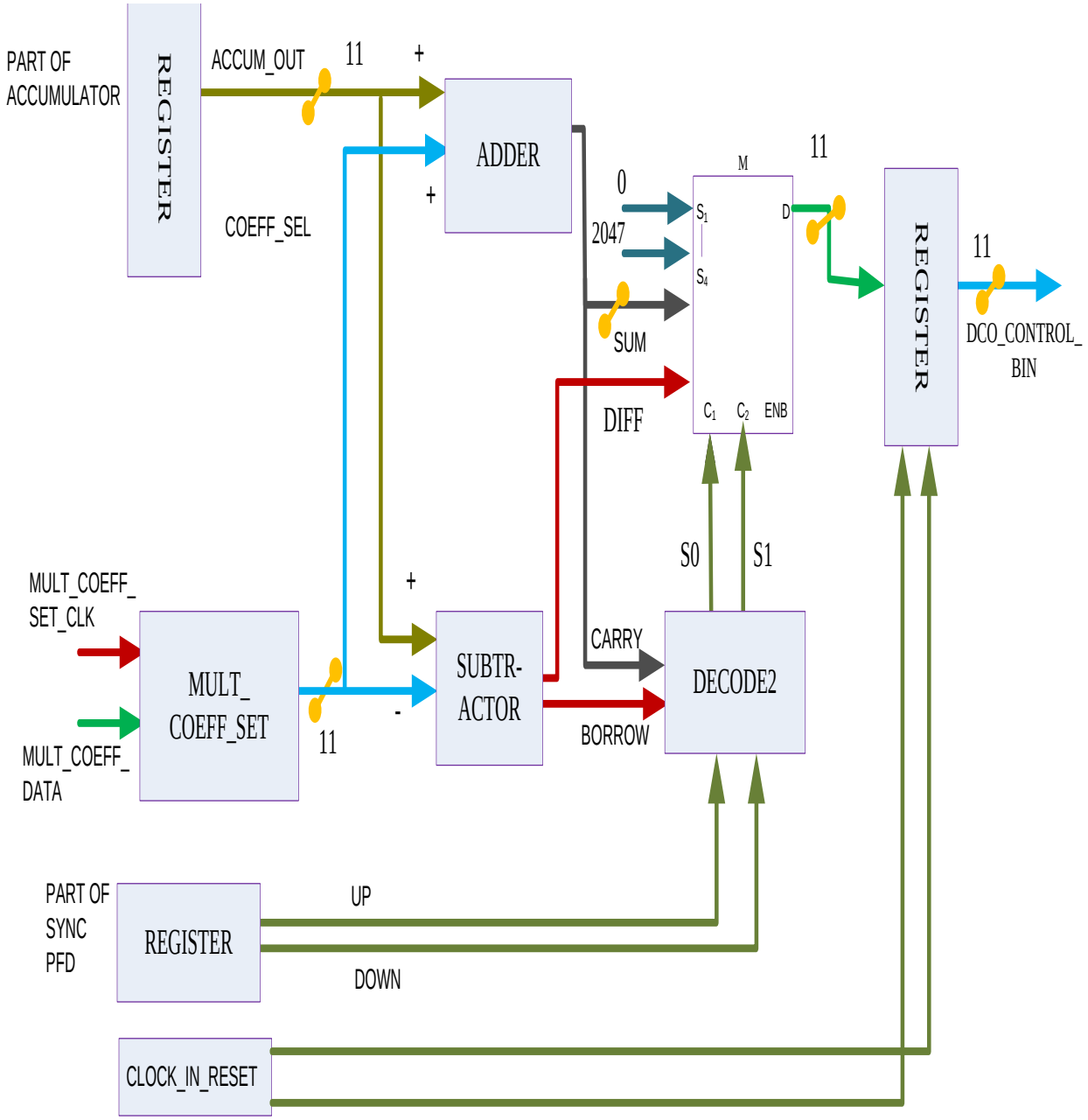

Figure 6.5 Adder and multiplier final implementation schematics

The constant C is added to or subtracted from the accumulator output irrespective of UP or DOWN signals. The selector for the multiplexer M2 is generated by the carry bit from the adder and subtractor along with UP and DOWN signals. Thus by adding a subtractor in figure.6.4, multiplexer M1 can be removed and the delay is reduced. As show in figure 6.5, multiplexer is followed by a register clocked by CLOCK_OUT_BUF and cleared by the active high RESET input. Similarly the serial clock and data pins are used to set the value of C before initialization. After all, the C value is stored in a serial and parallel out register clocked by the serial clock. So it takes eleven serial clock cycles to initialize the constant C.

6.2.3. Thermometer Encoder

The thermometric encoder is a specific decoder that generates the digital word which controls the DCO. As discussed in the previous section, the thermometer encoder has two segments, a 5 to 31 line encoder for the LSB, and a 6 to 63 line encoder for the MSB. That is for a binary word of N, N lines in the encoder output will be zero while 31-N line for LSB or 63 – N lines for MSB will be one. The output of the encoders is registered before giving to the DCO so that the intermediate transitions do not affect the DCO and create unwanted frequency changes. The following figures show cumulative schematics of the thermometer encoder.

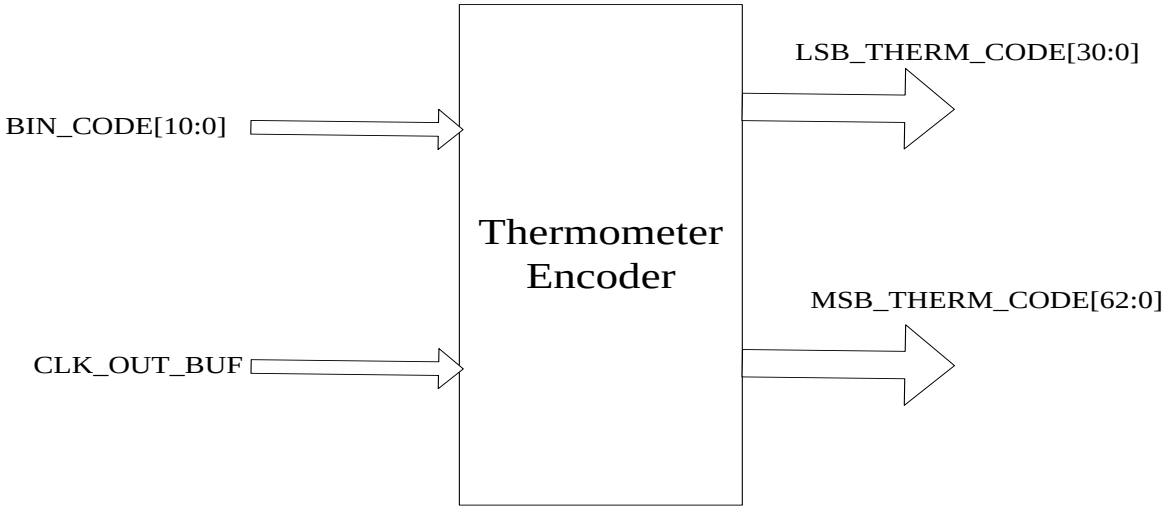

Figure.6.6. the schematics of thermometer encoder

6.3. Digital Controller Implementation

The digital controller is implemented in VHDL. In the implementation process, VHDL implementation and test bench code are synthesized for the accumulator, adder, thermometer encoder, mult_coef_set, DCO_control and PFD. In addition, synthesis to analyze and optimize timing, area and both leakage and dynamic power is done using Design Compiler of Synopsys, which is targeted for Faraday Standard Cell Library in the UMC 130 nm Technology. The design meets a clock period of 1 nsec and 0.56 nsec for band 1 and band 2 respectively. The extra slack helps the timing closure after placement and routing. The total cell area is 92.6 *89.6 um^2. The worst case dynamic power is 3.4 mW and leakage power is 1.67uW. Pre-synthesis and post synthesis simulation is done by ISim and testing is done for different scenarios of UP and DOWN signals. The timing analysis and the area analysis is done and for the possible conditions. The following figure shows the synthesized schematics of the digital controller circuit.

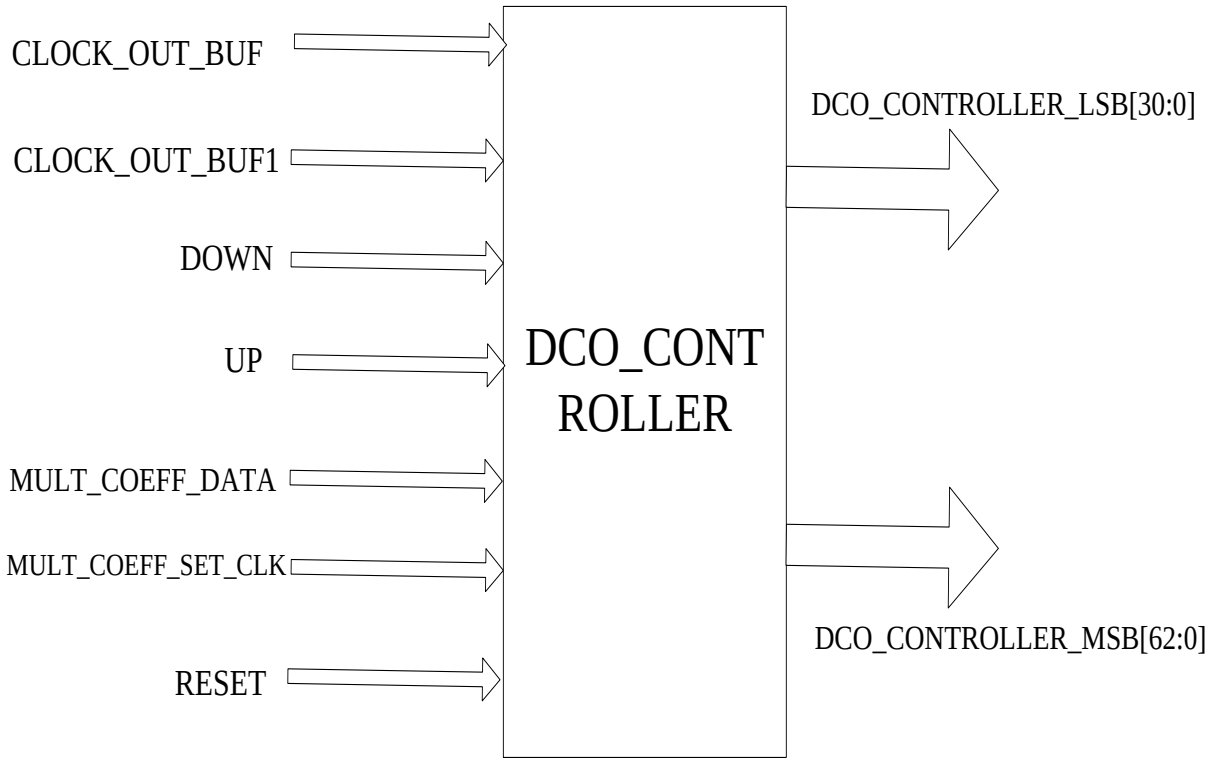

Figure 6.7 DCO_CONTROL module input and output

Chapter 7

ADPLL Integration and simulation

7.1. ADPLL Integration and simulation

The integrated schematics for ADPLL are shown in figure 7.1. The reference clocks are in the frequency range of 0.8 GHz to 1 GHZ, and 1.7 GHz to 1.9 GHz are provided. When the PLL gets locked, there will not be further UP and DOWN signals, and the binary control word will stabilize to the value which gives the same frequency at the DCO. The 11 bit control word is input to 11 bit ideal AHDL DAC module and the output control voltage is analyzed.

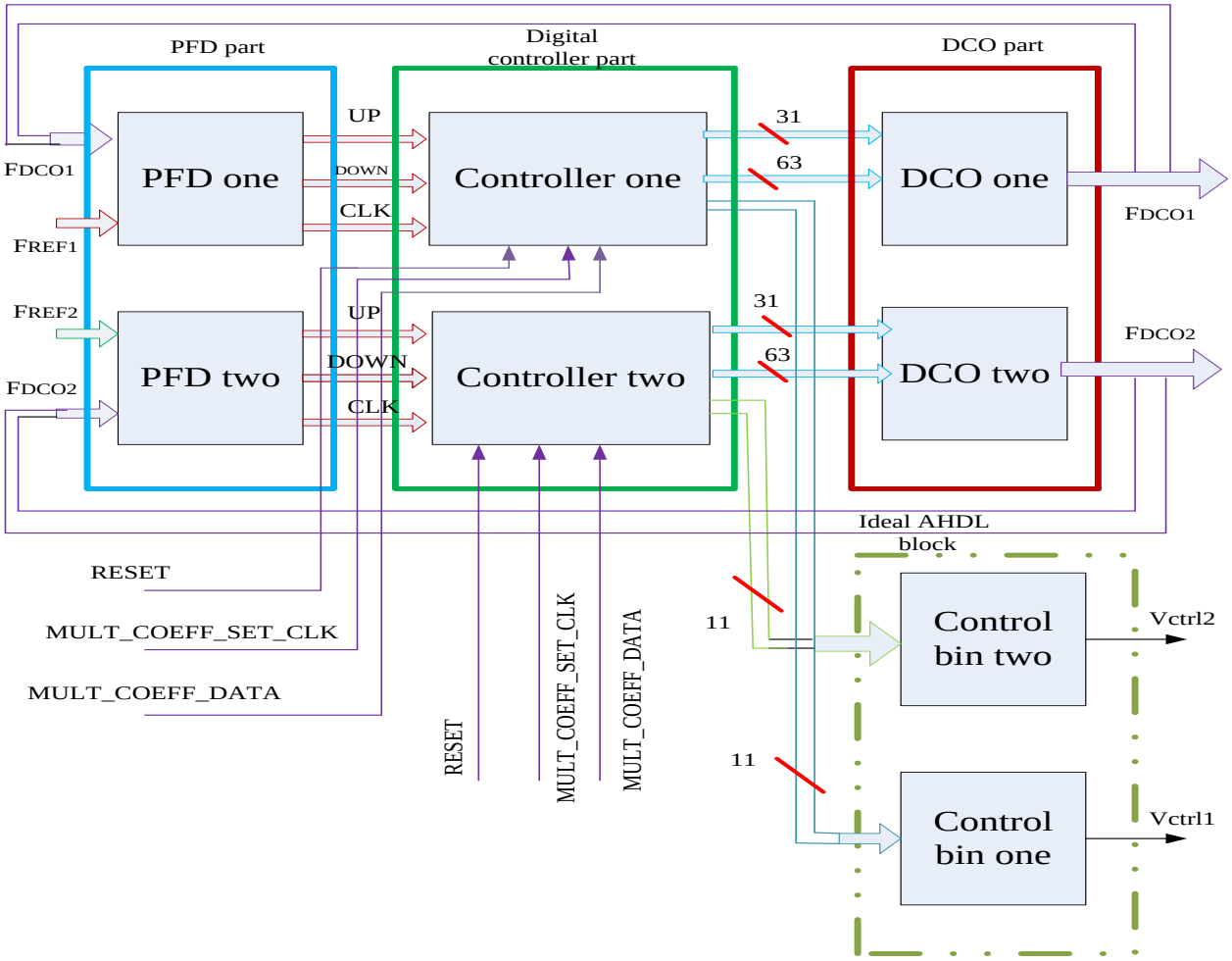

Figure 7.1.Integrated ADPLL schematics

The simulation results using spice tool for a center frequency of 1800 MHz is shown in figure 7.2 to 7.7. The output settles after 3.55usec. The PLL draws an average current of 13 mA. Since the DCO cannot give continuous frequency variations, for exact locking, the input frequency should be exactly equal to a frequency available at DCO. Otherwise the PLL will settle to the closest frequency, and the difference in frequency results in the PLL going out of lock once in a while. Figure 7.3 shows the variations in DCO frequency. There will be corresponding UP or DOWN signals and the loop will once again settle back into lock. The solution is to increase the frequency resolution. This can be achieved by reducing the C_{LSB} as shown in figure 4.3. Figure 7.2 shows at 1762 MHz reference frequency with peak voltage of 1.35v, the PLL locks and gives output frequency of same amount with reference frequency of 1.2v peak voltage amplitude.

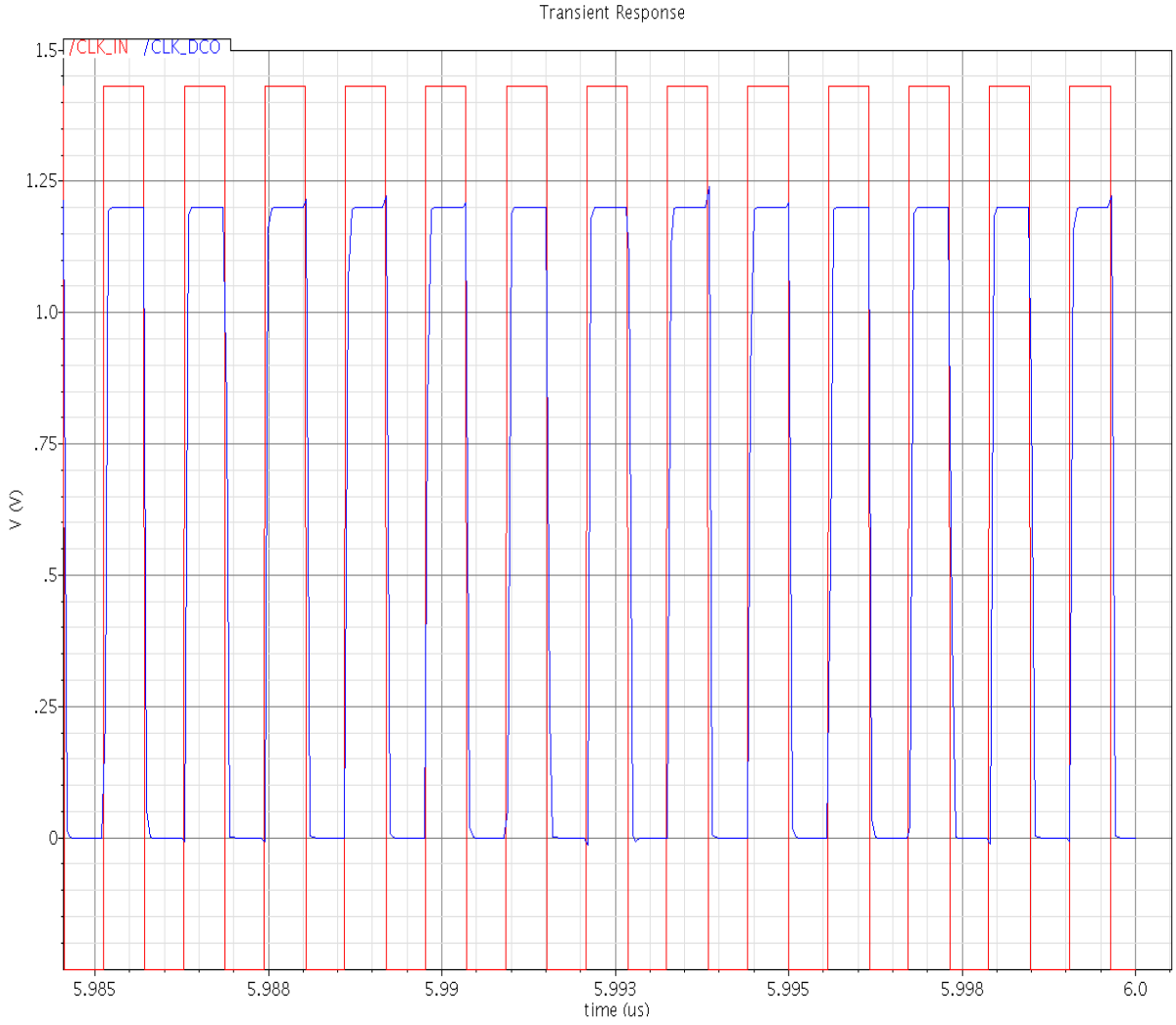

Figure 7.2.DCO locking transient response at 1762 MHz frequency

In figure 7.3, reference frequency of 1769 MHz, the PLL locks within 0.5ns, with a maximum peak voltage of 1.35v.

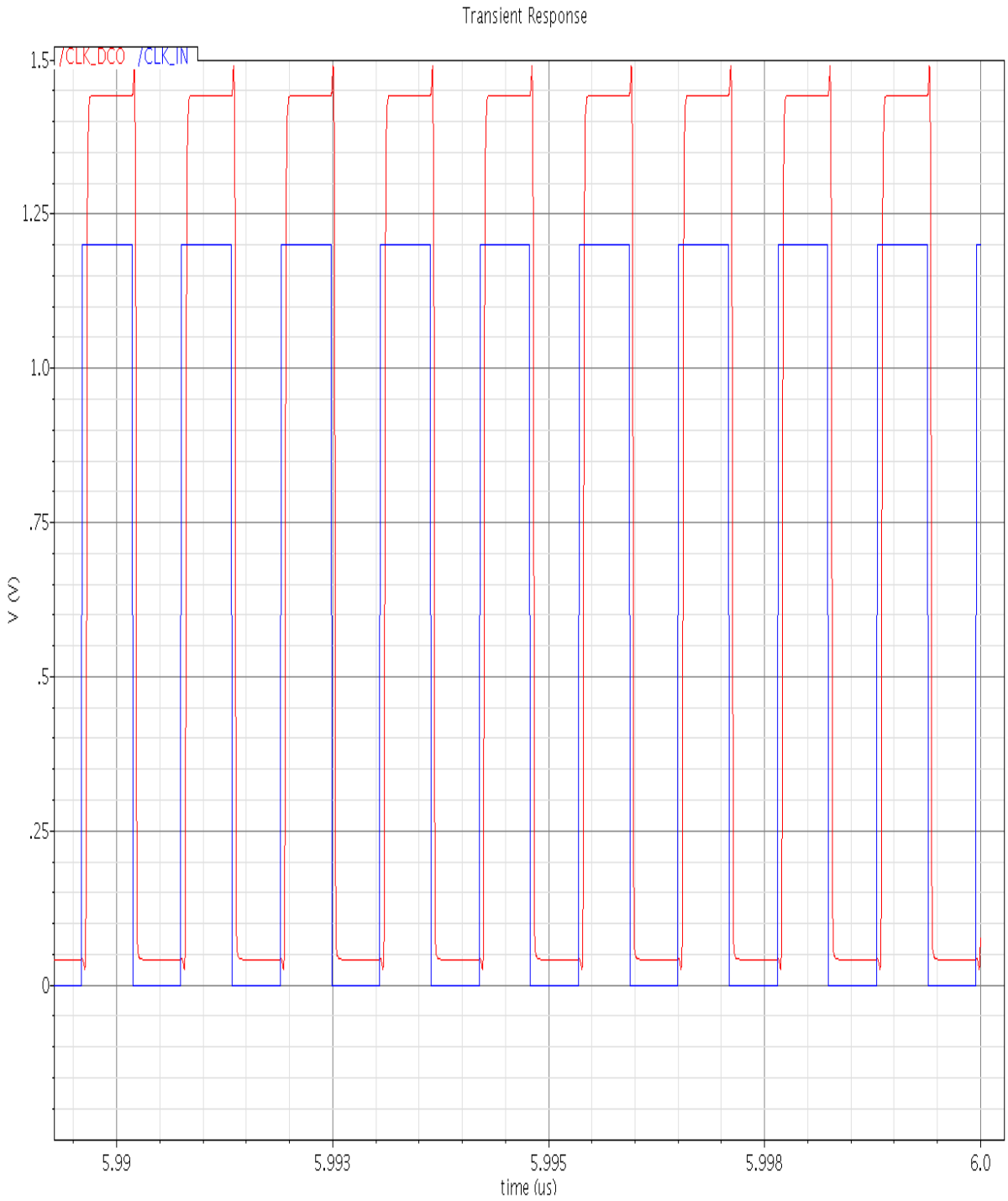

Figure 7.3.DCO locking transient response at 1769 MHz frequency

Figure 7.4 show the locking of PLL, with the minimum required control voltage of 0.4V at 4.36us, at band one center frequency.

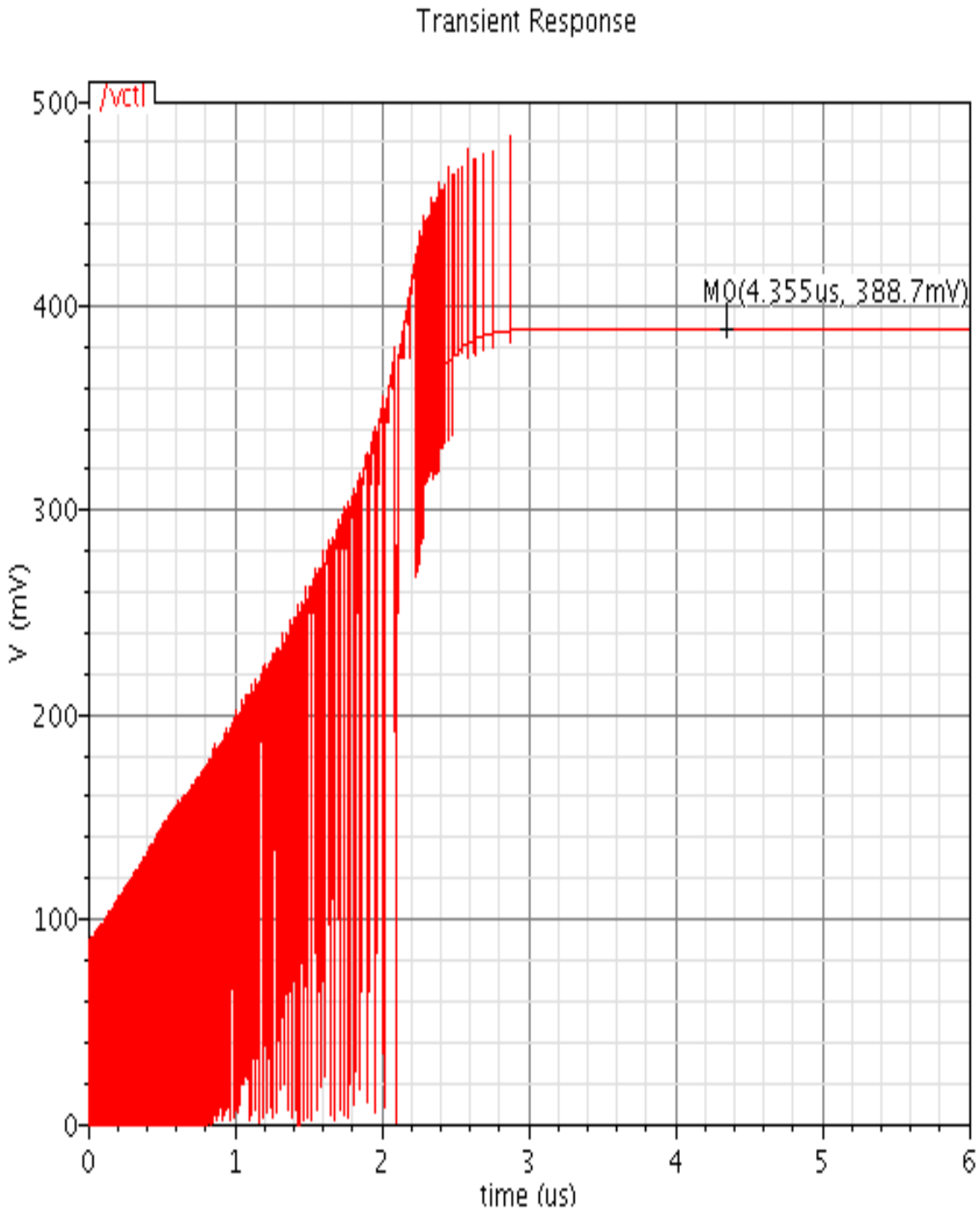

Figure 7.4.DCO output transient transient response at 1769 MHz frequency

Figure 7.5 shows the locking of PLL at center frequency (F_0) of 1800 MHz, with reference frequency at same voltage as DCO frequency of 1.2v, and the PLL locks at 0.5ns.

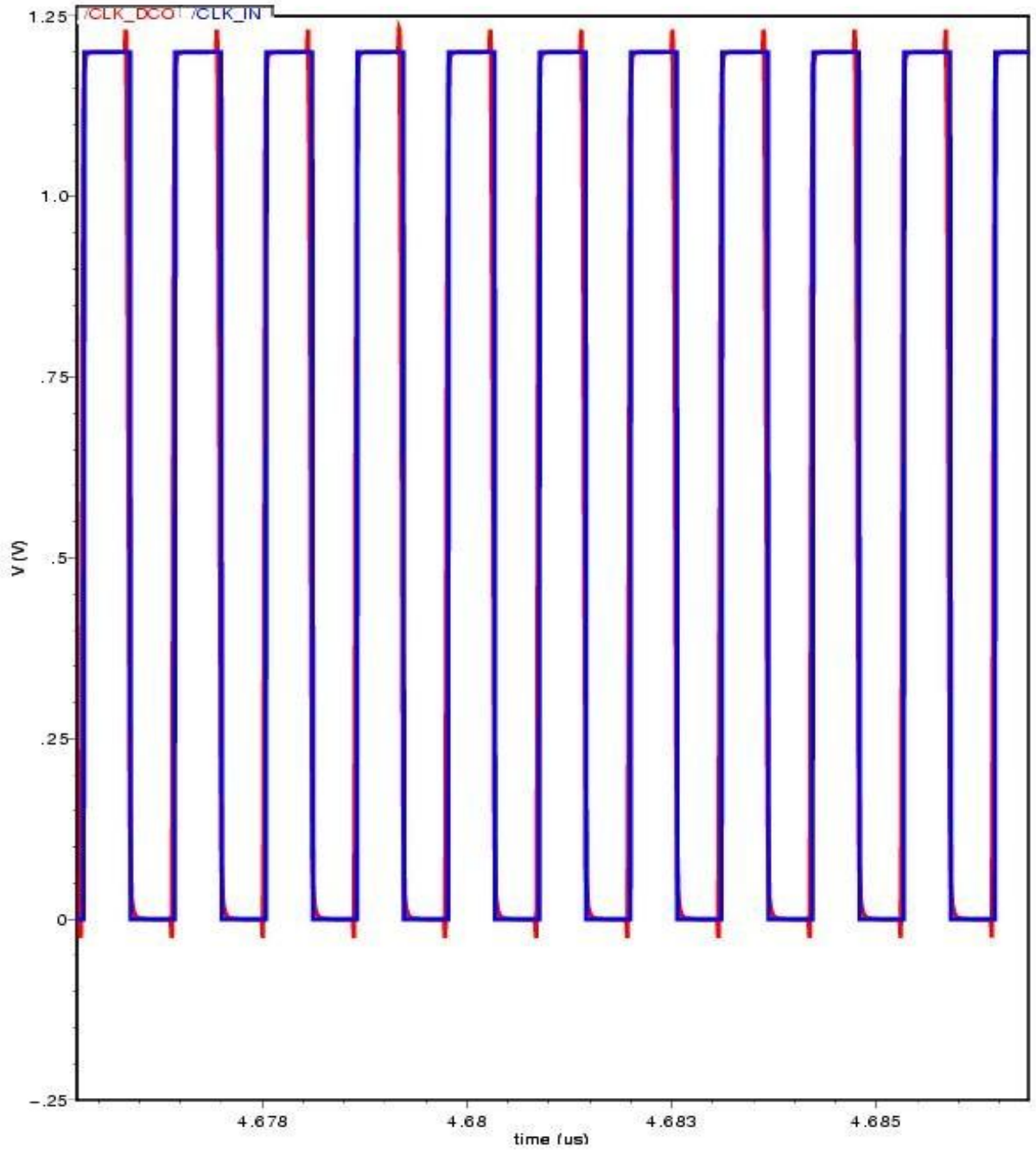

Figure.7.5.DCO locking transient response at band two center frequency

Figure 7.6 shows the locking of PLL with a maximum of 1.2v peak voltage and settling time of 3.6us, with reference frequency of 1800 MHz and 1.2v peak voltage.

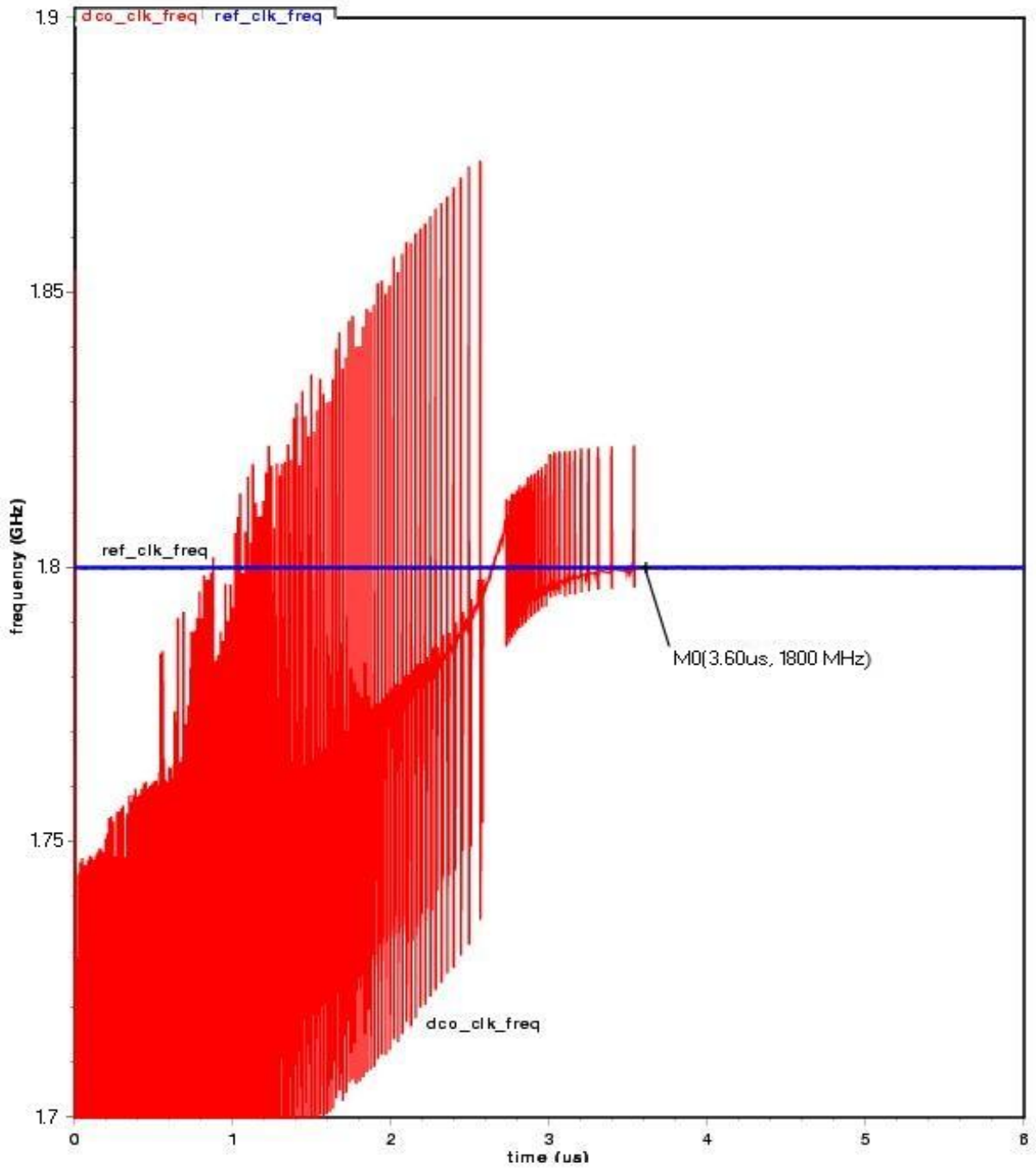

Figure 7.6.DCO output settling time response at band two center frequency

Figure 7.7 shows the minimum average control voltage transient response as per settling time of 3.5us and 0.6V minimum voltage.

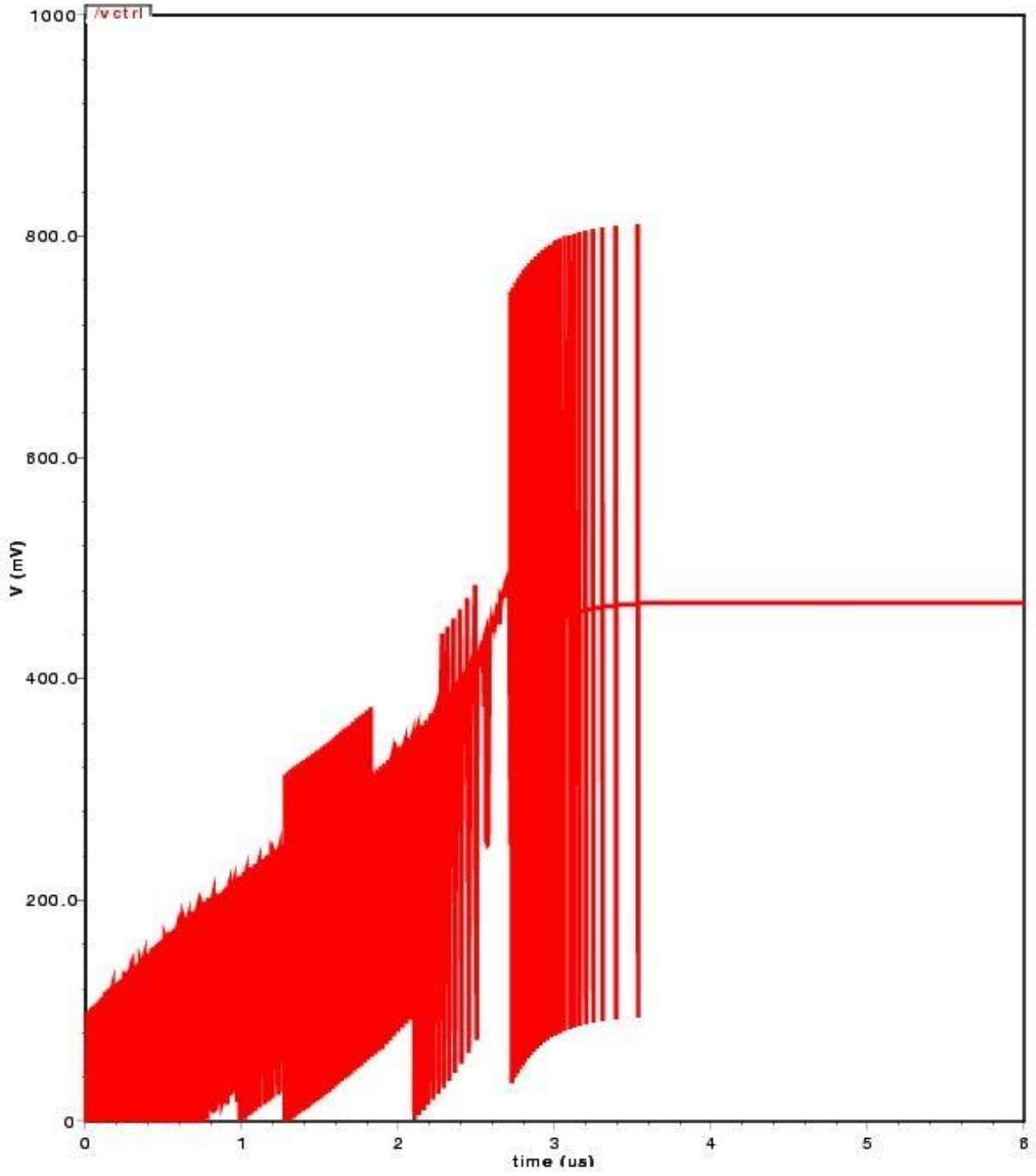

Figure 7.7 Control voltage transient responses

7.2. ADPLL Layout

The layout can be divided into two sections. The controller is completely digital and the layout is done following the digital design flow. The DCO and PFD layouts are done as custom designs. As already mentioned, the PFD part needs balancing of delays between the UP and DOWN path. Also some custom cells are used here and hence custom layout is done.

The controller layout is done using SoC Encounter place and Route from Cadence. The layouts uses standard cell library from Faraday standard cell library. The PFD and DCO are custom laid out using Virtuouso layout Editor from Cadence simulation tool. The controller layout after place and route is saved in graphic data system (gds) format and imported to Virtuouso. The integrated layout is made in Virtuouso simulation software.

Figure 7.8 shows the complete layout. The dimensions are 395um by 300 um which comes to area less than $0.12mm^2$. The design has 20 pins including the power supply and ground. The five digital outputs have output buffers designed from driving 50 ohm, 1 pF load.

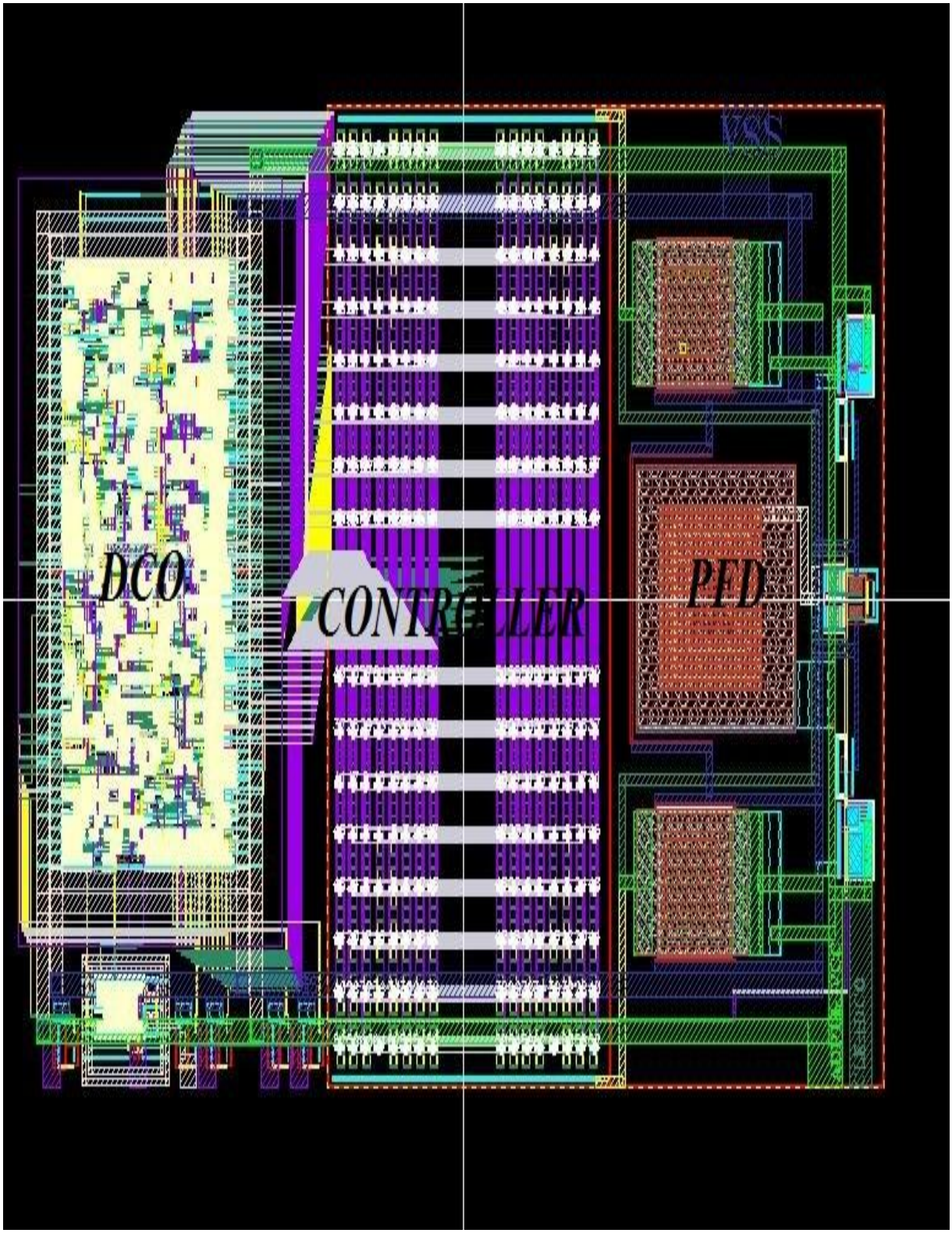

Figure 7.8.ADPLL layout

Chapter 8

Conclusion and Future Work

8.1. Conclusion

All digital phase locked loop, which has been derived as a digital equivalent of the conventional charge pump phase locked loop is introduced in this thesis. The ADPLL architecture used in this thesis is completely different from the conventional ADPLL architectures, which generally requires a high rate clock for sampling. The charge pump phase locked loop has been discretized and the charge pump and loop filter has been replaced with a digital controller in the architecture. The digital controller uses the respective reference input clock as the sampling clock.

By discritizing the conventional charge pump phase locked loop, the new architecture is obtained. After arriving at the new architecture, the loop is analyzed for stability and design equations are derived for critically damped condition. The new architecture driven ADPLL is programmable digital controller and simpler controller architecture. The Phase frequency detector is clocked by the reference clock, which avoids the need to use higher rate clocks. Since the design has minimized analog blocks, the pitfalls of analog part are reduced.

The PLL has been implemented in UMC 130 nm technology, which incorporates parameterized cells. The new architecture blocks are simulated one by one, and the result is promising compared with other related designs. The phase frequency detector is simulated for the output frequency leading or lagging and/or higher or lower the reference frequency for five cases and the result is promising with no dead zone. In addition timing, power and area analysis is done by synthesizing the PFD block VHDL code. The digital controller part synthesis for power, timing and area analysis is done, and promising result is obtained. In a nutshell, all digital phase locked loop has an area less than $0.12mm^2$, consumes 13 mA current, 1.2v supply voltage, 3.55us settling time and 0.5ns locking time, and programmable feed forward gain.

8.2. Limitation

In the UMC 130 nm technology, the minimum PMOS length and width are 120 nm and 169 nm respectively, which give a variable capacitance of 48 aF and frequency resolution of 17 KHz. This requires the control word width to be increased by three more bits. Still the frequency step size becomes 17 KHz, which is the limitation of the current implementation.

Since the capacitor array used is unit weighted rather than the mostly used binary weighted scheme due to variable capacitor library of unified microelectronics corporation technology, it increases the amount of MOSFET capacitors and hence increases area in the wide frequency resolution. This superior approach to analysis also includes an extensive multi-language capability to support design abstraction and the ability to add in RF information.

Today's system-on-chip designs integrate complex analog and digital blocks, requiring thorough testing and analysis of how analog and digital circuits interact and the influence they have on each other. Mixed-signal simulation solutions blend output results from industry-leading block-level and full-chip analog simulators with output from advanced digital analysis technologies. Transistor level power noise analysis and verification solution addressing static and dynamic power integrity needed to be sign-off validation could not be done due to lack of Totem MMX. Moreover off-chip test and full simulation could not be done due to lack of integrated circuit design simulation tools.

Integrated circuit steps include the design architecture fixing, specifying and verifying plan, block level design and simulation, integration, layout, off-chip testing and on-chip testing. But to undergo full off-chip design test like temperature and process variation is difficult due to lack of simulation facilities. In addition, the need to undergo on-chip testing and verification remains to be the future work due to lack of integrated circuit designing company in under developed countries like our country.

8.3. Future work

This work is the initial task of ADPLL integrated circuit design and on chip testing remains to be done as the fabricated chips are not available at present. Further and detailed testing and illustration has to be done and measurements taken to validate the design for further improvement remains future work.

In this thesis attempts to validate the new architecture with the basic design and implementation are done. This is only the initial point for the new architecture and various techniques can be incorporated further to the design to improve the performance and accuracy of the phase locked loop. As shown in the design, the frequency resolution of the phase locked loop is limited by the minimum capacitance available in the UMC technology. To improve the resolution, the capacitance dithering technique can be incorporated to explore the design further. In addition, to achieve better matching varactors, dynamic element matching method is used which forces the architecture to be modified to use these techniques.

Even if the loop filter used in the architecture is second order filter, it is approximated to first order filter. Accompanying the design with higher order filter is another more improvement scheme of the integrated circuit, which requires higher order controllers. In addition, the design can be expanded to a clock distribution network where multiple digitally controlled oscillators are kept in synchronous with each other for band two, and band three, which have been done using analog phase locked loops, and require phase frequency detector that measure phase frequency errors between/among more than two clocks.

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