SURFACE - CHARGE DENSITY

ON THE

SEMICONDUCTOR-INSULATOR INTERFACE

by

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DEDICATED TO

MY FATHER KASSAHUN HAILU

and

MY MOTHER ABEBA ABRAHA

ABSTRACT

The MOS and MNOS diodes, of which an oxidized silicon surface is an integral part, is introduced, and a theory for its operation in the absence of surface states is presented. Real time computer programmes for measurements and numerical analysis were constructed. Measurements of the MOS and MNOS structures were done for different n-type samples, of dry oxide and pyrogenic oxide with different thickness of oxide and nitride. In addition to this irradiated samples by γ-rays with energy 1 MeV were measured.

Different methods of measurements of determining the density and energy distribution of interface states at silicon-silicon dioxide interfaces are described. By using the set of very sensitive electrical measurements the density of interface states were obtained. A comparison of the theoretical capacitance versus voltage curves with measured experimental curves are shown. Computer simulated results of calculations using integration and spline interpolation are given. Obtained experimental results of energy distribution of the interface state density of the order less than 10^{10} states per eV cm^2 are presented and discussed.

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CONTENTS

I. INTRODUCTION

Surface states due to the discontinuity and impurities at an oxidized semiconductor surface with allowed energy levels are possible sources of charge at the semiconductor surface and affect its properties[36].

The study of the semiconductor insulator interfaces has a great practical importance nowadays for physics and device technology. In order to obtain information of the interface states the Metal-Insulator-Semiconductor (MIS) structure was first proposed as a voltage variable capacitor in 1959 by Moll and by Pfann and Garrett[1]. The MIS diode was first employed in a study of thermally oxidized silicon surfaces in 1962 by Terman [36] and in 1963 by Lehovec and Slobodskoy[11]. But in the last decade it has a new importance because of the emergence of the integrated circuits using Metal-Oxide-Semiconductor (MOS) field effect transistors as the active elements and Metal-Nitride-Oxide-Semiconductor (MNOS) structures as a mask against alkali metal contamination and as an oxidation mask. These structures and charge coupled devices are sensitive to the presence of minute traces of charge with surface charge density less than 10^{10} charges/eV cm^2.

The MIS capacitor is used as a simple test structure, in both monitoring integrated circuit fabrication and studying the electrical properties of the device systems. Control of the electrical properties of the MIS system is one of the major factors that has led to stable and high performance silicon integrated circuits. Three regions of the MOS system are important in integrated circuit technology: the bulk oxide, the $Si-SiO_2$ interface, and the silicon itself. Charges in all three regions

play a role in integrated circuits. In the silicon, charges such as dopant impurity ions are necessary for proper device operation. There are two major electrical properties of the $Si-SiO_2$ interface: oxide fixed charge and interface trap level density.

The superiority of the MIS capacitor rests on its structure, fabrication and analysis[45]. Using the MIS capacitor, nearly all of the properties of interest at the $Si-SiO_2$ interface can be measured.

In Chapter II the ideal MIS diode, which is the basis for understanding the non ideal MIS capacitance characterstic is considered and the Poisson equation for potential and charge density at the silicon surface, using the simplifying conditions is solved. In this chapter the ideal MIS curves by deriving expressions for different methods are treated.

Chapter III, deals with practical MIS diode in which interface trapped charges and insulator charges are considered. The major effects found in real MIS capacitor surfaces arise from surface states and different types of oxide charges.

In Chapter IV a description of the most important experimental techniques for measurements follows. Several different ways of investigating and measuring MIS and MNOS structure of semiconductor surfaces and oxide semiconductor interfaces using the set of very sensitive electrical measurements are presented.

Chapter V is devoted to sample preparation and specification of the

MOS and MNOS structures. The various steps of oxidation, including photolithography, gate electrode and deposited silicon nitride are described in this chapter.

In Chapter VI the instruments used are described. The instruments of HP Model LCR multifrequency meter, HP Model PA meter/DC voltage source and HP Model multimeter are directly connected through the bas with the HP-IB computer. In this chapter Block-diagram of measuring apparatus is shown.

Chapter VII deals with the experimental results and discussion of the measurements performed for different samples. Real time computer programme was constructed as shown in Appendices A and B. Using this computer programmes measurements were done and numerical analysis of the experiments were obtained at the same time.

MIS structures prepared by different technological methods were used and the resulting knowledge of the interface state density distribution is to improve the MIS structure technology, to improve fabrication techniques and to make better performing, longer lasting integrated circuits.

II. STUDY OF THE MIS SYSTEM

2.1 MIS Structure

The metal-Insulator-Semiconductor (MIS) structure consists of layers of a parallel plate capacitor with one electrode a metallic plate, called the gate and the other electrode, the silicon. The two electrodes are separated by a thin insulating layer of S_iO_2. Such a structure is shown in Fig.1 where d is the thickness of the insulator and V is the applied voltage on the metal field plate.

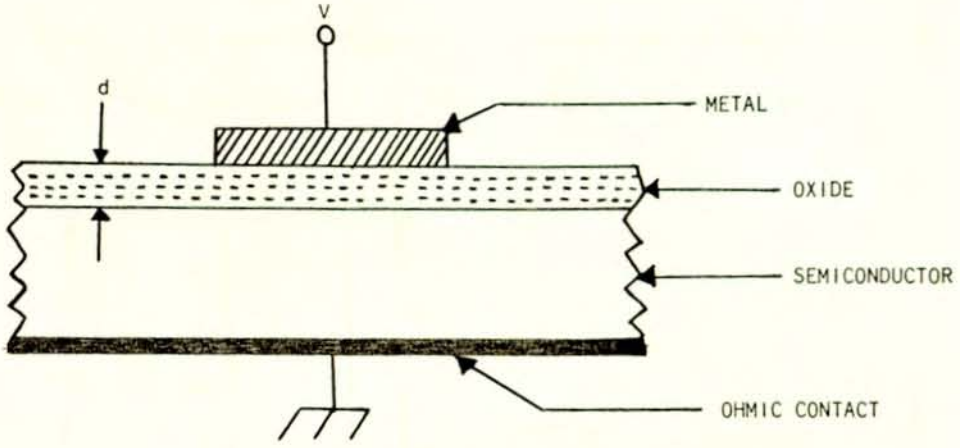

Fig.1. Cross Section of MIS Structure

2.2 Ideal Metal-Insulator-Semiconductor Diode

The energy-band diagram of an ideal MIS diode when V=0, for n-type semiconductor is shown in Fig.2[1]. An ideal MIS diode is defined as follows:

1. At zero applied bias there is no energy difference between the metal work-function and the semiconductor work-function[2], or

$$\phi_{ms} = \phi_m - (x + E_g/2q - \psi_B) = 0 \quad \text{for n-type.} \tag{2.1}$$

Where ϕ_m is the metal work-function; x, the semiconductor electron affinity; x_i, the insulator electron affinity; E_c, the energy of the lower edge of the conduction band; E_g, the band gap; q, the elementary electronic

charge; ϕ_B, the potential barrier between the metal and the insulator; and ψ_B, the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i. In other words, the bands are flat (flat-band condition) when there is no applied voltage.

2. The only chages that can exist in the structure under only biasing conditions are those in the semiconductor and those with equal but opposite sign on the metal surface adjacent to the insulator.

3. There is no carrier transport through the insulator under dc biasing conditions, or the resistivity of the insulator is infinity.

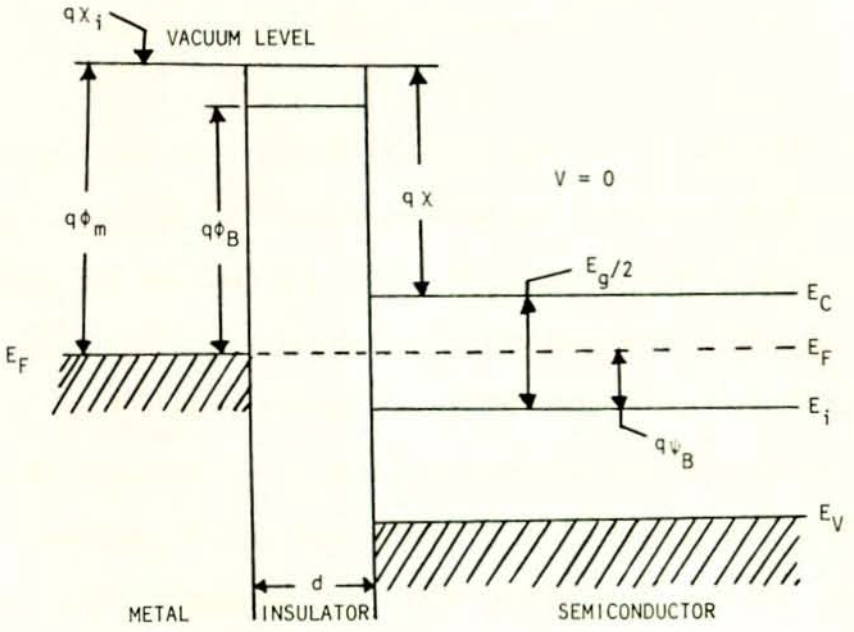

Fig.2. Energy-band diagram for ideal MIS structure at V=0, for n-type semiconductor

The voltage is defined in Fig.1 as that applied to the metal field plate. Thus, V is positive when the metal plate is positive and the semiconductor is negative.

When an ideal MIS diode is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface, as shown in Fig.3.

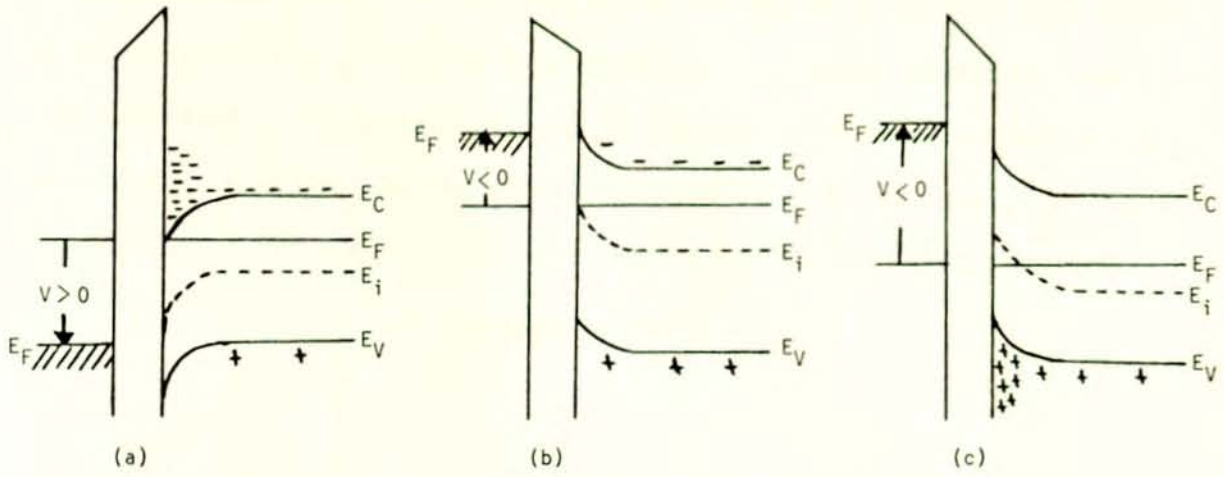

Fig.3 Energy-band diagrams for ideal MIS diodes of n-type semiconductor when $V \neq 0$, for the following cases: a) accumulation; b) depletion; c) inversion.

When a positive voltage (V>0) is applied to the metal plate, the top of the conduction band bends downward and is closer to the Fermi level (Fig.3a). For an ideal MIS diode, no current flows in the structure, so the Fermi level remains constant in the semiconductor. Since the carrier density depends exponentially on the energy difference (E_F-E_C), this band bending causes an accumulation of majority carriers (electrons) near the semiconductor surface. This is the "accumulation" case. When a small negative voltage (V<0) is applied, the bands bend upward, and the majority carriers are depleted (Fig.3b). This is the "depletion" case. When a larger negative is applied, the bands bend even more upward Fig.3c. So that the intrinsic level E_i at the surface crosses over the Fermi level. At this point the number of holes (minority carriers) at the surface is larger than that of the electrons, the surface is thus inverted, and this is the "inversion" case.

2.2.1 Surface Space-Charge Region

Fig.4 shows the band diagram at the surface of an n-type semiconductor. A negative voltage at the field plate causes the bands to be bent upward. The potential ψ is defined as zero in the bulk of the semiconductor and is measured with respect to the intrinsic Fermi level E_i as shown. At the semiconductor surface, $\psi = \psi_s$, and ψ_s is called the surface potential.

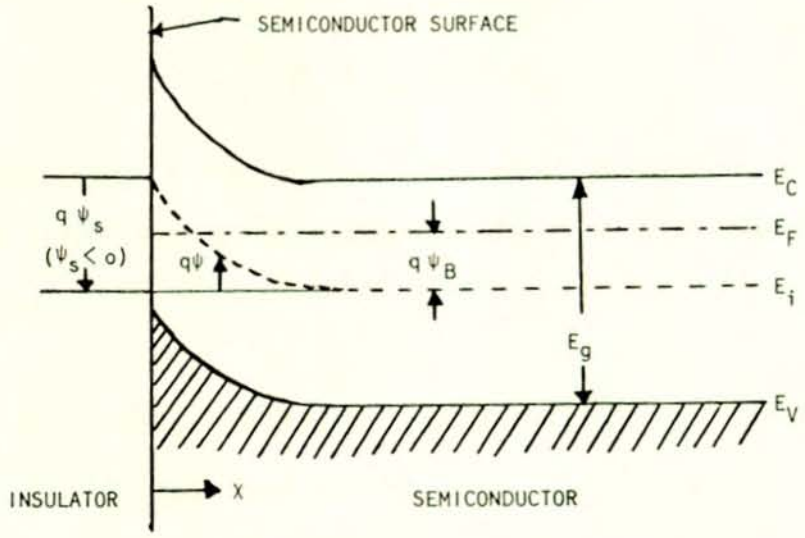

Fig.4 Energy-band diagram at the surface of an n-type semiconductor

The electrostatic potential is defined by

$$q\psi = -E_i \tag{2.2}$$

It is convenient to choose the origin of the potential so that it is zero in the bulk. The bands are flat in the bulk semiconductor with the exception of the surface, where surface fields can cause band bening. The Fermi level, which is the electrochemical potential depends only on the properties of the crystal and remains in its position despite band bending.

The electron and hole concentrations as a function of ψ are given by the following relations:

$$n_n = n_{no} \exp(q\psi/KT) = n_{no} \exp(\beta\psi) \tag{2.3}$$

$$p_n = p_{no} \exp(-q\psi/KT) = p_{no} \exp(-\beta\psi) \tag{2.4}$$

where n_{no} and P_{po} are the equilibrium densities of the electrons and holes in the bulk of the semiconductor; $\beta \equiv q/kT$; k is the Boltzmann's constant; and T, the absolute temperature. ψ is negative when the band is bent upward, as shown in Fig.4.

At the surface of the crystal, the concentrations are:

$$n_s = n_{no} \exp(\beta \psi_s) \tag{2.5}$$

$$P_s = P_{no} \exp(-\beta \psi_s) \tag{2.6}$$

where the subscript s refers to quantities at the surface. With the help of Eq.(2.5) and (2.6), the following regions of surface potential can be distinguished:

$\psi_s > 0$	Enhanced electron concentration-accumulation layer (bands bend upward).
$\psi_s = 0$	Flat-band condition.
$\psi_s < \psi_s < 0$	Depleted electron concentration-depletion layer (bands bend downward).
$\psi_s = \psi_B$	Midgap with $n_s = P_s = n_i$ (intrinsic-concentration).
$\psi_s < \psi_B$	Electron enhancement-Inversion layer, or channel (bands bend downward).

2.3 Solution of the Poisson Equation

2.3.1 Simplifying Conditions

We solve the Poisson equation with certain simplifying conditions. These conditions are:

1. The Poisson equation will be solved in one dimension in the direction perpendicular to the plane of the S_i - S_iO_2 interface. It is reasonable to treat only one dimension because the field under the gate is uniform

and perpendicular to the silicon surface. The fringing field at the gate edge is negligible, affecting an area that extends only an oxide thickness from the periphery of the gate.

2. We assume that the impurity concentration in the silicon is uniform right up to the surface. This assumption does not apply becuase thermal oxidation causes redistribution of the impurity concentration at the silicon surface. However, the case of a uniform impurity distribution is a good introduction.

3. The Poisson equation is solved for the nondegenerate case. In the degenerate case, equilibrium free carrier concentration in the silicon is described by degenerate or Fermi-Dirac statistics. Little useful information about interfacial or oxide properties are gained from MIS capacitor characterstics in the generate bias region. We use the nondegenerate or Boltzmann approximation of the Fermi-Dirac statistics[3].

4. The Poisson equation will be solved using an approximate charge density. The charge of electrons and holes is treated in a self-consistent field approximation. That is, each electron or hole is treated as though it moved in an average field.

5. Surface quantization is neglected. Surface quantization has no bearing on device or MIS capacitor characterstics under conditions of normal use.

2.3.2 Band-Bending Approximation

Figure 4 illustrates the band-bending, or the barrier height ψ_s at the surface of n-type silicon i.e. Band-bending $\psi(x)$ is shown as a function of distance x measured from the S_i - S_iO_2 interface. The band-bending approxi-

mation assumes that the density of states in the conduction and valence band is not changed by an electric field. In the band-bending approximation the only effect of an electric field is to shift all the energy levels in the conduction and valence bands by a constant amount determined by the potential at each given point in the silicon.

Using the band-bending approximation, we calculate the hole density distribution at the silicon surface under an applied bias. Because band-bending is a function of distance, as shown in Fig.4, free carrier concentrations also are functions of distance. The distance x is measured in a direction perpendicular to the interfacial plane into the silicon bulk.

2.3.3 The Poisson Equation

We treat the silicon as a semi-infinite homogeneous crystal in thermal equilibrium. The silicon surface is represented by the plane at $x = o$ and the bulk by positive values of x. This problem is one dimensional, so that potentials are functions of x only.

The Poisson equation will be solved under the simplifying conditions listed in section 2.3.1 above and where the band-bending approximation is valid. Surface potential as a function of x is given by the Poisson equation in one dimension.

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} \tag{2.7}$$

where $\rho(x)$ is the charge density ($coul/cm^3$) composed of immobile ionized donors and acceptors and mobile holes and electrons and $\varepsilon_s = 1.04 \times 10^{-12}$ F/cm is the dielectric permitivity of silicon. $\rho(x)$ is the algebraic sum of all the charge densities in the crystal.

$$\rho(x) = q[P_n - n_n + N_D - N_A] \tag{2.8}$$

where N_D and N_A represent the densities of the ionized donors and acceptors, respectively. Now in the bulk of the semiconductor, far from the surface, charge neutrality must exist. Therefore, $\Psi = 0$ and $\rho(x) = 0$, and we have

$$N_D - N_A = n_{no} - P_{no} \tag{2.9}$$

In general, for any value of Ψ we have from Eqs.(2.3) and (2.4)

$$P_n - n_n = P_{no} \exp(-\beta\Psi) - n_{no} \exp(\beta\Psi) \tag{2.10}$$

substituting (2.8) and (2.9) into (2.7) gives

$$\begin{aligned}\rho(x) &= q[n_{no} - P_{no} + P_{no} \exp(-\beta\Psi) - n_{no} \exp(\beta\Psi)] \\ &= q[P_{no}(\exp(-\beta\Psi)-1) - n_{no}(\exp(\beta\Psi) -1)]\end{aligned} \tag{2.11}$$

The Poisson equation for one dimensional geometry is then

$$\frac{d^2\Psi}{dx^2} = -\frac{q}{\epsilon_s}[P_{no}(\exp(-\beta\Psi)-1) - n_{no}(\exp(\beta\Psi)-1)]. \tag{2.12}$$

Integrating Eq.(2.12) from the bulk toward the surface[4]

$$\int_0^{\partial\Psi/\partial x} \left(\frac{\partial\Psi}{\partial x}\right) d\left(\frac{\partial\Psi}{\partial x}\right) = -\frac{q}{\epsilon_s}\int_0^{\Psi} [P_{no}(\exp(-\beta\Psi)-1) - n_{no}(\exp(\beta\Psi)-1)]d\Psi \tag{2.13}$$

leads to the electric field $E = -d\Psi / dx$:

$$E^2 = \left(\frac{kT}{q}\right)^2 \left(\frac{2 q P_{no} \beta}{\epsilon_s}\right) \left[(\exp(-\beta\Psi) + \beta\Psi - 1) + \frac{n_{no}}{P_{no}}(\exp(\beta\Psi) - \beta\Psi - 1)\right] \tag{2.14}$$

The following abbreviations are introduced:

$$L_D = \sqrt{\frac{kT\ \epsilon_s}{P_{no}\ q^2}} = \sqrt{\frac{\epsilon_s}{q\ P_{no}\ \beta}} \tag{2.15}$$

and

$$F\left(\beta\Psi, \frac{n_{no}}{P_{no}}\right) = \left[(\exp(-\beta\Psi) + \beta\Psi - 1) + \frac{n_{no}}{P_{no}}(\exp(\beta\Psi) - \beta\Psi - 1)\right]^{\frac{1}{2}} \geq 0 \tag{2.16}$$

where L_D is called the extrinsic Debye length for electrons and $F(\beta\psi, \frac{n_{no}}{p_{no}})$ is a dimension less electric field. Thus, the electric field becomes

$$E = -\frac{\partial\psi}{\partial x} = \pm \frac{\sqrt{2}\,kT}{qL_D} F(\beta\psi, \frac{n_{no}}{p_{no}}) \qquad (2.17)$$

The positive sign applies for $\psi < 0$; the negative, for $\psi > 0$.

To determine the electric field at the surface, we let $\psi = \psi_s$:

$$E_s = \pm \frac{\sqrt{2}\,kT}{qL_D} F(\beta\psi_s, \frac{n_{no}}{p_{no}}) \qquad (2.18)$$

Similarly, by Gauss's law the space charge per unit area required to produce this field is

$$Q_s = -\varepsilon_s E_s = \mp \sqrt{2}\,\frac{\varepsilon_s\,kT}{q\,L_D} F(\beta\psi_s, \frac{n_{no}}{p_{no}}) \qquad (2.19)$$

The dc bias at which measurements are made is varied slowly enough so that the charge distribution in the semiconductor can be adequately described by the equilibrium analysis[5,6].

A typical variation of the space-charge desnity Q_s as a function of the surface potential ψ_s is shown in Fig.5 using computer programming for an n-type silicon with $N_D = 10^{15}$ cm^{-3} at room temperature. Note that for positive ψ_s, Q_s is negative and corresponds to the accumulation region. The function F is dominated by the third term in Eq.(2.16), that is, $Q_s \sim -\exp(q|\psi_s|/2kT)$. For $\psi_s = o$, we have the flat-band condition and $Q_s = o$. For $\psi_B < \psi_s < o$, Q_s is positive and we have the depletion case.

The function F is now dominated by the fourth term, that is, $Q_s \sim \sqrt{\Psi_s}$. For $\Psi_s \ll \Psi_B$, we have the inversion case with the function F dominated by the second term, that is $Q_s \sim \exp(q\Psi_s/2kT)$.

Also note that the strong inversion begins at a surface potential

$$\Psi_s(\text{inv}) \simeq 2\Psi_B = \frac{2kT}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{2.20}$$

Two capacitances can be defined for the MIS capacitor in equilibrium C-V curves. The static capacitance which is defined as $C_{stat} \equiv Q_s/\Psi_s$, where Q_s is the total charge density on the capacitor and Ψ_s is the bias applied to it and the differential capacitance which is defined as $C_s \equiv dQ_s/d\Psi_s$. Because charge on an MIS capacitor can vary nonlinearly with voltage, these two capacitances will be different.

The differential capacitance of the semiconductor depletion layer is given by

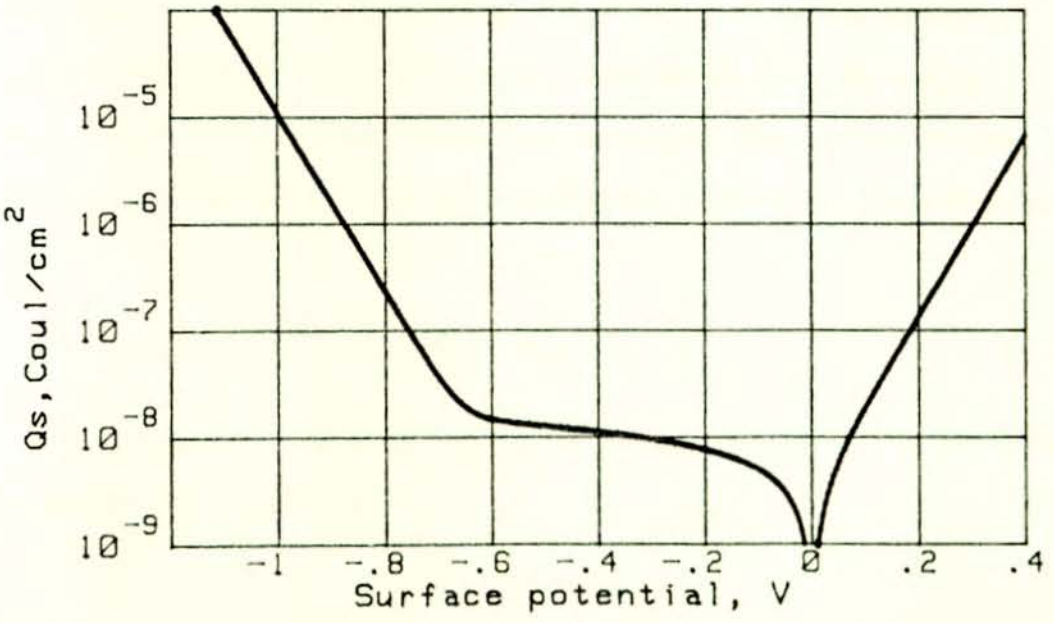

Fig.5 Variation of space-charge density in the semiconductor as a function of the surface potential Ψ_s for n-type silicon with $N_D = 10^{15}\ cm^{-3}$ at room temperature.

$$C_D \equiv \frac{\partial Q_s}{\partial \Psi_s} = \frac{\varepsilon_s}{\sqrt{2} L_D} \frac{[1-\exp(-\beta\Psi_s) + (n_{no}/P_{no})(\exp(\beta\Psi_s) -1)]}{F(\beta\Psi_s, n_{no}/P_{no})} \tag{2.21}$$

At flat-band conditions, that is, $\Psi_s = o$, C_D can be obtained by expanding the exponential terms into series, and we obtain

$$C_D(\text{flat-band}) = \frac{\varepsilon_s}{L_D} \quad F/cm^2 \tag{2.22}$$

2.4 Ideal MIS Curves

2.4.1 Quasistatic and High Frequency Curves

We develop the equivalent circuit representation of the MIS capacitor with no interface traps, oxide charge, or work function difference and derive mathematical expressions for the circuit elements as a function of gate bias. For charge neutrality of the system, it is required that

$$Q_M = Q_n + q N_D W = Q_s \tag{2.23}$$

where Q_M is charges per unit area on the metal, Q_n is the electrons per unit area in the inversion region, $q N_D W$ is the ionized donors per unit area in the space-charge region with space charge width W, and Q_s is the total charge per unit area in the semiconductor. The applied voltage will partly appear across the insulator and partly across the semiconductor. Thus,

$$V_G = V_{ox} + \Psi_s \tag{2.24}$$

We relate the charge per unit area in the silicon Q_s to the field in the oxide, $(V_G - \Psi_s)/d$ by

$$\varepsilon_{ox} E_{ox} = \varepsilon_s E_s \tag{2.25}$$

where ε_{ox} is the dielectric permitivity of S_iO_2 and E_{ox} is the electric field in the S_iO_2. Since there are no charges in the S_iO_2, the field in

the S_iO_2 is constant and equal to

$$E_{ox} = \frac{V_{ox}}{d} = \frac{|Q_s|}{\varepsilon_{ox}} = \frac{|Q_s|}{C_{ox}\, d} \tag{2.26}$$

where V_{ox} is the voltage across the S_iO_2. Using Eq.(2.25) we have

$$C_{ox}(V_G - \Psi_s) = - Q_s \tag{2.27}$$

where $C_{ox} = \varepsilon_{ox}/d$ is the oxide capacitance per unit area; d is oxide thickness; V_G and Ψ_s are the gate voltage and silicon band bending, respectively. The total capacitance per unit area of the MIS capacitor C of the system is a series combination of the oxide capacitance per unit area C_{ox}, and the silicon depletion-layer capacitance C_D:

$$C = \frac{C_{ox}\, C_D}{C_{ox} + C_D} \quad F/cm^2 \tag{2.28}$$

For a given insulator thickness d, the value C_D is constant and corresponds to the maximum capacitance of the system. The capacitance C_D as given by Eq.(2.21) depends on the voltage. Combination of Eqs.(2.21, 2.24, 2.26 and 2.28) gives the complete description of the ideal MIS curve as shown in Fig.6, which is plotted after computer programming was done.

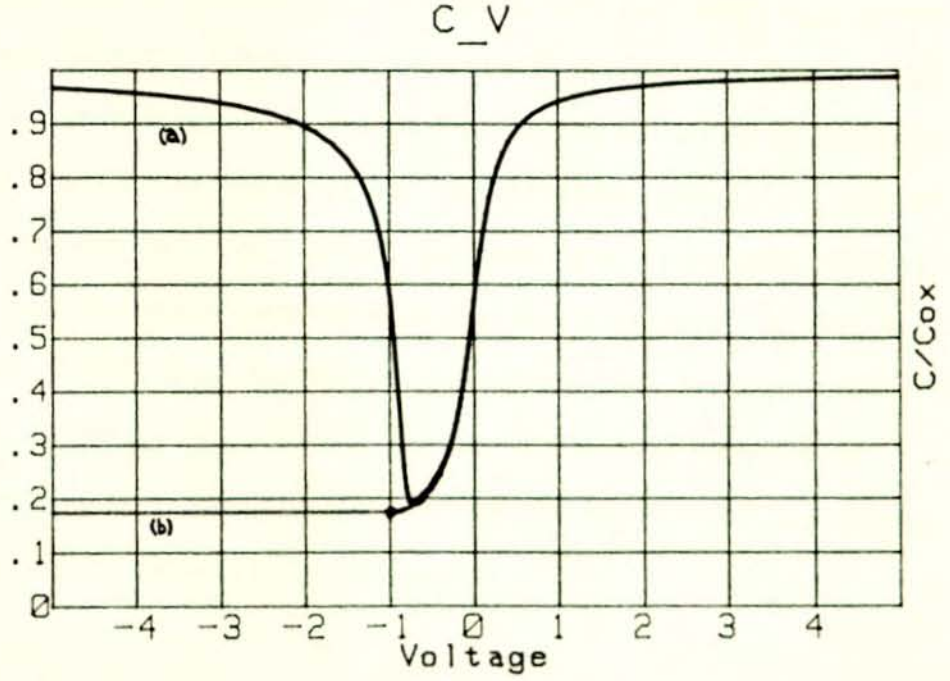

Fig.6 MIS capacitance-voltage curves (a) Law frequency (b) High frequency

Of particular interest is the total capacitance at flat-band condition, that is, $\Psi_s = 0$. From Eqs.(2.22) and (2.28) we obtain

$$C_{FB}(\Psi_s = 0) = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox}/\varepsilon_s) L_D} = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox}/\varepsilon_s)\sqrt{kT\varepsilon_s/P_{no}q^2}} \qquad (2.29)$$

where ε_{ox} and ε_s are the permittivities of the insulator and the semiconductor, respectively, and L_D is the extrinsic Debye length given by Eq.(2.15).

In describing this curve we begin at the right side, positive voltage, where we have an accumulation of electrons and therefore a high differential capacitance of the semiconductor. As a result the total capacitance is close to the insulator capacitance. As the positive voltage is reduced sufficiently, a depletion region which acts as a dielectric in series with the insulator is formed near the semiconductor surface, and the total capacitance decreases. The capacitance goes through a minimum and then increases again as the inversion layer of holes forms at the surface. The minimum capacitance and the corresponding minimum voltage are designated C_{min} and V_{min}, respectively Fig.6. Note that the increase of the capacitance depends on the ability of the holes concentration to follow the applied ac signal. This only happens at low frequencies where the recombination-generation rates of minority carriers (in this case, holes) can keep up with the small-signal variation and lead to charge exchange with the inversion layer in step with the measurement signal. Experimentally, it is found that for the metal - S_iO_2-S_i system the frequency is between 5 and 100 Hz[7]. As a consequence, MIS curves measured at higher frequencies do not show the increase of capacitance on the left side, Fig.6, curve(b).

Figure 6 also shows the corresponding surface potentials. For an ideal MIS diode, the flat-band capacitance occurs at V = 0, where Ψ_s = o. The depletion region corresponds to a surface potential range from Ψ_s = o to $\Psi_s = \Psi_B$.

Weak inversion begins at $\psi_s = \psi_B$, which is slightly greater than V_{min}, and the onset of strong inversion occurs at $\psi_s = 2\psi_B$, as indicated in the figure. The quasi-static curves occurs at $f \leq 100$ Hz.

The high-frequency curve can be obtained using an approach analogous to a one-sided abrupt p-n junction[8]. When the semiconductor surface is depleted, the ionized donors in the depletion region are given by $(-q N_D W)$, where W is the depletion width. For a uniform impurity distribution, $q N_D$ = constant, and the electric field, integrating from the bulk toward the surface is

$$E(x) = \frac{q}{\epsilon_s} N_D \int_w^x dx' \tag{2.30}$$

Integrating (2.30) yields

$$E(x) = \frac{q}{\epsilon_s} N_D (x-w) \tag{2.31}$$

The field at the silicon surface (x=o) will be given by

$$E = -\frac{q}{\epsilon_s} N_D w \tag{2.32}$$

Equation (2.31) and (2.32) show that the field in the silicon depletion layer decreases linearly from E_s at the surface to zero at x = w, the edge of the depletion layer. Integrating (2.31) from the bulk to the surface to obtain the potential in the depletion layer yields

$$\int_o^{\psi(x)} E(x')\, dx' = \frac{q}{\epsilon_s} N_D \int_w^x (x'-w)dx' \tag{2.33}$$

The result of integrating (2.33) is

$$\psi(x) = \frac{q}{2\epsilon_s} N_D (W-X)^2 \tag{2.34}$$

At the surface, x = o, and the surface potential ψ_s from (2.34) becomes

$$\psi_s = \frac{q}{2\epsilon_s} N_D w^2 \tag{2.35}$$

From (2.34) and (2.35), we write

$$\psi(x) = \psi_s\left(1 - \frac{x}{w}\right)^2 \tag{2.36}$$

Equations (2.34) or (2.36) show that band bending in the depletion layer has a parabolic shape as it varies from ψ_s at the surface to zero in the bulk. When the applied voltage increases, ψ_s and w increase. Eventually, strong inversion will occur. As shown in Fig.5, strong inversion begins at $\psi_s(inv) \simeq 2\,\psi_B$. Once strong inversion occurs, the depletion-layer width reaches a maximum. The maximum width W_m of the surface depletion region under steady-state condition can be obtained from Eqs.(2.35) and (2.36):

$$W_m = \sqrt{\frac{2\,\varepsilon_s \psi_s(inv)}{q\,N_D}} = \sqrt{\frac{4\,\varepsilon_s kT\,\ell n(N_D/n_i)}{q^2\,N_D}} \tag{2.37}$$

From equation (2.27), we obtain

$$V_G = -\frac{Q_s}{C_{ox}} + \psi_s \tag{2.38}$$

Equation (2.38) expresses how the applied gate bias divides between the S_iO_2 and the silicon.

To calculate a C-V curve to compare to experiment, (2.21) is calculated as a function of band bending. Then, this result is used to calculate total capacitance as a function of band bending from (2.28). Finally, band bending is related to gate bias using (2.38) to obtain the C-V curve. Surface charge is calculated from (2.19) by substituting (2.16) in (2.19) for n-type. The corresponding total capacitance for high frequency is given by

$$C'_{min} = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox}/\varepsilon_s)W_m} \tag{2.39}$$

For n-type semiconductor the thinner the oxide, the more rapidly capacitance changes with gate bias[9,10].

Alternatively the high frequency capacitance in inversion and its smooth connection with the C-V curve in weak inversion, depletion, and accumulation is calculated. By introducing the small-signal quantities defined by

$$u_{Fn} = u_B + \delta u_{Fn} \tag{2.40.1}$$

and

$$v_s = v_{so} + \delta v_s \tag{2.40.2}$$

Where v_{so} is the total band bending set by the gate bias and δv_s is the ac band bending at x = o, the silicon surface capacitance becomes

$$C_D = \varepsilon_s \frac{\delta}{\delta v_s} \left(\frac{dv}{dx}\right)_{x=o} \tag{2.40.3}$$

Taking the derivative of the dimensionless electric field given by (2.21), the silicon surface capacitance from (2.40.3) becomes (for $v_s > o$)

$$C_D = C_{FB} \left\{1-\exp(-v_s) + \left(\frac{n_i}{N_D}\right)^2 \left[(\exp(v_s)-1)\left(1-\frac{\delta u_{Fn}}{\delta v_s}\right)+1\right] F^{-1}(v_s, u_B)\right\} \tag{2.40.4}$$

Where $C_{FB} = \varepsilon_s L_D^{-1}$ from (2.22). The excess minority carrier charge Q_n is given by

$$Q_n = q n_i \int_o^\infty \left\{\exp[v(x) + u_{FN}] - \exp(u_B)\right\} dx \tag{2.40.5}$$

The excess electron charge set by gate bias alone is also given by

$$Q_n = q n_i \int_o^\infty \left\{\exp[v_o(x) + u_B] - \exp(u_B)\right\} dx \tag{2.40.6}$$

Where $v_o(x)$ is the band bending at x established by the gate bias. The constant on Q_n is obtained by setting (2.40.5) equal to (2.40.6). Thus, we obtain

$$\int_0^\infty \{ \exp[v(x)+u_{Fn}] - \exp(u_B) \}\, dx = \int_0^\infty \{\exp[v_o(x)+u_B] - \exp(u_B)\}\, dx \qquad (2.40.7)$$

Introducing the small-signal quantities from (2.40.1) and (2.40.2) into (2.40.7) and making a small-signal analysis [55,56]

$$\frac{\delta u_{Fn}}{\delta v_s} = \frac{1}{1+\Delta} \qquad (2.40.8)$$

Where Δ is a fraction taking into account the constancy of inversion layer charge and its spatial redistribution. The particular form of (2.40.8) has been chosen deliberately to avoid round-off error in the capacitance when $\delta u_{Fn}/\delta v_s = 1$, which will occur in strong inversion. The expression for Δ is

$$\Delta = \frac{F(v_{so},u_B)}{\exp(v_{so})-1} \{ \int_0^{v_{so}} dv \left[\frac{\exp(v_s) - \exp(-v_s) - 2v_s}{F^3(v_s,u_B)}\right] - 1 \} \qquad (2.40.9)$$

Now we can rewrite (2.40.4) in terms of Δ, to obtain

$$C_D = C_{FB} \{1-\exp(-v_{so}) + \left(\frac{n_i}{N_D}\right)^2 [(\exp(v_{so})-1)\, \frac{\Delta}{1+\Delta} + 1] \} F^{-1}(v_{so},u_B) \qquad (2.40.10)$$

Eq.(2.40.10) is an accurate expression for the high frequency capacitance. To see how Δ affects the high frequency capacitance at different values of v_{so}, (2.40.9) must be evaluated.

2.4.2 Origin of the Equivalent Parallel Conductance

The dominant process causing the measured equivalent parallel conductance is capture and emission of carriers by interface states. Series resistance is not important because it can be made negligible by using epitaxial samples or it can be measured in strong accumulation and subtracted from the total impedance. Noramlly, small-signal measurement are made so that harmonics of the signal frequency arising from the nonlinearity of the charge-voltage characterstics are unimportant.

2.4.3 Admittance of a Single Level State

The purpose is to derive expressions for the admittance of the MIS capacitor as a function of bias and frequency, and to obtain the corresponding equivalent circuits which fit in detail to experimental observations. To describe the MIS conductance technique and interpret the measurements in the depletion and weak inversion regions, we shall rederive the theory for the admittance of the MIS capacitor. The starting point will be the theory for majority carrier capture and emission by a single-level interface state first calculated by Lehovec and Slobodskoy[11].

Experimental evidence shows that only capture and emission of majority carriers are important when measuring in the depletion region. The quasi Fermi level and Fermi level are identical for majority carriers. Thus, application of an ac signal simply results in a time varying Fermi function. From Shockley and Read[12], the capture rate of electrons, taken as majority carriers, by single-level interface state is

$$R_n(t) = N_s C_n[1-f(t)]n_s(t) \tag{2.40}$$

and the emission rate is

$$G_n(t) = N_s e_n f(t) \tag{2.41}$$

Where N_s is the density of states Cm^{-2}; C_n electron capture probability, cm^3/sec, e_n electron emission constant, sec^{-1}, f(t) the Fermi function at time t, and $n_s(t)$ electron density at the silicon surface at time t, cm^{-3}.

Net current density flowing is

$$i_s(t) = q N_s C_n[1-f(t)]n_s(t) - q N_s e_n f(t) \qquad (2.42)$$

where q is electronic charge in Coulombs. Making the small-signal approximation, the admittance is,

$$Y_s = j\omega \frac{q^2}{kT} \frac{N_s f_o (1-f_o)}{(1+j\omega f_o / c_n n_{so})} \qquad (2.43)$$

Where ω is the angular frequency of the ac signal, sec^{-1}, k Boltzman's constant eV x coul/°k, T the absolute temperature, °k, f_o the Fermi function established by the bias, $f_o = [1 + \exp(u-u_s)]^{-1}$, and n_{so} the electron density at the silicon surface established by the bias, cm^{-3}.

Equation (2.43) is the admittance of a series RC network with capacitance $C_s = q^2 N_s f_o(1-f_o)/kT$ and time constant $\tau = f_o / C_n n_{so}$. Separating (2.43)into its real and imaginary parts, the equivalent parallel capacitance is

$$C = \frac{C_s}{1+\omega^2 \tau^2} \qquad (2.44)$$

and the equivalent parallel conductance is

$$G_p = \frac{C_s \omega^2 \tau}{1+\omega^2 \tau^2} \qquad (2.45)$$

Plot of single level state of Eq.(2.45) is shown in Fig.12(a).

2.4.4 Equivalent Circuit of MIS Capacitor

Let Q_T be the total charge density at a given bias. Then

$$Q_T = Q_{sc} + Q_s + Q_f \tag{2.46}$$

Where Q_{sc} is the silicon space-charge density, coul/cm^2, Q_s the interface state charge density, coul/cm^2, and Q_f the fixed-charge density in the oxide, coul/cm^2. The ac current density, $i_T(t)$, obtained by differentiating (2.46) with respect to time is

$$i_T(t) = i_{sc}(t) + i_s(t) \tag{2.47}$$

Where $i_{sc}(t)$ and $i_s(t)$ are the ac current densities charging the silicon space-charge layer and the interface states, respectively. To obtain $i_{sc}(t)$ we have

$$i_{sc}(t) = \left(\frac{dQ_{sc}}{d\Psi_s}\right)\left(\frac{d\Psi_s}{dt}\right) \tag{2.48}$$

Where $\Psi_s(t) = \Psi_{so} + \delta\Psi_s$ is the silicon band bending in volts at time, t; Ψ_{so} the silicon band bending established by the bias, and $\delta\Psi_s = a\exp(j\omega t)$. From this, $d\Psi_s/dt = j\omega\,\delta\Psi_s$. Also, $dQ_{sc}/d\Psi_s = C_D$ the depletion layer capacitance per cm^2. Substituting these into (2.48) we get

$$i_{sc} = j\omega C_D\,\delta\Psi_s \tag{2.49}$$

$i_s(t)$ given by (2.42) can be written

$$i_s(t) = Y_s\,\delta\Psi_s \tag{2.50}$$

Where Y_s is defined by (2.43). Substituting (2.49) and (2.50) into (2.47), we have

$$i_T(t) = (j\omega C_D + Y_s)\delta\Psi_s \tag{2.51}$$

From (2.50), it is seen that C_D appears in parallel with the series RC network of the interface states. The voltage, $v_a + v_o + \delta v_a$, applied to the capacitor devides between the silicon and the oxide film so that

$$v_a(t) = v_o + \delta v_a = \Psi_s(t) + \frac{Q_I}{C_{ox}} \tag{2.52}$$

where v_o is the dc bias, $\delta v_a = b \exp(j\omega t)$, and C_{ox} is the oxide capacitance per cm^2. Differentiating (2.52) with respect to t to get the ac terms only

$$j\omega\delta v_a = j\omega\delta\Psi_s + \frac{i_I(t)}{C_{ox}} \tag{2.53}$$

Substituting for $\delta\Psi_s$ from (2.51)

$$\delta v_a = i_I(t)\ (Z_s + \frac{1}{j\omega C_{ox}}) \tag{2.54}$$

Where

$$Z_s = (j\omega C_D + Y_s)^{-1} \tag{2.55}$$

The bracketed term in (2.54) is the impedance of a circuit in which C_{ox} is in series with Z_s[13]. The equivalent circuit for the MIS capacitor from (2.43), (2.51) and (2.54) is given in Fig.8(a).

III. PRACTICAL MIS DIODE

Of all the MIS diodes, the Metal-$Si O_2$-Si (MIS) diode is by far the most important. An appealing picture of the interface is that the chemical composition of the interfacial region, as a consequence of thermal oxidation, is a single-crystal silicon followed by a monolayer of $Si O_x$, that is, incompletely oxidized silicon, then a strained region of $Si O_2$[14]. For a practical MIS diode, interface traps and oxide charges exist that will, in one way or another, affect the ideal MIS characterstics.

The basic classifications of these traps and charges are shown[15,16] in Fig.7:

1. Interface trapped charges Q_{it}, which are charges located at the Si-$Si O_2$ interface with energy states in the silicon-forbidden bandgap and which can exchange charges with silicon in a short time; Q_{it} can possibly be produced by excess silicon (trivalent-silicon), excess oxygen, and impurities[17,18].

2. Fixed oxide charges Q_f, which are located at or near the interface and are immobile under an applied electric field.

3. Oxide trapped charges Q_{ot}, which can be created, for example, by x-ray radiation or hot-electron injection; these traps are distributed inside the oxide layer.

4. Mobile ionic charges Q_m, such as sodium ions, which are mobile within the oxide under bias-temperature aging conditions.

The effective number of charges per unit area (i.e. C/cm^2) is $N = Q/q$ in number of charges/cm^2. Because interface-trap levels are distributed

accross the silicon energy bandgap, we shall define an interface-trap density N_{it}:

$$N_{it} = \frac{1}{q} \frac{dQ_{it}}{d\psi_s} \quad \text{number of charges/cm}^2 - \text{eV} \tag{3.1}$$

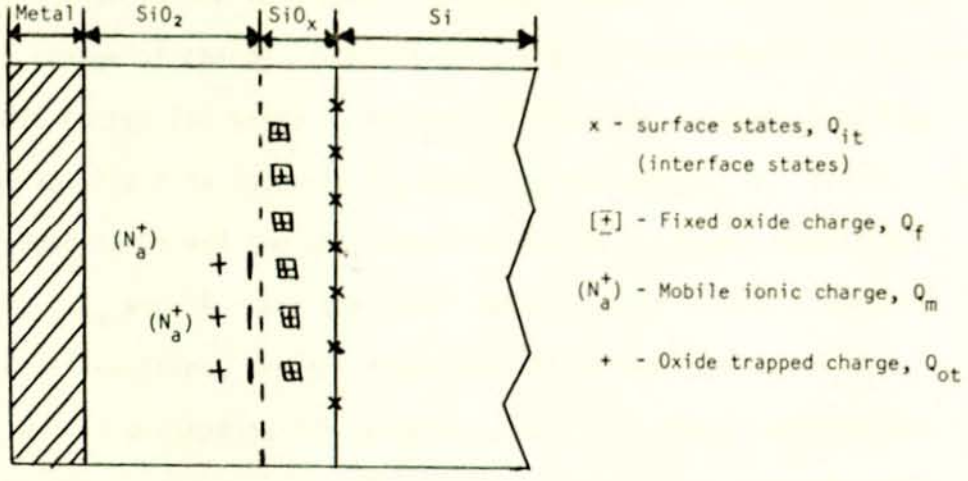

Fig.7 Terminology for charges associated with thermally oxidized silicon in nonideal MIS diode

3.1 Interface Trapped Charge

Interface traps are defects located at the $Si-SiO_2$ interface, each of which has one or more energy levels within the silicon bandgap [19,20,21]. These defects can exchange charge with the silicon specifically, they can interact with the silicon conduction band by capturing or emitting electrons and with the valence band by capturing or emitting holes. Shockley[22], and others[23] have studied the interface-trapped charge Q_{it} (historically called the interface state, fast state, or surface state) and have shown that Q_{it} exists within the forbidden gap due to the interruption of the periodic lattice structure, at the surface of a crystal[24].

An interface trap is considered a donor if it can become neutral or positive by donating (giving up) an electron. An acceptor interface trap

can become neutral or negative by accepting an electron[25,26,27].

When a voltage is applied, the interface-trap levels move up or down with the valence and conduction bands while the Fermi level remains fixed. A change of charge in the interface trap occurs when it crosses the Fermi level. This change of charge contributes to the MIS capacitance and alters the ideal MIS curve. The basic equivalent circuit[28] incorporating the interface-trap effect is shown in Fig.8(a). In the figure, C_{ox} and C_D are the oxide capacitance and the semiconductor depletion-layer capacitance, respectively. C_s and R_s are the capacitance and resistance associated with the interface traps, and are functions of surface potential. The product C_sR_s is defined as the interface-trap life time, which determines the frequency behavior of the interface traps. The parallel branch of the equivalent circuit in Fig.8(a) can be converted into a frequency-dependent capacitance C_p in parallel with a frequency-dependent conductance G_p, as shown in Fig.8(b), where

$$C_p = C_D + \frac{C_s}{1+\omega^2\tau^2} \tag{3.2}$$

and

$$\frac{G_p}{\omega} = \frac{C_s\,\omega\tau}{1+\omega^2\tau^2} \tag{3.3}$$

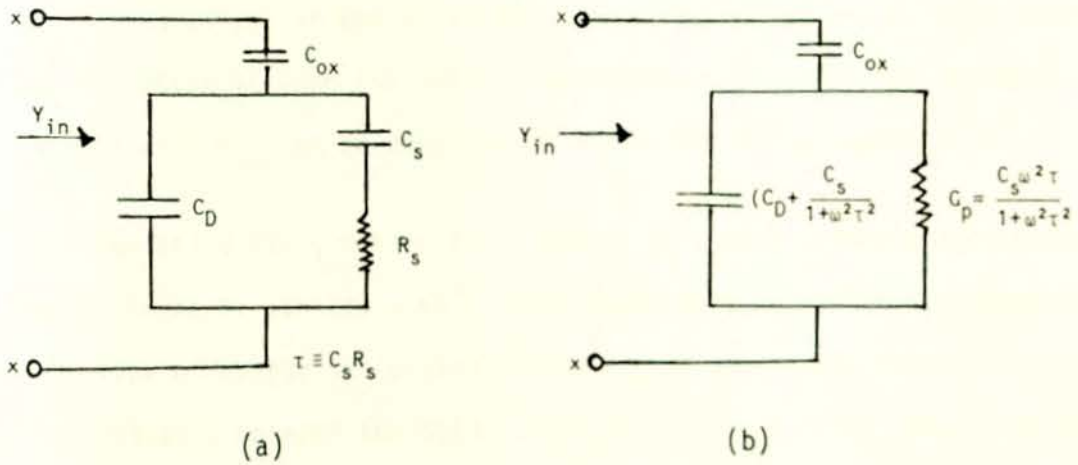

Fig.8 Equivalent circuit including interface-trap effect, where C_s and R_s are associated with interface-trap density.

with $\tau \equiv C_s R_s$. The input admittance Y_{in} is given by

$$Y_{in} = G_{in} + j\omega C_{in} \tag{3.4}$$

where

$$G_{in} = \frac{\omega^2 C_s \tau C_{ox}^2}{(C_{ox} + C_D + C_s)^2 + \omega^2 \tau^2 (C_{ox} + C_D)^2} \tag{3.5}$$

and

$$C_{in} = \frac{C_{ox}}{C_{ox} + C_D + C_s}\left[C_D + C_s \frac{(C_{ox} + C_D + C_s)^2 + \omega^2 \tau^2 C_D (C_{ox} + C_D)}{(C_{ox} + C_D + C_s)^2 + \omega^2 \tau^2 (C_{ox} + C_D)^2}\right] \tag{3.6}$$

3.2 Oxide Charges

There are three types of oxide charges[29,30], that are technologically important. The first type, oxide fixed charge Q_f, is the charge density remaining after interface trap is annealed out. It is fixed and cannot be charged or discharged over a wide variation of ψ_s. Oxide fixed charge is located at or very near the Si-SiO_2 interface. In electrical measurements Q_f can be regarded as a charge sheet located at the Si-SiO_2 interface.

The second type of oxide charge, oxide trapped charge Q_{ot}, usually is located either at the metal-SiO_2 interface or at the Si-SiO_2 interface. One exception is when the oxide traps are introduced by ion implantation. In this case Q_{ot} can be distributed within the oxide layer.

The third type, mobile ionic charge Q_m, most commonly is caused by the presence of ionized alkali metal atoms such as sodium or potassium. This type of charge is located either at the metal-SiO_2 interface, where it originally entered the oxide layer, or at the Si-SiO_2 interface, where it has drifted under an applied field. Drift can occur because such ions are

mobile in SiO_2 at relatively low temperatures.

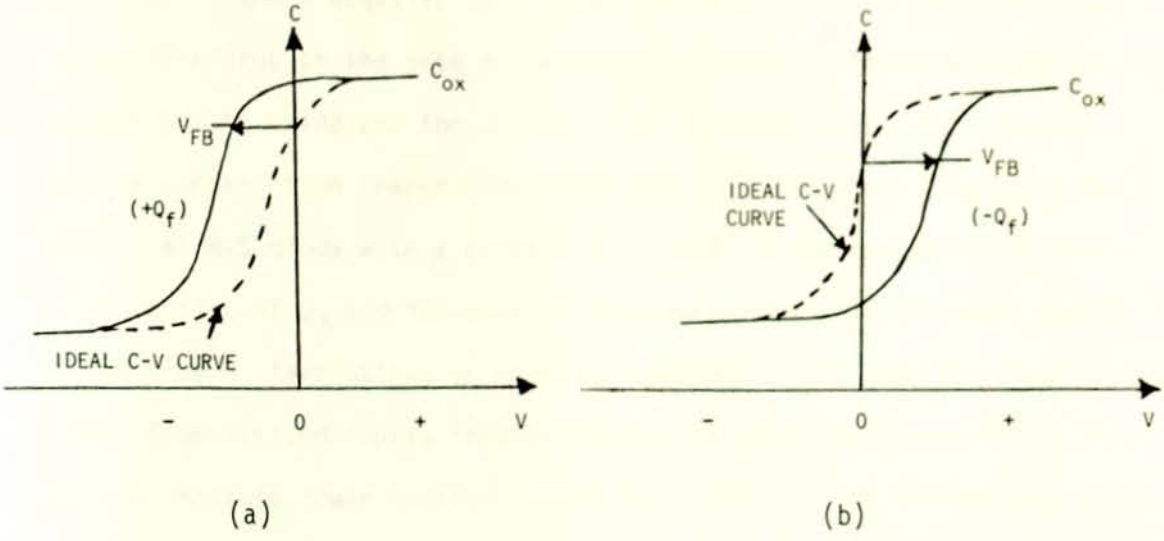

Fig.9 C-V curve shift along the voltage axis due to positive or negative fixed oxide charge for n-type semiconductor

Fig.9 shows the shift along the voltage axis of a high frequency C-V curve when positive or negative Q_f is present at the interface[31]. The voltage shift is measured with respect to an ideal C-V curve where $Q_f = o$. For both n-type and p-type substrates, positive Q_f causes the C-V curve to shift to more negative values of gate bias with respect to the ideal C-V curve, while negative Q_f causes the C-V curve to shift to more positive gate voltage.

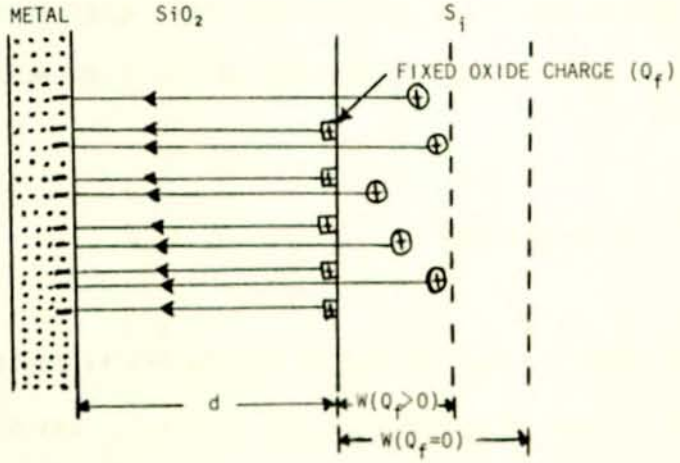

Fig.10 Effect of fixed oxide charge on MIS diode

The votage shift of the C-V curve caused by Q_f can be explained with the help of Fig.10, which shows a cross section through an MIS diode having positive Q_f and a negative gate bias. Charge neutrality requires every negative charge on the gate to be compensated by an equal and opposite charge in the oxide and the silicon. For the ideal case, $Q_f = 0$, the entire compensation charge comes from the ionized donors. However, for a practical MIS diode with a positve Q_f , part of the compensating charge must consist of Q_f and the rest of ionized donors. Fig.10 shows some field lines from Q_f terminating on negative charges on the gate and fewer field lines from ionized donors terminating on the gate than would exist if $Q_f = 0$. Because fewer ionized donors are required, the silicon depletion layer width will be smaller than with $Q_f = 0$ at any given gate bias. Thus, the capacitance will be higher than for the ideal case for all values of gate bias in the depletion and weak inversion regions. The result is a shift of the C-V curve toward more negative gate bias for positive Q_f. For negative Q_f the C-V curve shifts to the opposite direction. The magnitude of the shift is given by

$$\Delta V_f = \frac{Q_f}{C_{ox}} \tag{3.7}$$

There is a large concentration of sodium ions at the Si- SiO_2 interface. This ions cause large flat-band voltage shift and device instability. The flat-band voltage shift due to the mobile ionic charge is given from Gauss's law by

$$\Delta V_m = \frac{Q_m}{C_{ox}} = \frac{1}{C_{ox}}\left[\frac{1}{d}\int_o^d x\,\rho_m(x)dx\right] \tag{3.8}$$

where Q_m is the effective net charge of mobile ions per unit area at the Si- SiO_2 interface and $\rho_m(x)$ is the volume charge density of the mobile ions (i.e., C/cm^3).

Oxide trapped charge also can cause a voltage shift of the MIS C-V curve. These oxide traps are associated with defects in $Si0_2$. The oxide traps are usually electrically neutral, and are charged by introducing electrons and holes into the oxide. The shift due to the oxide trapped charge is given by

$$\Delta V_{ot} = \frac{Q_{ot}}{C_{ox}} = \frac{1}{C_{ox}} \left[\frac{1}{d} \int_0^d x \, \rho_{ot}(x) dx \right] \tag{3.9}$$

where Q_{ot} is the effective net charge in bulk oxide traps per unit area at the Si-SiO_2 interface, and $\rho_{ot}(x)$ is the volume oxide-trap density. The total voltage shift due to all the oxide charges is given by

$$\Delta V = \Delta V_f + \Delta V_m + \Delta V_{ot} = \frac{Q_o}{C_{ox}} \tag{3.10}$$

where $Q_o = (Q_f + Q_m + Q_{ot})$ is the sum of the effective net oxide charge per unit area at the Si- SiO_2 interface.

3.3 MNOS Device

Among several kinds of MIOS (Metal-Insulator-SiO_2 - Si) memory devices, the MNOS (Metal-Si_3N_4- SiO_2-Si) device is the most popular as shown in Fig. 13(c). Other MIOS devices use different insulators to replace the silicon nitride film, such as aluminum oxide, tantalum oxide, and titanium oxide. The MIOS device has been made by using metal ions of Au inplanted into SiO_2 to alter the conduction properties of the outer oxide to form the interfacial charge storage centers[32].

Silicon dioxide, or silica, is the most widely used dielectric in silicon devices at present because this material is readily prepared by

the oxidation of silicon. However, silica is structurally porous, as indicated by its low density, and the use of silica films in devices has some inherent disadvantages. For example, the high permeability of silica toward water vapor and other impurities reduces its effectiveness for passivation, and the migration of alkali ions in thermally grown silica is responsible for the instability of MIS devices. To overcome these disadvantages of silica films, the utilization of silicon nitride films in silicon devices has been explored recently[33].

The two most important applications of silicon nitride in integrated circuit technology are (1) as a mask against alkali metal contamination and (2) as an oxidation mask[34,35]. Used as an oxidation mask, it is possible to have oxide isolation rather than junction isolation resulting in reduced device size similar to the anodic oxide isolation. The oxidation masking feature also allows self-alignment and simplified masking that translate into higher yields and low costs.

IV. SURFACE-STATE MEASUREMENT TECHNIQUES

A number of techniques have been developed to obtain surface-state parameters from MIS capacitors. Among these either the capacitance measurement or the conductance measurement can be used to evaluate the interface-charge density, because in (3.2) and (3.3) both the input conductance and the input capacitance contain similar information about the interface-charge densities. Four techniques for surface-state measurements were used; these are:

1. the high frequency MIS capacitance method
2. the quasi-static MIS capacitance method
3. the combined high-low frequency MIS capacitance method and
4. the MIS conductance method

4.1 High Frequency MIS Capacitance Method

Terman[36] developed and used the high frequency capacitance method for determining interface trap capactance. In the high frequency capacitance method, capacitance is measured as a function of gate bias with frequency fixed at a high enough value so that interface traps do not respond.

"High frequency" meant a frequency high enough to rule out minority carrier response. Generally, minority carriers do not respond to frequencies much above 1KHZ in device grade silicon, whereas interface traps will respond to frequencies upto 100 MHZ. Thus, the term "high frequency" mean a frequency sufficiently high that neither interface traps nor minority carriers follow the ac gate voltage.

The presence of surface states will alter the shape of a capacitance-

voltage curve even if the measurements are made at a frequency high enough that the states do not contribute their charge to the capacitance measurements. At a given bias, surface states lying above the Fermi level in energy will be empty. The empty states represent a density of positive charge at the silicon oxide/silicon interface, and will give rise to an additional field in the oxide. This will result in a larger voltage drop across the oxide than would be experienced if no states were present[37]. The capacitance-voltage curve will consequently be shifted horizontally by the amount of the increased drop in the oxide[38].

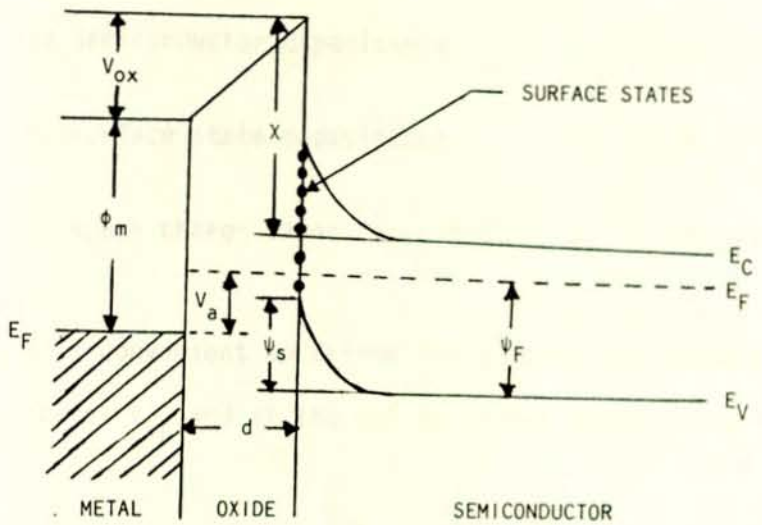

Fig.11 Band picture for MOS capacitor of n-type.

From Fig.11 it follows that

$$V_a - [\phi_m - (x - \psi_B)] \equiv V = V_{ox} + \psi_s \qquad (4.1)$$

where V is the effective applied gate voltage and the contact potential between metal and semiconductor is zero so that $V = V_a$[39].

When a voltage V is applied to the MOS structure, the net semiconductor charge Q_{tot} is distributed between a charge Q_{ss} in surface states and a charge Q_{sc} in the semiconductor space charge layer. Thus,

$$Q_{tot} = Q_{ss} + Q_{sc} \tag{4.2}$$

As the applied voltage (and with it V_{ox} & ψ_s) changes, these charges will change so that we define the following capacitances:

The MOS capacitance $$C \equiv dQ_{tot}/dV \tag{4.3}$$

The oxide capacitance $$C_{ox} \equiv dQ_{tot}/dV_{ox} \tag{4.4}$$

The semiconductor capacitance $$C_s = dQ_{tot}/d\psi_s \tag{4.5}$$

The surface state capacitance $$C_{ss} = dQ_{tot}/d\psi_s \tag{4.6}$$

The space charge layer capacitance $$C_{sc} = dQ_{sc}/d\psi_s \tag{4.7}$$

It is also convenient to define the voltage equivalents of the charge in surface states V_{ss} and of the charge in the space charge layer V_{sc} as

$$V_{ss} \equiv Q_{ss}/C_{ox} \tag{4.8}$$

and

$$V_{sc} \equiv Q_{sc}/C_{ox} \tag{4.9}$$

Since we have assumed that the charge Q_{ss} has a negligible effect on the uniformity of the field in the oxide, it follows from Gauss' law that

$$Q_{tot} = \varepsilon_{ox} E_{ox} = \varepsilon_{ox}(V_{ox}/d) = C_{ox} V_{ox} \tag{4.10}$$

From (4.2, 4.5, 4.6 and 4.7) it can be shown that

$$C_s = C_{ss} + C_{sc} \tag{4.11}$$

is a parallel combination of the surface state and space charge layer capacitance. In addition, from (4.2) through (4.5) it can be shown that

$$C = \frac{C_{ox} C_s}{C_{ox} + C_s} \tag{4.12}$$

is a series combinations of oxide and semiconductor capacitance.

As is discussed in detail in Terman[36], Lehovec, et al.[11] and Heiman and Warfield[40], one can determine an effective surface state density N_{ss} from measurements of the high-frequency MOS capacitance as a function of bias. Because of the pecularities in the high-frequency response of an inversion layer, we will restrict to accumulation and depletion layers. For convenience, we summarize here the procedure for carrying out this type of experiment.

1. Determine experimentally the high-frequency capacitnace as a function of bias.
2. Calculate $dV_{sc}/d\psi_s$ for each bias
3. Determine ψ_s corresponding to this particular bias[40].
4. This value of surface potential can now be used to calculate the voltage equivalent V_{sc} of the charge stored in the semiconductor space charge layer.
5. Now that V, ψ_s, and V_{sc} are knwon, V_{sc} can be calculated from the relation

$$V = V_{ox} + \psi_s = V_{ss} + V_{sc} + \psi_s \tag{4.13}$$

which is a consequence of (4.2, 4.8, 4.9 and 4.10).

6. Plot V_{ss} as a function of ψ_s

7. From (4.8) it can be seen that the slope of this curve is

$$\frac{dV_{ss}}{d\psi_s} = \frac{1}{C_{ox}} \left(\frac{dQ_{ss}}{d\psi_s}\right) = \frac{e}{C_{ox}}\left(\frac{dN_{ss}}{d\psi_s}\right) = \frac{e}{C_{ox}} \mathbf{N}_{ss} \qquad (4.14)$$

where N_{ss} is the total number of occupied trap states and $\mathbf{N}_{ss}$ is the effective occupied surface state concentration in units of $(cm^2\ V)^{-1}$.

4.2 Quasi-Static MIS Capacitance Method

Berglund[41] developed and was first to use the quasi-static frequency C-V method. C-V curve is measured at a frequency so low that interface trap response is immediate.

"Quasi-static frequency" meant a frequency low enough for immediate minority carrier response. Generally, it requires a lower frequency to elicit immediate minority carrier response than to elicit immediate interface trap response. Thus, the term "quasi-static frequency" mean a frequency low enough for immediate minority carrier and interface trap response. Measurements at low frequencies, where the period of the measurement signal is long compared to the time constants of the surface states, will be utilized to determine the energy distribution of the surface states[42].

Fig.11 shows the voltage and charge relationships in an MOS capacitor. At equilibrium, the relation between appleid voltage across the MOS structure and band bending in the silicon neglecting space charge in the oxide is

$$\frac{\varepsilon_{ox}(V_{ox}+V_c)}{d} = q\int_0^{\infty} N_{SD}^{+}(E)[1-f(E,\psi_s)]dE$$

$$- q\int_0^{\infty} N_{SA}^{-}(E)f(E,\psi_s)dE + Q_D(\psi_s) \qquad (4.15)$$

where V_c is a constant voltage which accounts for the zero bias band bending. This voltage includes the effect of fixed charge in the oxide, net charge in the surface states at zero bias, and differences in work functions; $N_{SD}^{+}(E)$, the density of surface states of energy E which are positively charged when ionized; $N_{SA}^{-}(E)$, the density of surface states of energy E which are negatively charged when occupied; $f(E,\psi_s)$, the Fermi distribution function; and $Q_D(\psi_s)$, the net charge per square centimeter in the silicon.

The charge in the silicon has been calculated by several authors as a function of band bending, temperature, and bulk doping density[6,43,44]. If (4.15) is differentiated with respect to ψ_s, the result can be solved for $d\psi_s/d\,V_{ox}$ to give

$$\frac{d\psi_s}{dV_{ox}} = \frac{\varepsilon_{ox}}{d}/\left[\frac{dQ_D(\psi_s)}{d\psi_s} + qN_{ss}(\psi_s)\right] \qquad (4.16)$$

where

$$N_{ss}(\psi_s) = N_{SD}^{+}(\psi_s) + N_{SA}^{-}(\psi_s) \qquad (4.17)$$

is the total surface-state density per unit area located at an energy $q\psi_s$, provided that the surface-state density does not vary significantly over several kT/q of surface potential about ψ_s.

Refering to Fig.11 an MOS structure can be represented by an oxide capacitance in series with a network which takes into account the silicon

space charge region and the surface states. The small-signal capacitance C of the device at an applied dc voltage V_a is

$$C(V_a) = dq/dV_a \tag{4.18}$$

But

$$dq = C_{ox}\, dV_{ox} \tag{4.19}$$

so

$$C(V_a) = C_{ox}\, dV_{ox}/dV_a \tag{4.20}$$

since

$$dV_a = dV_{ox} + d\psi_s(V_a) \tag{4.21}$$

then[40]
$$C(V_a) = C_{ox}\left[1 - \frac{d\psi_s(V_a)}{dV_a}\right] \tag{4.22}$$

Hence
$$d\psi_s/dV_a = 1 - C(V_a)/C_{ox} \tag{4.23}$$

Integrating (4.23), the charge in surface potential due to a change in applied MOS voltage from V_1 to V_2 is

$$\psi_s(V_1) - \psi_s(V_2) = \int_{V_1}^{V_2} [1 - C(V_a)/C_{ox}]\, dV_a \tag{4.24}$$

Using (4.21) and (4.22), it can also be shown that

$$d\psi_s/dV_{ox} = C_{ox}/C(V_a) - 1 \tag{4.25}$$

The values of $d\psi_s/dV_{ox}$ obtained from (4.25) are given by (4.16) under the condition that the surface states are in equilibrium at all times during the measurement. Hence, if $dQ_d(\psi_s)/d\psi_s$ is known, an experimental curve of $d\psi_s/dV_{ox}$ Vs. ψ_s, obtained from low-frequency MOS capacitnace measurements and (4.24) and (4.25), can be compared to that given by (4.16) to determine directly the surface-state density.

4.3 Combined High-Low Frequency MIS Capacitance Method

Combined High-Low Frequency MIS capacitance method is a combination of both the high frequency and low frequency MIS capacitance methods. This method is used to obtain a measured C_D which eliminates the need for a theoretical computation of C_D and for measurement of the doping profile of the device. At high frequencies the interface traps capacitance $C_{it} = 0$, because frequency is too large for any ac response of interface traps. The capacitance at high frequencies C_{HF} is given by

$$C_{HF} = \frac{C_D\, C_{ox}}{C_D + C_{ox}} \tag{4.3.1}$$

Therefore, regardless of interface trap level density, the high frequency capacitance of an MOS capacitor is the same as that of an ideal one without interface traps, provided that C_D is the same. Using Eq.(4.3.1), we have

$$C_D = \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \tag{4.3.2}$$

The low frequency capacitance of the MOS capacitor is

$$C_{LF} = (C_D + C_{it})\ \frac{C_{ox}}{C_{ox} + C_D + C_{it}} \tag{4.3.3}$$

Eq.(4.3.2) shows that C_{it} can be extracted from the measured low frequency capacitance if C_D and C_{ox} are known. The relation between this capacitances in Eq.(4.3.2) can be rewritten as

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_D + C_{it}} \tag{4.3.4}$$

Where C_{LF} is the low frequency capacitance measured at gate bias V_G . Solving (4.3.3) for C_{it} yields

$$C_{it} = [\frac{1}{C_{LF}} - \frac{1}{C_{ox}}]^{-1} - C_s \qquad (4.3.5)$$

Where C_{ox} can be measured in strong accumulation. Substituting Eq.(4.3.2) into (4.3.5) yields

$$C_{it}=(\frac{1}{C_{LF}} - \frac{1}{C_{ox}})^{-1} - (\frac{1}{C_{HF}} - \frac{1}{C_{ox}})^{-1} \qquad (4.3.6)$$

In this way C_{it} is obtained directly from the measured C-V curves, without the uncertainty introduced by a theoretical C_D and without uncertainty as to whether C_D has been calculated for the correct band bending. The low frequency capacitance C_{LF} is eliminated from (4.3.6) by the relation

$$C_{LF} = \Delta C + C_{HF} \qquad (4.3.7)$$

Where $\Delta C = C_{LF} - C_{HF}$. Substituting (4.3.7) into (4.3.6) yields

$$N_{it} = \frac{C_{ox}}{q}[(\frac{1}{\Delta C/C_{ox} + C_{HF}/C_{ox}} - 1)^{-1} - (\frac{1}{C_{HF}/C_{ox}} - 1)^{-1}] \qquad (4.3.8)$$

$$= \frac{\Delta C}{q}(1 - \frac{C_{HF} + \Delta C}{C_{ox}})^{-1}(1 - \frac{C_{HF}}{C_{ox}})^{-1} \qquad (4.3.9)$$

Where C_{it} is related to N_{it} by

$$C_{it} = q N_{it} \qquad (4.3.10)$$

and N_{it} is the interface trap level density.

4.4 MIS Conductance Method

The principle of the MIS conductance technique is easily illustrated by equivalent circuit of Fig.8(a). The admittance of the capacitor is measured in the region of strong accumulation. The admittance of the network is then converted into an impedance. The reactance of the oxide capacitance is subtracted from this impedance and the resulting impedance converted back into an admittance. This leaves C_D in parallel with the series Rc Network of the interface states. The capacitance from (2.44) and (2.51) is

$$C_p = C_D + \frac{C_s}{1 + \omega^2 \tau^2} \tag{4.26}$$

and the equivalent parallel conductance divided by ω from (2.45) is

$$\frac{G_p}{\omega} = \frac{C_s \omega \tau}{1 + \omega^2 \tau^2} \tag{4.27}$$

G_p is divided by ω to make (4.27) symmetrical in $\omega\tau$. Equation (4.26) describes the capacitance dispersion and is the basis of Terman's method. To extract C_s and τ from C_p using (4.26), C_D must be known. C_D can be calculated[43] using an estimated doping density. The doping density is not accurately known near the silicon surface because of pile up or depletion of the dopant during oxidation. Equation (4.27) on the other hand depends only on the interface state branch of the equivalent circuit. G_p/ω goes through a maximum when $\omega\tau = 1$ which gives τ directly. The value of G_p/ω at the maximum is $C_s/2$. Thus, equivalent parallel conductance corrected for C_{ox} gives C_s and τ directly from the measured conductance. The surface-state density is obtained by using the relation

$$N_{ss} = C_s/qA \tag{4.28}$$

where A is the metal plate area and C_s is the capacitance of the surface state.

4.4.1 Admittance of an Interface State Continuum

The interface states are observed to be comprised of many levels so closely spaced in energy that they cannot be distinguished as separate levels. Thus, they appear as a continuum over the bandgap of the silicon. A continuum of interface states appears to be characteristic of the $Si-SiO_2$ interface.

For a continuum of states at a finite absolute temperature, capture and emission of majority carriers can occur by states located within a few KT/q on either side of the Fermi level. This results in a time constant dispersion. The admittance of the continuum is obtained by integrating (2.43) over the bandgap.

$$Y_{ss} = j\omega\left(\frac{q^2}{KT}\right) \int \frac{N_{ss} f_o (1-f_o) d\psi}{(1+j\omega f_o / C_n n_{so})} . \tag{4.29}$$

Here N_{ss} is the density of interface states, $cm^{-2}eV^{-1}$, and ψ is energy in eV. The integrand of (4.29) is sharply peaked about the Fermi level with a width of about KT/q. Thus, (4.29) can be easily integrated if both N_{ss} and C_n the capture probability do not vary very much with ψ over a range KT/q. Making the substitution $f_o(1-f_o) = (KT/q)(df_o/d\psi)$ transforms (4.29) into an integral over f_o. Integrating from zero to unity yields.

$$Y_{ss} = \frac{qN_{ss}}{2\tau_m} \ln(1+\omega^2\tau_m^2) + j\, q\, \frac{N_{ss}}{\tau_m} \arctan(\omega\tau_m) \tag{4.30}$$

where

$$\tau_m = 1/c_n n_{so} \tag{4.31}$$

Concentrating on the real part of (4.30), we have for the continuum

$$\frac{G_p}{\omega} = \frac{qN_{ss}}{2\omega\tau_m} \ln(1+\omega^2\tau_m^2). \tag{4.32}$$

The plot of interface state continuum of eq.(4.32) is shown in Fig.12(b).

4.4.2 Extraction of G_p/ω

It is necessary first to get G_p/ω and C_p from the measurements. C_p and G_p are shown in Fig.8(b) to be the capacitance and equivalent parallel conductance of the portion of the equivalent circuit consisting of C_D in parallel with the distributed network representing the interface states. The admittance measured across the terminals x-x in Fig.8(a) is

$$Y_s = G_m + j\omega C_m \tag{4.33}$$

Converting (4.33) to an impedance, we get

$$Z_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} - j \frac{\omega C_m}{G_m^2 + \omega^2 C_m^2} \tag{4.34}$$

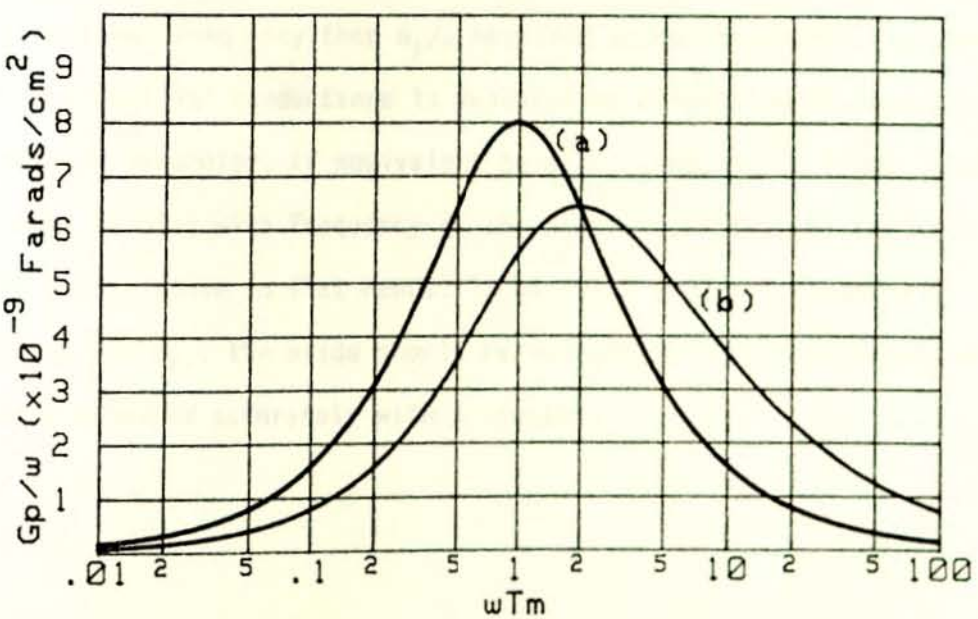

Fig.12 Calculated G_p/ω Vs. log $\omega\tau_m$. (a) Plot of single level state and (b) Plot of interface state continuum.

Subtracting away the reactance, $X_c = 1/j\omega C_{ox}$, of C_{ox} from (4.34) we get,

$$Z_s - X_c = \frac{\omega C_{ox} G_m}{\omega C_{ox}(G_m^2+\omega^2 C_m^2)} + j\frac{(G_m^2+\omega^2 C_m^2-\omega^2 C_{ox} C_m)}{\omega C_{ox}(G_m^2+\omega^2 C_m^2)} \tag{4.35}$$

and converting back (4.35) to an admittance, we get

$$Y_p = \frac{\omega^2 C_{ox}^2 G_m(G_m^2+\omega^2 C_m^2) + j\omega C_{ox}(G_m^2+\omega^2 C_m^2)[\omega^2 C_m(C_{ox}-C_m)-G_m^2]}{\omega^2 C_{ox}^2 G_m^2 + [\omega^2 C_m(C_{ox}-C_m)-G_m^2]^2} \tag{4.36}$$

where

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m(G_m^2+\omega^2 C_m^2)}{\omega^2 C_{ox}^2 G_m^2 + [\omega^2 C_m(C_{ox}-C_m) - G_m^2]^2} \tag{4.37}$$

and

$$C_p = \frac{C_{ox}(G_m^2+\omega^2 C_m^2)[\omega^2 C_m(C_{ox}- C_m) - G_m^2]}{\omega^2 C_{ox}^2 G_m^2 + [\omega^2 C_m(C_{ox}-C_m)-G_m^2]^2} \tag{4.38}$$

It should be noted that the circuit across the terminals x-x in Fig.8(a) has a shorter time constant than that of just the interface state branch of the circuit becuase of C_{ox}. Therefore, G_p/ω from (4.37) will peak at a lower frequency than G_p/ω measured across termianls x-x when equivalent parallel conductance is measured as a function of frequency with bias as parameter. If equivalent parallel conductance is measured as a function of bias with frequency as parameter, G_p/ω from (4.37) will peak at a bias close to flat bands. To minimize errors introduced by correcting for C_{ox}, the oxide should be made as thin as practicable and frequency measured accurately with a counter.

V. SAMPLE PREPARATION

MOS and MNOS samples including the holder of the sample were brought from St. Petersberg, Technical University. All these MOS and MNOS structure samples as shown in Table 1 are n-type, of not irradiated and irradiated by γ-rays with energy 1MeV, and dry oxide and pyrogenic oxide with different thicknesses of oxide and nitride.

The samples as shown in Fig.13(a) are phosphorus doped of donor concentration $N_D = 10^{15}$ cm^{-3}, having resistivity of $\rho = 4.5$ Ohm-cm oriented in the [100] direction with surface area of $A = 4 \times 10^{-2}$ cm^2.

No.	Sample	Structure	Type of 'O'	Radiation	Thickness 'Å'
1	N8D-6	MOS	Dry	Not-Irradiated	670
2	N8P-18	"	Pyrogenic	"	620
3	N8NP-19	MNOS	"	"	600/800
4	N7D-9	MOS	Dry	"	690
5	N7NP-10	MNOS	"	"	750/810
6	γ5-8	MOS	"	"	625
7	N4D-13	"	"	"	400
8	N8NP-8	MNOS	"	Irradiated(10^7rad)	660/850
9	N8NP-12	"	Pyrogenic	"	600/800
10	γ7-14	"	Dry	Not-Irradiated	1000/800

Table 1. Sample specification of MOS and MNOS structures

The MOS capacitor consists of a silicon substrate, an ohmic back contact to the silicon substrate, a thin oxide layer, and a metal gate electrode. Such an array of MOS capacitors on a silicon wafer is shown in Fig.13(b).

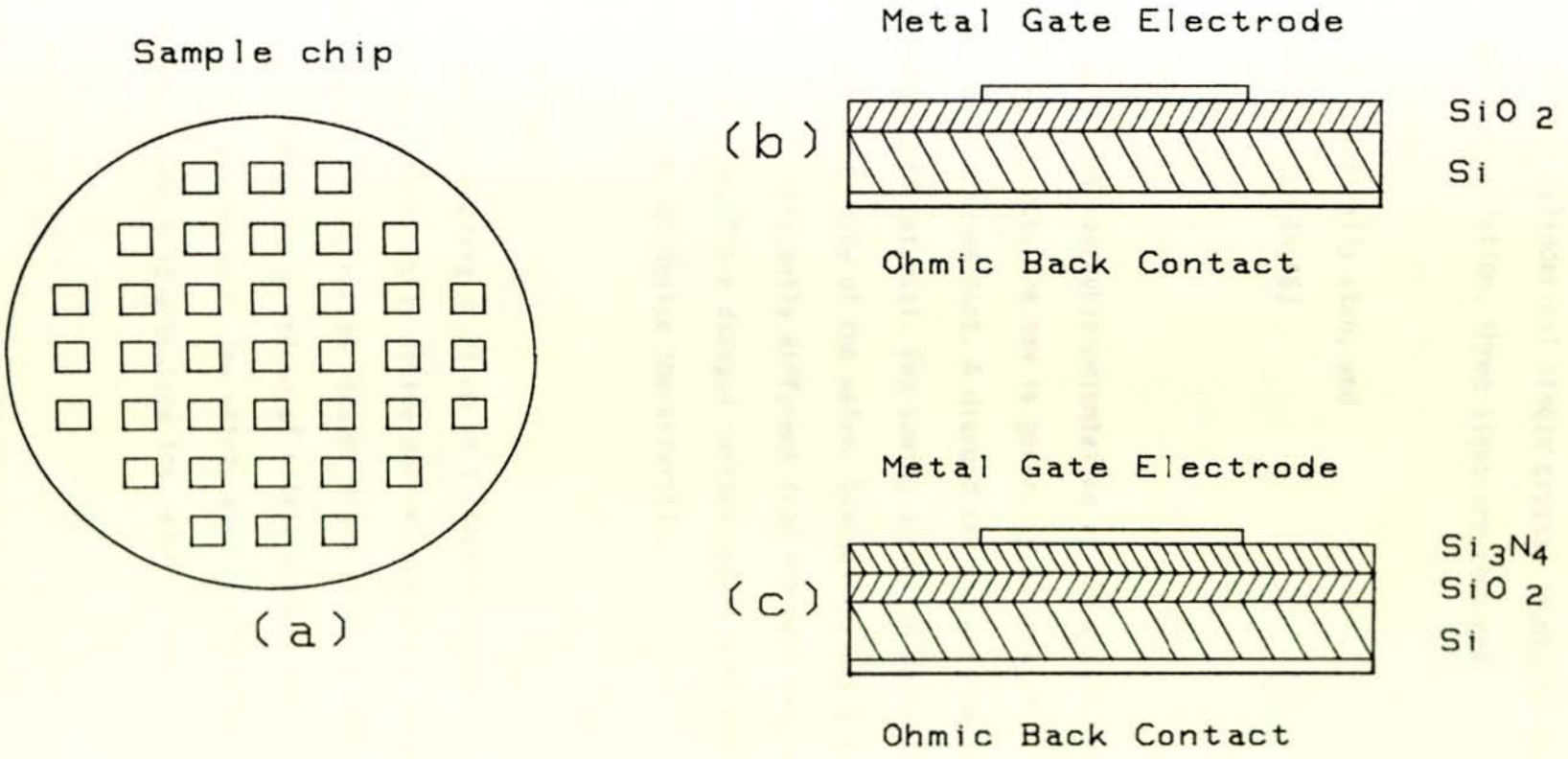

Fig.13 Typical MOS Capacitor Array on a Wafer

The silicon crystal for electron device application was pulled into the form of a cylinderical single crystal ingot. To prepare wafers from an ingot for oxidation, three steps are required:

1) saw,
2) chemically etch, and
3) polish[45,46]

5.1 Sawing

The crystallographic orientation of the wafers was determined during the sawing process. The saw is generally a circular disk with an edge charged with diamond dust. A diamond saw was used because silicon is a relatively hard material. The sawing operation mechanically damages the surface on each side of the wafer. Damaged surface layers have electrical properties significantly different from the bulk properties of single-crystal silicon. These damaged surface layers were removed to eliminate adverse effects on device characterstics.

5.2 Etching

Chemical etching of 25 μm of silicon from each side of the wafer removed the electrically active damage completely and neither leaved the wafers nonflat nor caused feather edges prone to chipping. The etchant consists of 4 parts by volume of nitric acid, 1 part hydrofluoric acid, and 3 parts acetic acid. The nitric acid oxidized the silicon surface and the hydrofluoric acid dissolved the oxide formed.

5.3 Polishing

The polishing operation is the last and most critical step. It leave one surface of the wafer flat, specular, and undamaged. Polishing was done

by rubbing the wafer against a cloth saturated with an abrasive material such as syton. Syton is powdered SiO_2, which was used because it is not foreign to the Si-SiO_2 system. After polishing, an oxide was grown to protect the silicon surface during storage.

5.4 Preoxidation Cleaning

After polishing residues were cleaned off and the wafers were ready for the preoxidation cleaning step. The preoxidation cleaning step must be regarded as part of the oxidation process, as the wafers should be placed in the oxidation furnace immediately after preoxidation cleaning. The purpose of preoxidation cleaning was to remove both organic and inorganic contaminants that the wafers have picked up during handling and storage. If not removed, such contaminants can cause poor performance and stability of the devices subsequently made.

5.5 The Oxidation Process

The basic oxidation process is the sharing of valence electrons between silicon and oxygen to form four silicon-oxygen bonds. For oxidation in pure oxygen, which produces "dry" oxides, the stoichiometric chemical reaction producing the oxide is

$$Si(\text{solid}) + O_2 \rightleftharpoons SiO_2(\text{solid}) \tag{5.1}$$

The stoichiometric chemical reaction for producing the oxide film in water vapor, "wet" oxides, is

$$Si(\text{solid}) + 2H_2O \rightleftharpoons SiO_2(\text{solid}) + 2H_2 \tag{5.2}$$

Reaction (5.1) describes the overall reaction between oxygen and silicon, and reaction (5.2) describes that between water vapor and silicon at a pressure of 1 atm, and elevated temperatures, typically 900-1200°C.

5.6 Photolithography

Photolithography was used to make the dot pattern[47]. The slective removal of the silicon dioxide was carried out by a photolithographic process using photoresistant material. A mask of glass containing an opaque printed pattern of the areas into which impurities were diffused was secured over the wafer, and the structure was exposed to ultraviolet light, with a photomask being used as a template for the diffused and non-diffused areas[48]. This light "fixed" the photoresist in all areas of the wafer except those covered by the opaque pattern of the masks[49]. The entire wafer was then immersed in a solution which removed unexposed photoresist, uncovering the SiO_2 film in these regions. The fixed photo-resist film was not affected by the solution.

The wafer was then subjected to an etching solution which attacked and removed the uncovered SiO_2 film but cannot penetrate the fixed photoresist. The SiO_2 film, was then removed only in those areas which, subsequently, were diffused. After etching, the fixed photoresist was removed and the result was an opening through the oxide layer in which the wafer was ready for the diffusion cycle.

5.7 Gate Electrode

To make the gate electrode, aluminium was deposited about 3000Å thick in a high vacuum system by evaporation. It was difficult to contact an aluminium gate with a probe without significant series resistance

because of the protective oxide layer that forms on it an exposure to room air. It was much easier to make a low resistance contact to a metal such as gold, which did not form a protective oxide. Unfortunately, because gold is not an active metal, it did not bond strongly to the oxide surface.

To obtain reproducible results, it was desirable that the gate electrode adhere strongly to the oxide surface. This problem was solved by using a bimetallic gate. An active metal such as chromium was first deposited on the oxide surface. This metal chemically react with SiO_2 and strongly adhere. Next gold was immediately deposited over the active metal. Because the active metal was in a vacuum, no protective oxide layer formed. Thus, gold formed on adherent ohmic metal-to-metal contact but did not form a protective oxide layer when exposed to room air. Then, Cr-Au was deposited by evaporation to the same thickness.

5.8 Deposited Silicon Nitride

Although silicon nitride is not an oxide, it is so intimately connected with silicon dioxide in integrated circuit technology. Chemical Vapor deposition of the silicon nitride was used from a gaseous mixture of either SiH_4 or $SiCl_4$ diluted to 1-3% in nitrogen or hydrogen and ammonia. The volatile silicon compound, silane or silicon tetrachloride was reacted with the ammonia at temperatures above 850°C to form silicon nitride on substrate surfaces[34,50,51].

The most important parameters determining the deposition rate of silicon nitride films are the substrate temperature, the composition and

flow rate of the reactant mixture. The substrate temperature was in the range of 800-1100°C. The interface characteristics of silicon-silicon nitride structures depend to a large extent on the surface condition of the substrate prior to the deposition process.

VI MEASUREMENT APPARATUS

In this work, the set of very sensitive electrical measurements were done to detect low charge densities. Block-diagram of C-V and G-V measuring-apparatus is shown in Fig.14. Computer programming was done to collect data interfacially from the measuring instruments: HP model PA meter/Dc voltage source, HP model LCR multifrequency meter, HP model multimeter and to plot C-V and G-V curves using the printer and the plotter.

6.1 PA Meter/DC Voltage Source 4140B[52]

The HP model 4140B PA meter/DC voltage source comprises a high stability PA meter with 10^{-15} A (max.) resolution coupled with two programmable DC voltage sources to ensure useability in many application areas. The PA meter has a basic accuracy of 0.5% over wide measurement ranges ($\pm$ 0.001 x 10^{-12}A - $\pm$ 1.99 x 10^{-2}A) enabling stable PA current measurement at 10^{-15}A ($\pm$ count). One of the two programmable DC voltage sources (V_A) can operate not only as a programmable DC voltage source, but also as a unique stair case (,) and accurate ramp (,) generator.

With the 4140B it is especially easy to make a quasi-static C-V measurement which is usually employed as one of the measurements when trying to improve semiconductor quality. The 4140B measures capacitance value by the following formula:

$$C = \frac{I(\text{measured Current Value})}{dv/dt\ (\text{ramp rate})} \qquad (5.3)$$

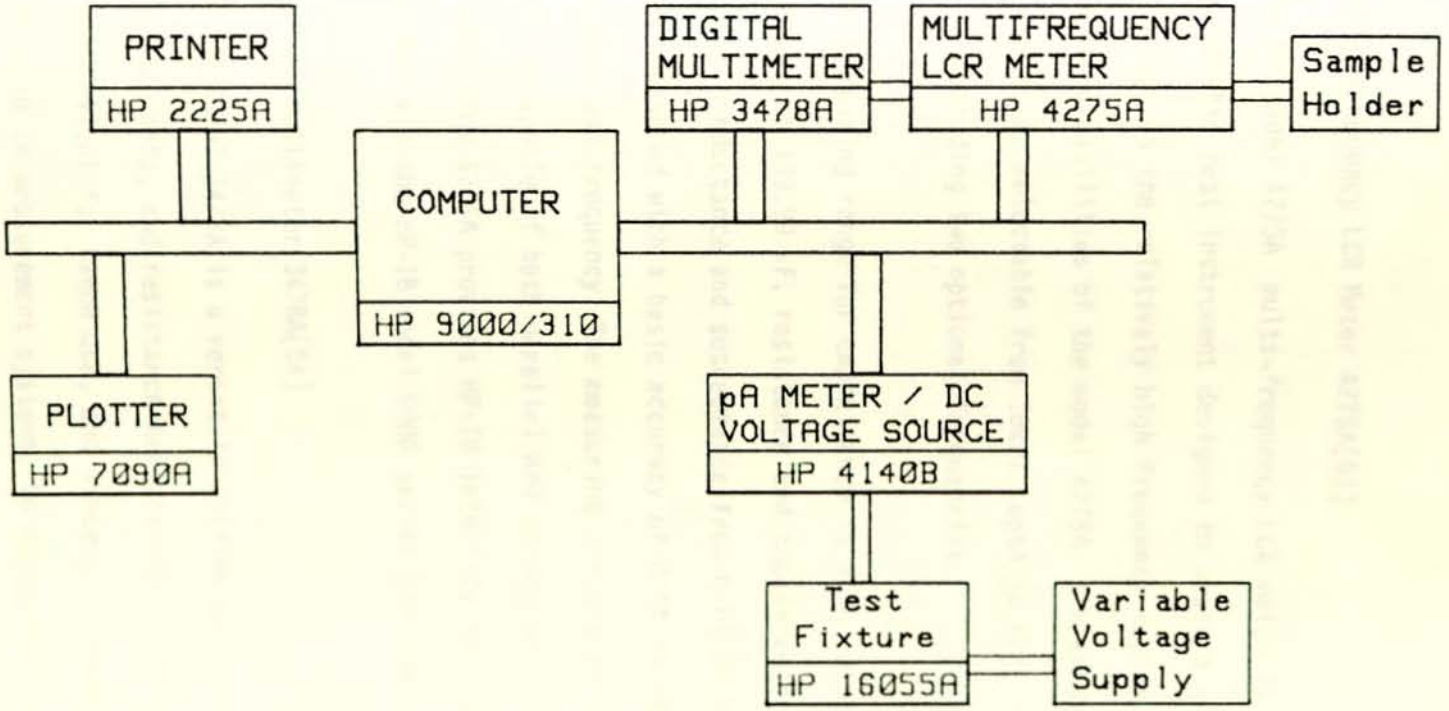

Fig.14 Block - Diagram of
C-V & G-V Measuring-Apparatus

For a C-V measurement, the 4140B provides two measurement ranges, 0.0pF - 199.9 pF in 0.1 pF steps and 200 pF - 1999 pF in 1pF steps. The 4140B provides HP-IB computer interface for remote control and data output via the HP-IB computer.

6.2 Multi-Frequency LCR Meter 4275A[53]

The HP model 4275A multi-frequency LCR meter is a high perfrmance, fully automatic test instrument designed to measure values of an impedance element in the relatively high frequency region. The wide range measurement capabilities of the model 4275A are enhanced by the 12 spot test frequencies selectable from 10kHz upto 10 MHZ in a 1-2-4-10 sequence, including two optional frequencies.

The measuring range for capacitance is from 0.01fF (femto farads = 10^{-15} farads) to 199.99 μF, resistance and impedance from 0.01 mΩ to 19.999 MΩ, conductance and susceptance from 0.01 nS to 19.999 S all of which are measured with a basic accuracy of 0.1% to 5% depending on test signal level and frequency. The measuring circuit for the device to be measured is capable of both parallel and series equivalent circuit measurement. The 4275A provides HP-IB interface for remote control and data out put via the HP-IB model 9000 series 310 computer.

6.3 Digital Multimeter 3478A[54]

The HP-Model 3478A is a versatile multimeter with dc and ac volts, dc and ac currents, and resistance measurement capabilities. The multimeter is excellent for bench use, and since it is remotely programmable, it can be used in measurement systems. No mechanical adjustments are necessary to calibrate the 3478A.

The 3478A is able to make dc volts measurements from .1 V to 300 V in five ranges: 30mV, 300mV, 3V, 30V, and 300V. The 3478A uses a true RMS AC to DC converter to measure ac voltages from 1 V to 300 V in four ranges: 300mV, 3V, 30V, and 300V. The response of the converter is from 20Hz to 100kHz on all ranges. All ranges are protected from input voltages upto 450V peak.

6.4 Description of Computer Programs

Real time computer programs for measurements and for plotting curves using spline interpolation and numerical integration were constructed as shown in Appendices A and B.

Appendix A represents computer program constructed for high frequency MIS capacitance method of measurements, numerical integration, the set of interpolation and calculation of derviatives, plottings and additional calculations. Short discussion of the contents for the computer program are given below.

Lines from 110 to 160 is part of a program for measurement using multifrequency LCR meter.

Lines from 240 to 450 represent constants of measurements and formulas used in calculations.

Lines from 470 to 520 is installation of parameters of subprogram for numerical integration (refer 3380).

Lines from 540 to 790 is part of a program for theoretical calculation (2.4.1) and plotting of the voltage versus total capacitance using numerical integration (refer 6790).

Lines from 910 to 1070 and 1090 to 1290 are for calculating theoretical capacitance versus potential and experimental capacitance versus voltage respectively using splin interpolation (refer 7850).

Lines from 1310 to 1790 are for plotting theoretical capacitance versus potential curves and experimental capacitance versus voltage curves. (See 2.4 and 4.1).

Lines from 1810 to 1960 and 2580 to 2730 are for theoretical and experimental derivatives of voltage dV_G versus potential $d\psi_s$ respectively using spline interpolation (Ref.4.1).

Lines from 1980 to 2790 and 2750 to 2790 are for plotting theoretical and experimental curves of ψ_s versus V_G.

Lines from 2810 to 3340 are for plotting interface trap level density versus energy (Refer 7.1).

Lines from 3380 to 6620 is subprogram for numerical integration.

Lines from 6630 to 6770 is part of a program for ψ_s versus V_G (Refer (2.38)).

Lines from 6790 to 7310 is Graphics for plotting theoretical and experimental curves of high frequency MIS capacitance versus voltage.

Lines from 7340 to 7600 is subprogram for measurement of the experimetntal voltage versus capacitance using the multifrequency LCR meter.

Lines from 7620 to 7710 are for calculating flatband voltage shift using experiment. (Refer 2.4.1).

Lines from 7730 to 7820 are for plotting experimental capacitance versus voltage before and after shift of voltage.

Lines from 7850 to 8660 is subprogram for spline interpolation and derivative calculations.

Appendix B represents computer program constructed for combined high-low frequency MIS capacitance method of measurements, the set of interpolation and calculation of derivatives, plottings and additional calculations.

Lines from 100 to 320 represent constants of measurements and formulas used in calculations.

Lines from 340 to 430 is installation of parameters of subprogram for Graphics (Refer 2040).

Lines from 450 to 490 is installation of parameters of subprogram for plotting (refer 2550).

Lines from 510 to 730 is program for measurement of quasistatic frequency using pA meter DC/voltage source and plotting experimental capacitance versus voltage.

Lines from 750 to 950 and 970 to 1150 are for plotting measured high frequency capacitance versus voltage and quasistatic frequency capacitance versus voltage using spline interpolation and derivative calculations (Refer 3050).

Lines 1170 to 1280 and 1300 to 1440 are for calculation of energy versus ψ_s Eq.(7.1) using spline interpolation.

Lines from 1460 to 1900 and 1920 to 2020 are for plotting interface trap level density versus energy (Refer Eq.(7.1) and (7.4)).

Lines from 2040 to 2530 and from 2980 to 3040 are subprogram for Graphics of plotting combined high-low frequency MIS capacitance versus voltage.

Lines from 2550 to 2870 is program for measurements of the experimental voltage versus capacitance using multifrequency LCR meter and digital multimeter.

Lines from 2880 to 2970 are for calculation of experimental voltage shift. And Lines from 3050 to 3740 is subprogram for spline interpolation and derivative calculations.

VII. EXPERIMENTAL RESULTS AND DISCUSSIONS

Results of the experiments for different types of samples using the high frequency MIS capacitance and the combined high-low frequency of the measurement techniques are presented and discussed. The samples are n-type, phosphorus doped of donor concentration $N_D = 10^{15} cm^{-3}$ having resistivity of $\rho = 4.5 \Omega$ - cm oriented in the [100] direction with surface area of $A = 4x10^{-2}$ cm^2. The results of measurements were obtained in dark condition, at room temperature and were automatically recorded interfacially on the HP 9000/310 computer. Real time computer programmes for measurements and numerical analysis were constructed.

7.1 High Frequency MIS Capacitance Method

The frequency of measurement range was from 10KHZ upto 10MHZ in a 1-2-4-10 sequence. The measuring circuit for the experiment was series equivalent circuit of measurement. Using integration and spline interpolation the C-V curve of the theoretical one is plotted in Fig.15(a). In this figure the initial curve of the experimental result of sample 7 is represented by dotes to the right of the theoretical curve. Taking the flat band capacitance as reference point for both the theoretical and experimental curves, the experimental curve of capacitance versus voltage of high frequency is shifted along the voltage axis to make the flat band points coincide as shown in Fig.15(b). The range of the voltage in this figure is from -2V to 2V and the selected frequency is 200KHZ. The top of the accumulation region of high frequency theoretical curve fit to the experimental curve by adjusting thickness of the oxide as a parameter.

Measurement of samples used were with initial value of thicknesses as given by the factory which was measured by ellipsometry (see Table 1). But thickness measurement by ellipsometry method is not accurate enough than the set of sensitive electrical measurements used. Similarly, the inversion region of the high frequency fit to the experimental curve by adjusting the doping concentration of the sample as a parameter. The initial value of the doping concentration N_D was taken from Chapter V as it was given by the factory.

From the fitted theoretical curves, the dependence of C_{HF} versus surface potential ψ_S is obtained by knowing ψ_S corresponding to a given C_{HF} in the ideal curve and measuring V_G corresponding to the same C_{HF} in the real curve. From this relation ψ_S versus V_G curve is constructed as shown in section (4.1). A theoretical plot of high frequency capacitance C_{HF} versus surface potential ψ_S was compared with the measured plot of high frequency capacitance C_{HF} versus voltage V_G as shown in Fig.16. For any choice of capacitance, comparison of these two plots determined surface potential ψ_S versus voltage V_G as shown in Fig.17. Fig.17 is the result after spline interpolation was applied to the theoretical curve (a) and the experimental curve (b) comparison of the curves (a) and (b) of Fig.15 shows the interface state density exist due to distortion of the curves but it is not simple to find this small interface state density by differentiation of the curve. From Fig.17 it is possible to see the necessary conditions for obtaining the interface state density as it shows that interface states stretch the ψ_S versus V_G curve along the gate bias axis. It is this ψ_S versus V_G relationship that contains all the information about interface level density in high frequency C-V curve.

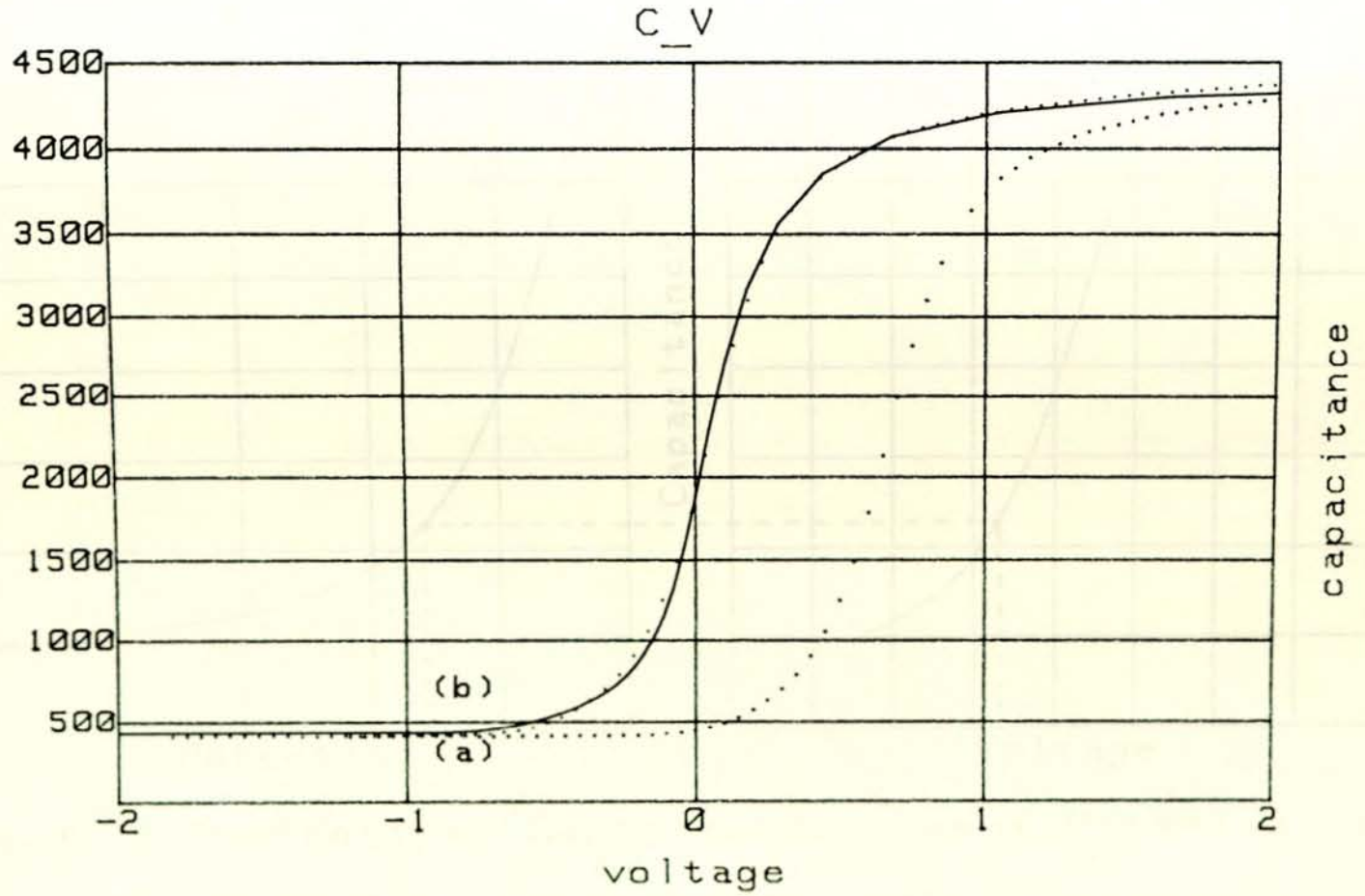

Fig. 15 High-Frequency MIS Capacitance-Voltage Curves
(a) Theoretical Curve (b) Experimental Curve
Sample 7

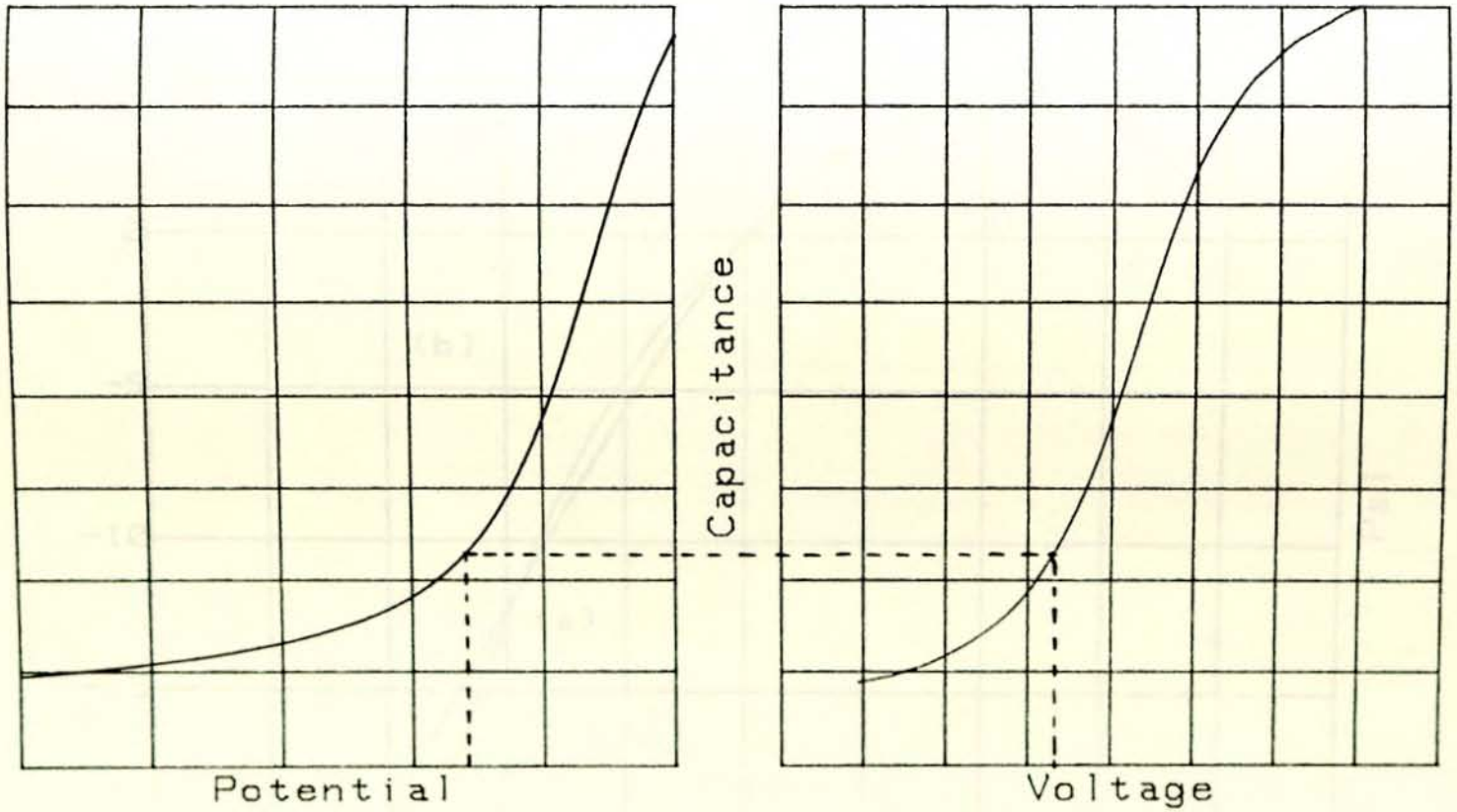

Fig.16 A Theoretical Capacitance versus Potential and Experimental Capacitance versus Voltage

Sample 7

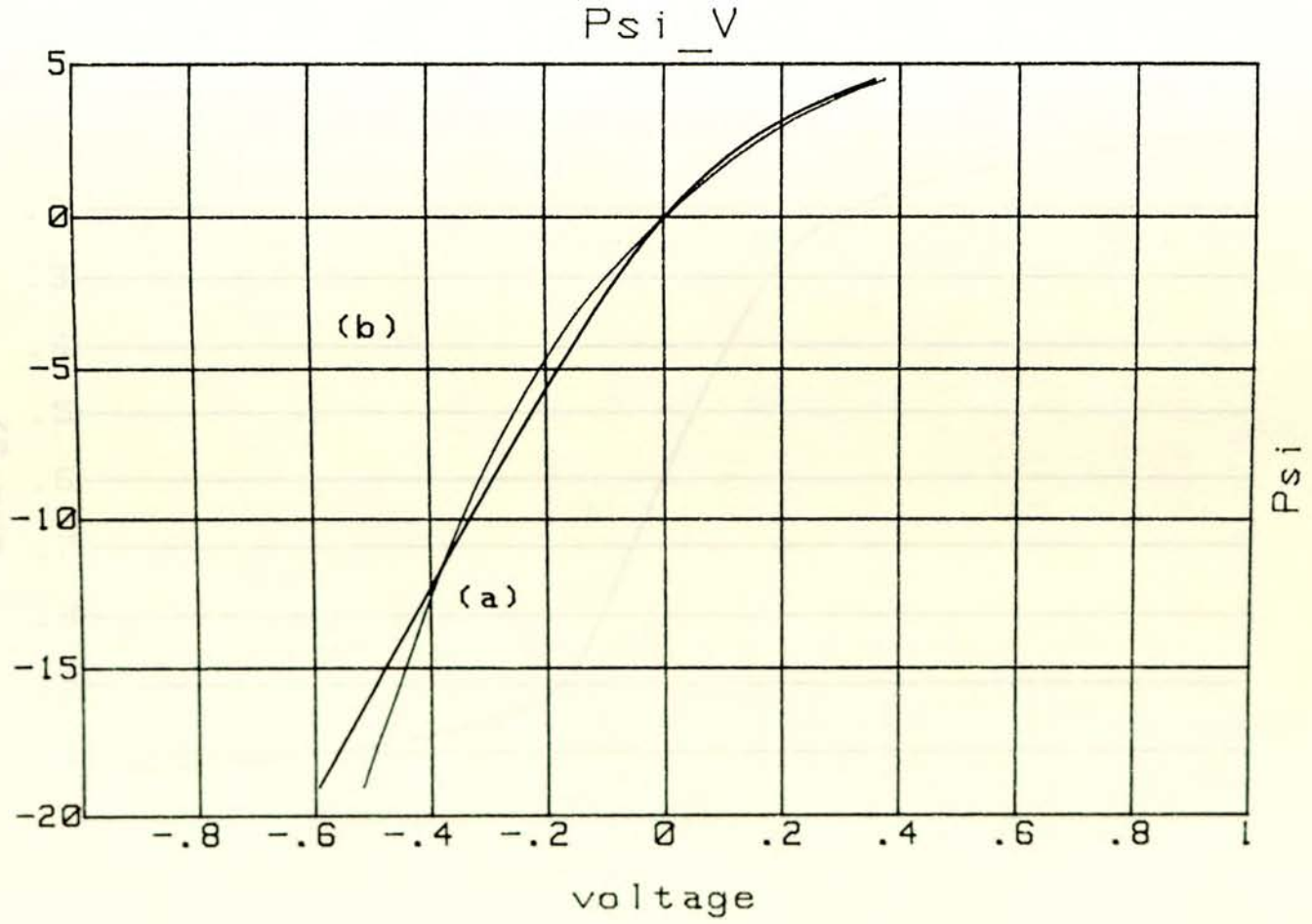

Fig.17 Surface Potential Versus Applied Voltage
(a) Theoretical Curve (b) Experimental Curve
Sample 7

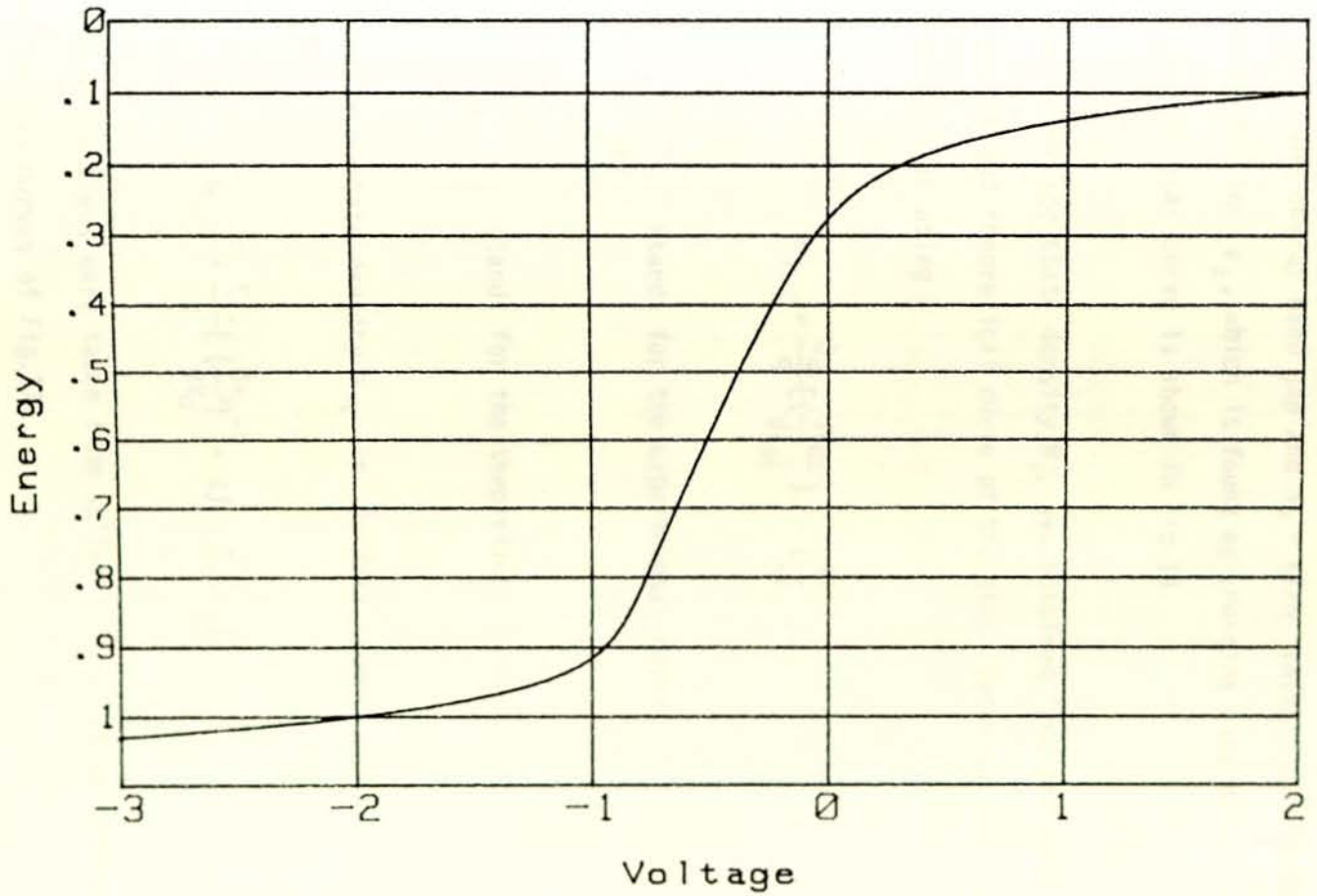

FIG. 18 Interface Energy Versus Bias

Fermi level at the interface from Fig.11 is found by

$$\frac{E_C - E_F}{q} = \frac{E_g}{2q} + \psi_S - \phi_B \qquad (7.1)$$

where E_g is the energy band gap and $\phi_B = KT/q \ \ell n(N_D/n_i)$. The band gap is scanned by varying ψ_S, which is found by changing gate bias. Interface energy versus bias curve is shown in Fig.18.

The interface state density N_{it} was obtained from the results of measurements and theoretical curve of the high frequency capacitance as a function of bias using

$$N_{it} = \frac{C_{ox}}{q}\left[\left(\frac{dV_{GE}}{d\psi_{SE}}\right) - \left(\frac{dV_{GT}}{d\psi_{ST}}\right)\right] \qquad (7.2)$$

where $\frac{dV_{GE}}{d\psi_{SE}}$ stands for the experimental curve.

and $\frac{dV_{GT}}{d\psi_{ST}}$ stands for the theoretical curve.

The interface state density N_{it} is derived from

$$N_{it} = \frac{C_{ox}}{q}\left[\left(\frac{d\psi_S}{dV_G}\right)^{-1} - 1\right] - C_D(\psi_S) \qquad (7.3)$$

and the derivatives were taken from spline interpolation programmes of the corresponding curves of Fig.17.

To determine the density and energy distribution of interface states

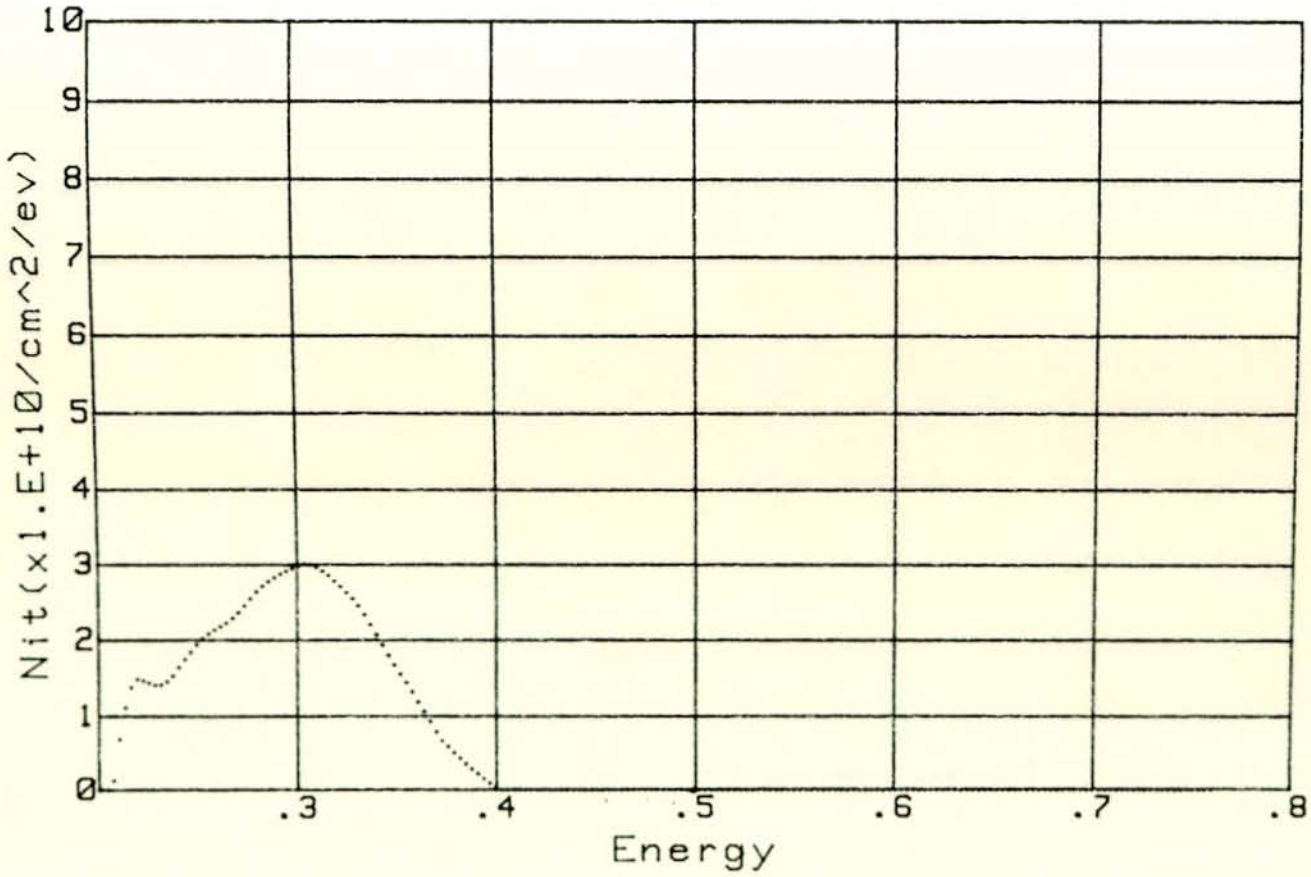

Fig.19 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 7

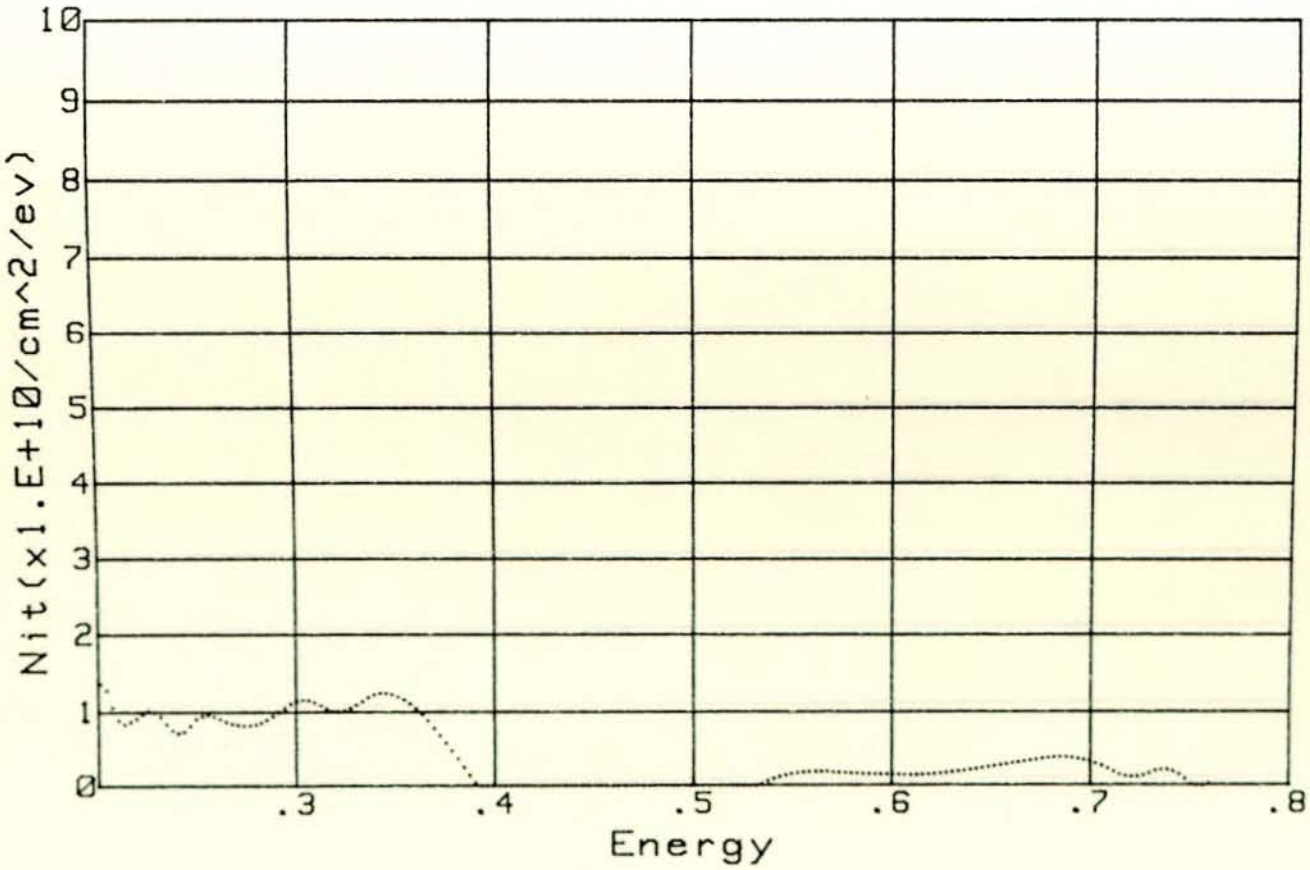

Fig.20 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 1

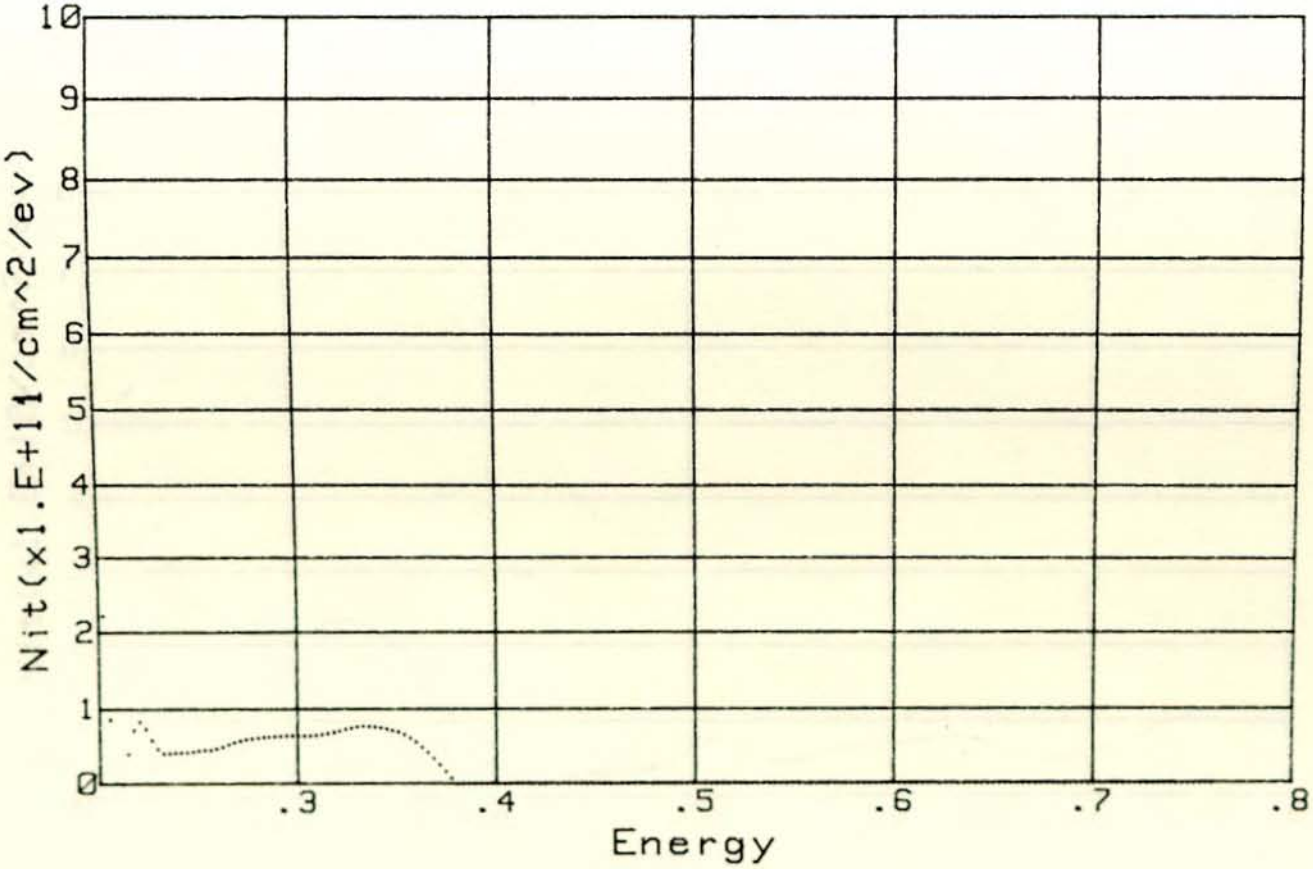

Fig.21 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 2

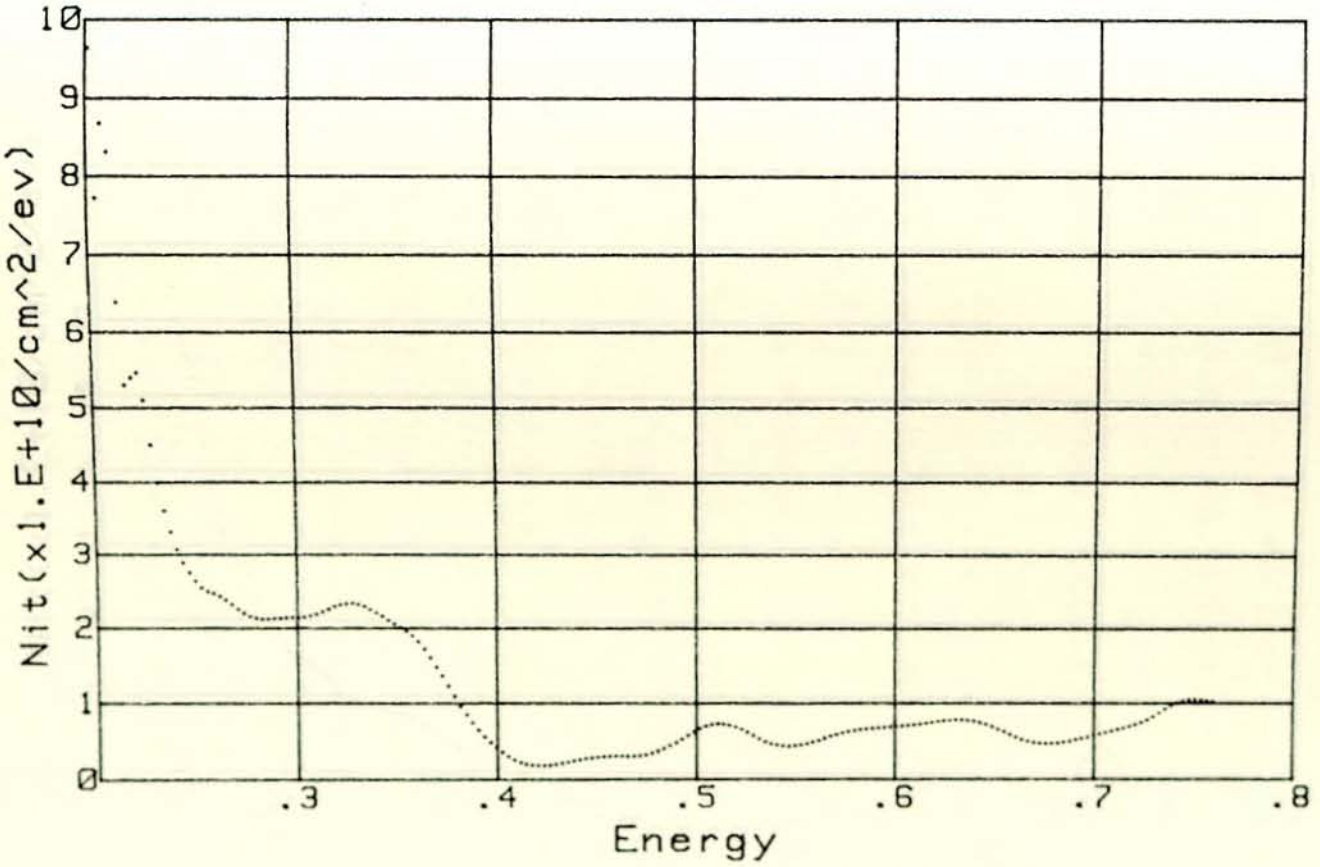

Fig.22 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 4

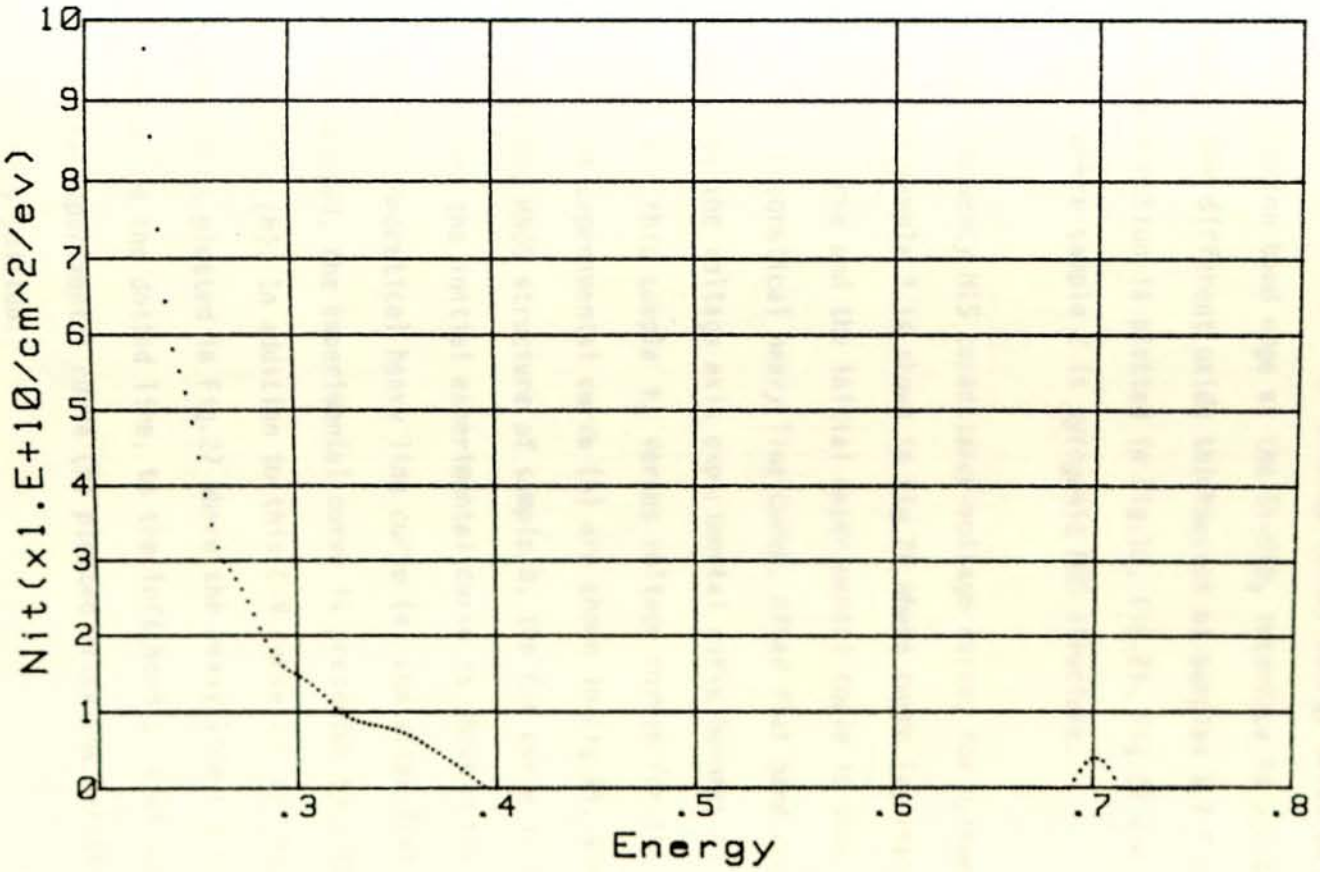

Fig.23 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 6

at silicon-silicon dioxide interfaces, Real time computer programme was constructed using numerical integration and spline interpolation methods as shwon in Appendix A.

The interface trap level density versus energy measured with respect to the conduction band edge at the $Si-SiO_2$ interface is plotted in Fig.19. Similarly for different oxide thicknesses of samples 1,2,4 and 6 the energy distribution is plotted in Fig.20, Fig.21, Fig.22 and Fig.23 respectively. Where sample 2 is pyrogenic MOS structure.

High-frequency MIS capacitance-voltage curves for pyrogenic MNOS structure of sample 3 is shown in Fig.24 where curve (a) represents the theoretical curve and the initial experimental curve is shown to the right side of the theoretical heavy line curve. After flat band capacitance is shifted along the voltage axis experimental curve becomes as shown in curve (b). For this sample ψ_s versus voltage curves for theoretical curve (a) and experimental curve (b) are shown in Fig.25. Similarly for irradiated dry MNOS structure of sample 8, the C-V curve is shown in Fig.26. In this figure the initial experimental curve is shown to the left hand side of the theoretical heavy line curve (a) and after flat band capacitance is shifted, the experimental curve is presented by dotted curve as shown in curve (b). In addition to this C-V curve for dry MNOS structure of sample 10 is plotted in Fig.27 where the heavy line (a) is the theoretical curve and the dotted line, to the left hand side of the theoretical curve is the experimental curve (b) plotted after the original experimental curve is shifted.

In Fig.24 it is possible to use graphical differentiation to obtain

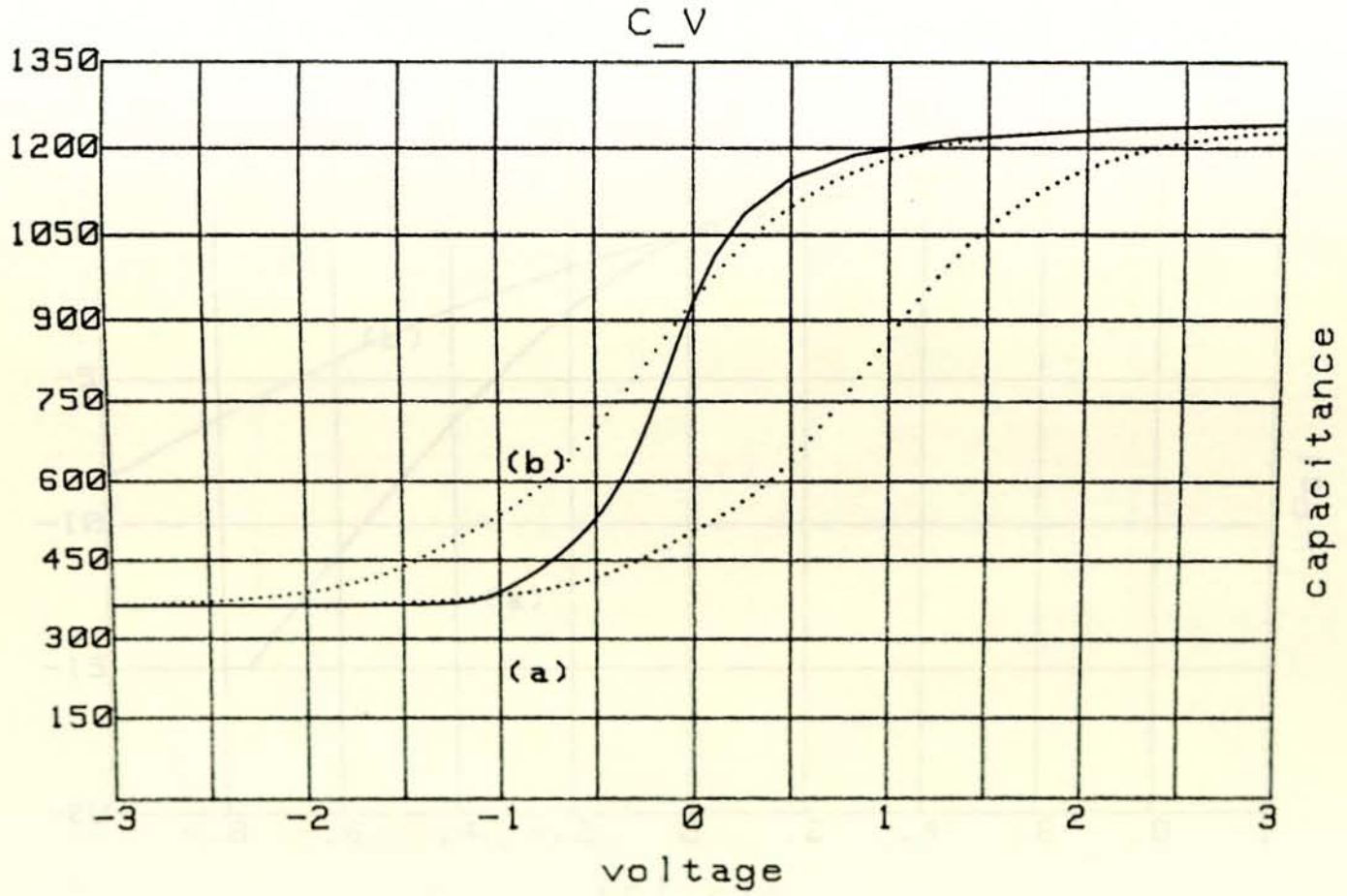

Fig.24 High-Frequency MIS Capacitance-Voltage Curves

(a) Theoretical Curve (b) Experimental Curve

Sample 3

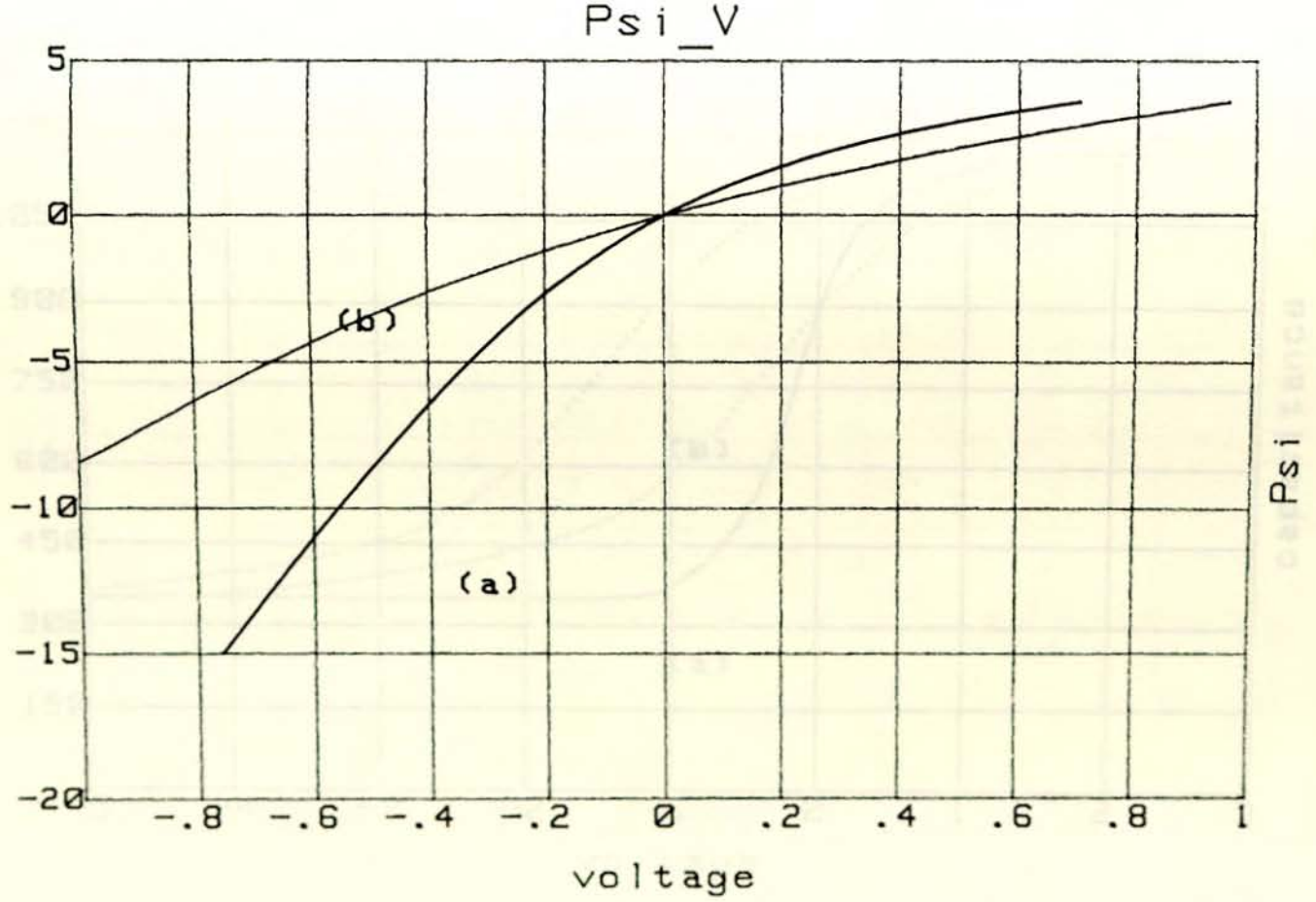

Fig.25 Surface Potential Versus Applied Voltage
(a) Theoretical Curve (b) Experimental Curve
Sample 3

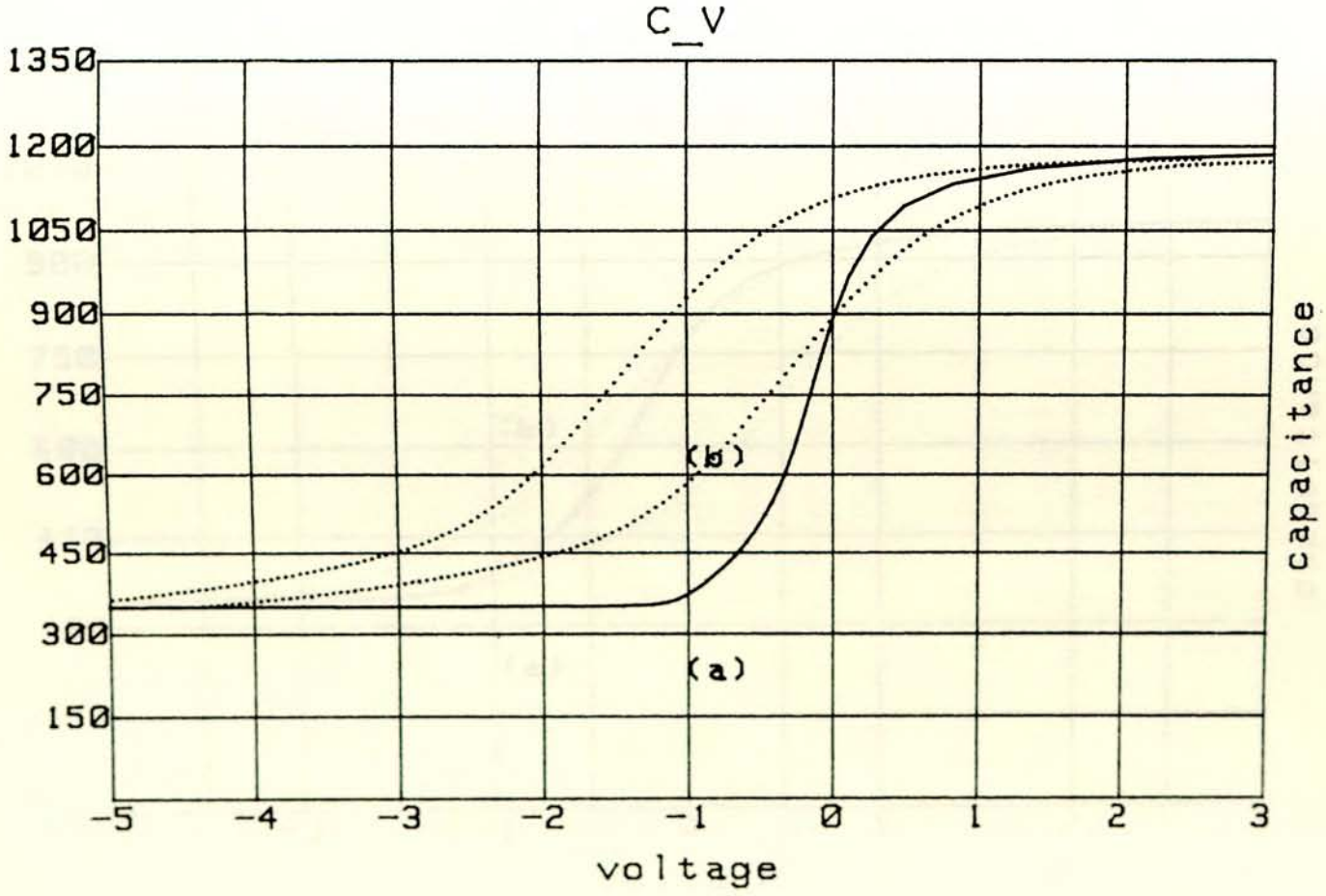

Fig.26 High-Frequency MIS Capacitance-Voltage Curves
(a) Theoretical Curve (b) Experimental Curve
Sample 8

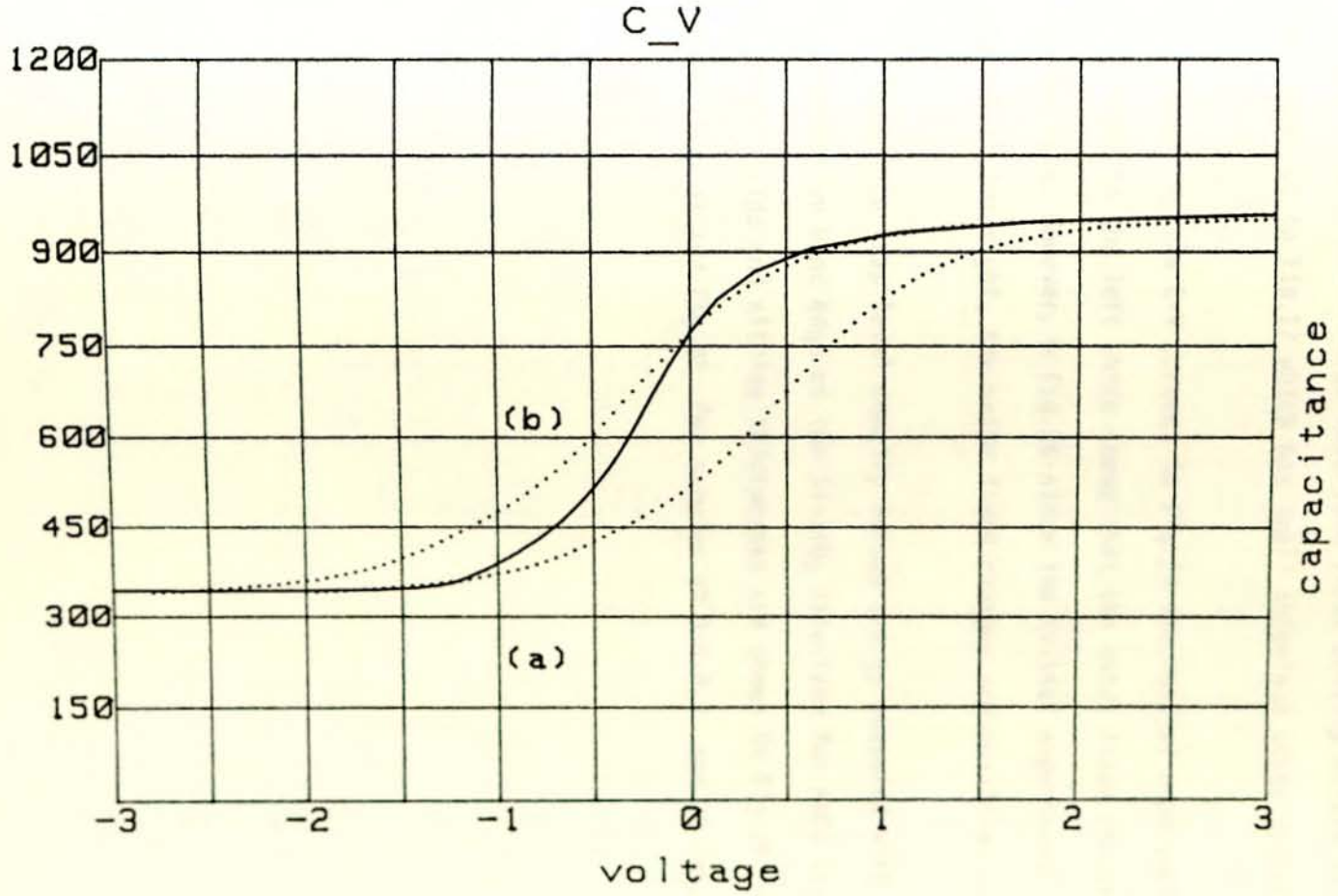

Fig.27 High-Frequency MIS Capacitance-Voltage Curves
(a) Theoretical Curve (b) Experimental Curve
Sample 10

the interface state density. Compared with the other C-V curves the slope of this curve is small and inclined which shows that more interface state density exists. Similar information is found from Ψ_S versus V_G curve. That is, Fig.25 shows large interface state density exists in the interface compared to Fig.17 which has small interface state density.

Comparing the C-V curves, in Fig.24 the initial experimental curve is shifted to the left which shows that the oxide fixed charges present are negative. However, in Fig.26 since the initial experimental curve is shifted to the right, the oxide fixed charges are positive.

Interface trap level density versus energy measured with respect to the conduction band edge at the Si-SiO_2 interface for MNOS structures of different oxide and nitride thicknesses are shown in Fig.28, Fig.29, Fig.30, Fig.31 and Fig.32 for samples of 3,5,8,9 and 10 respectively.

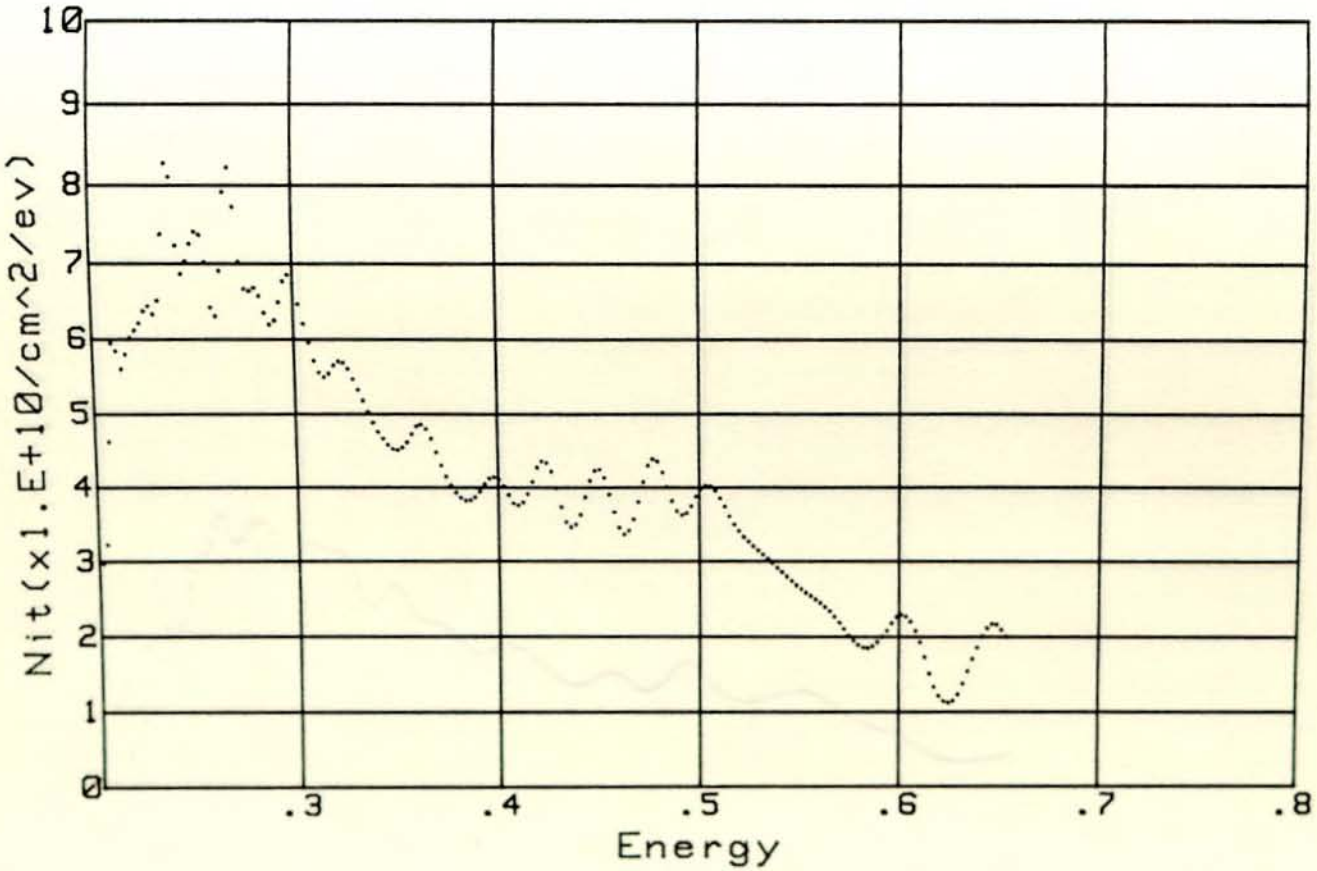

Fig.28 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 3

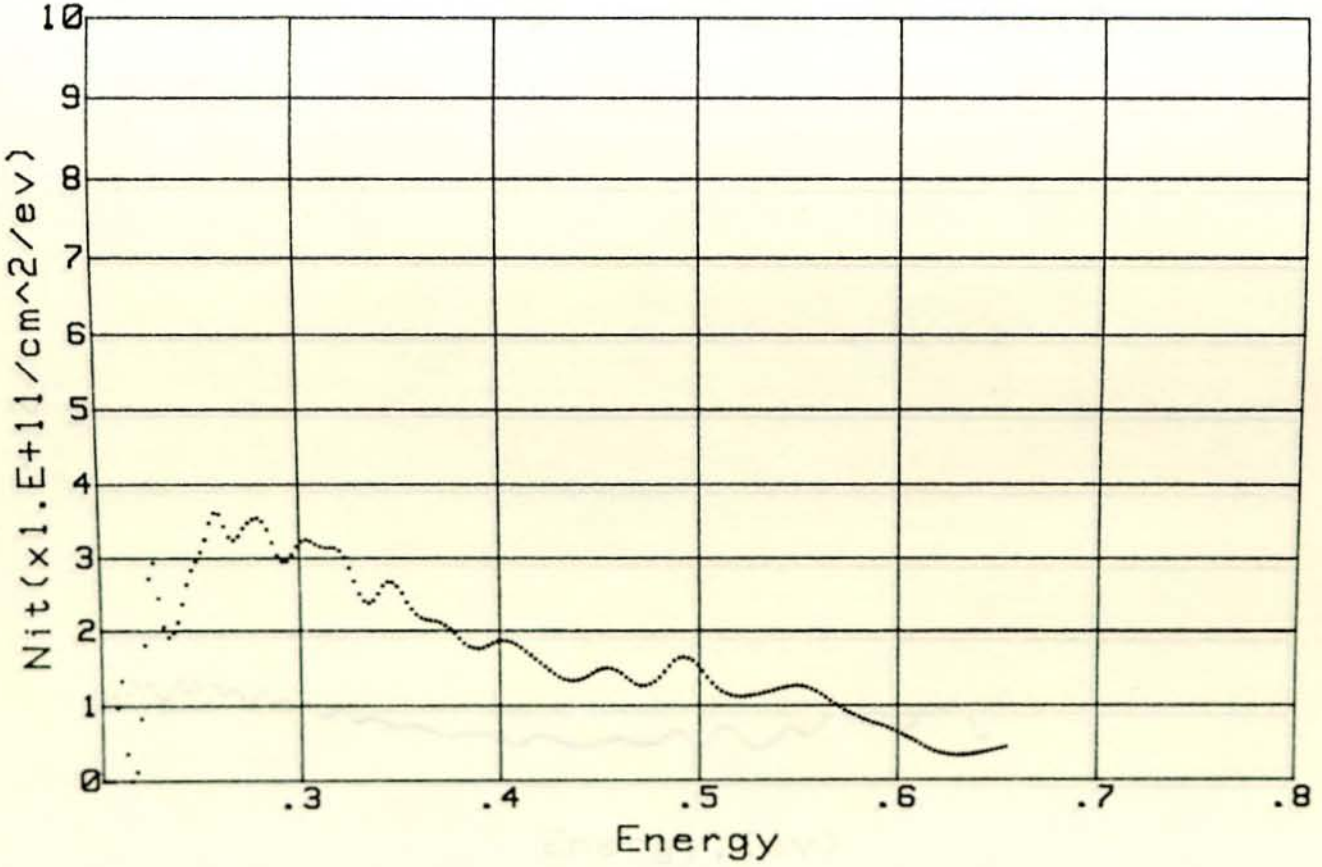

Fig.29 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 5

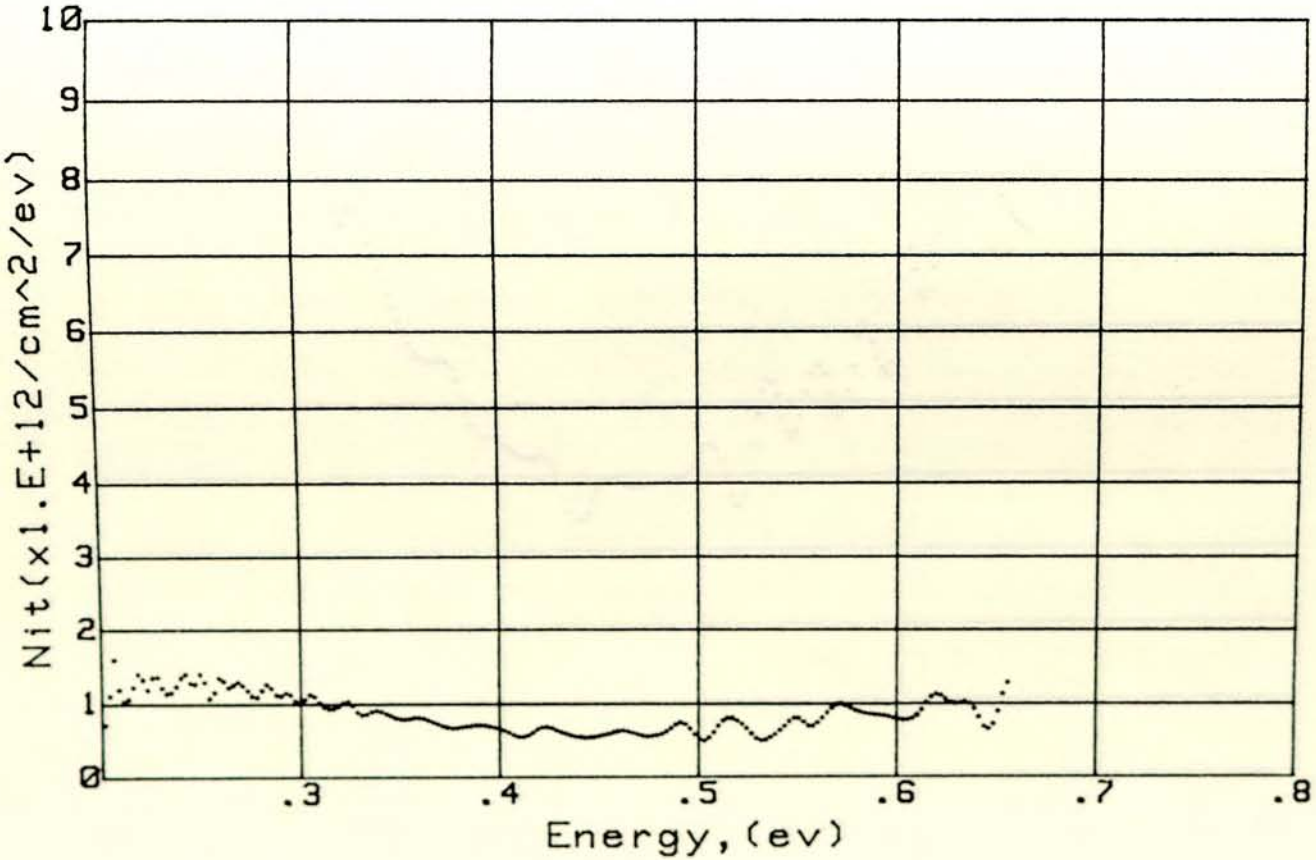

Fig.30 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 8

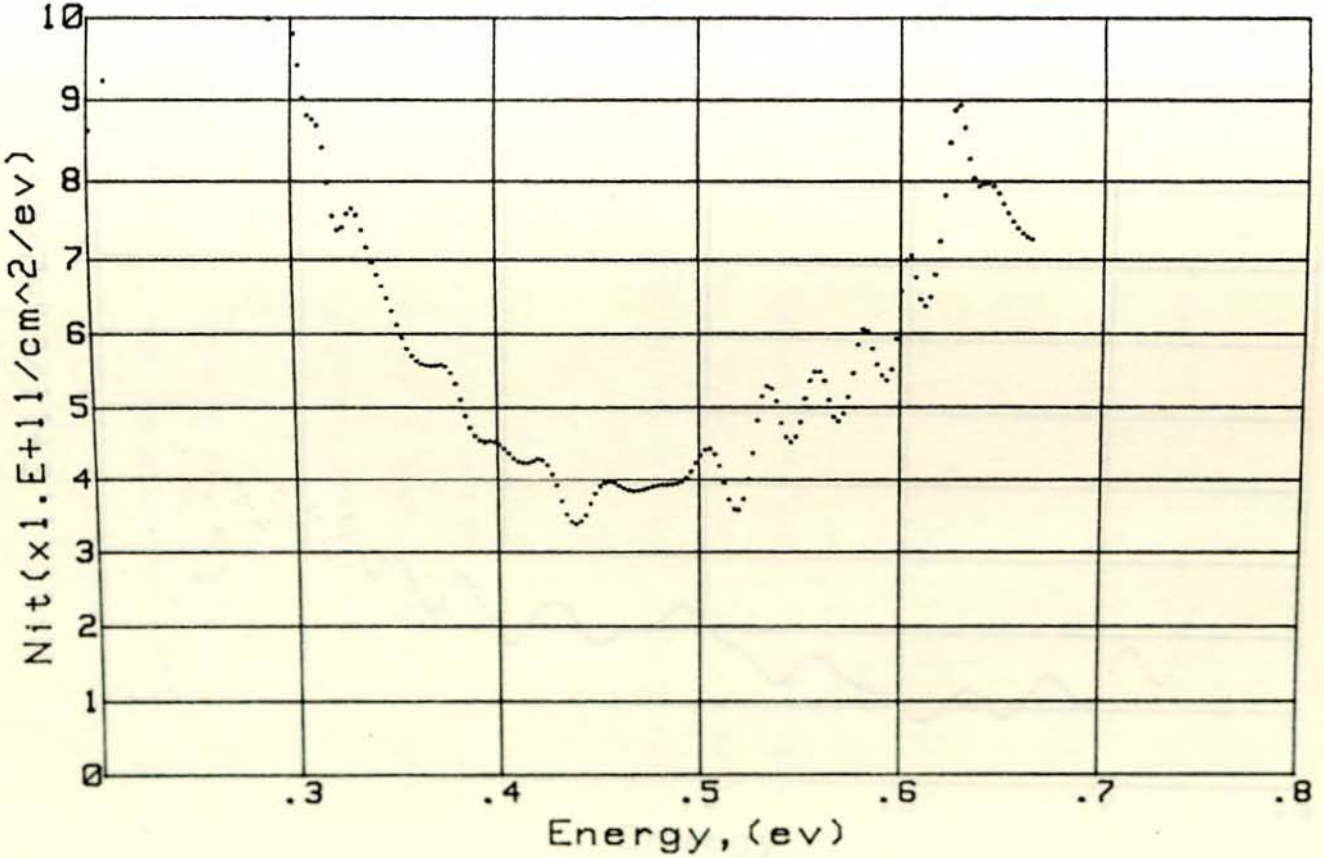

Fig.31 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 9

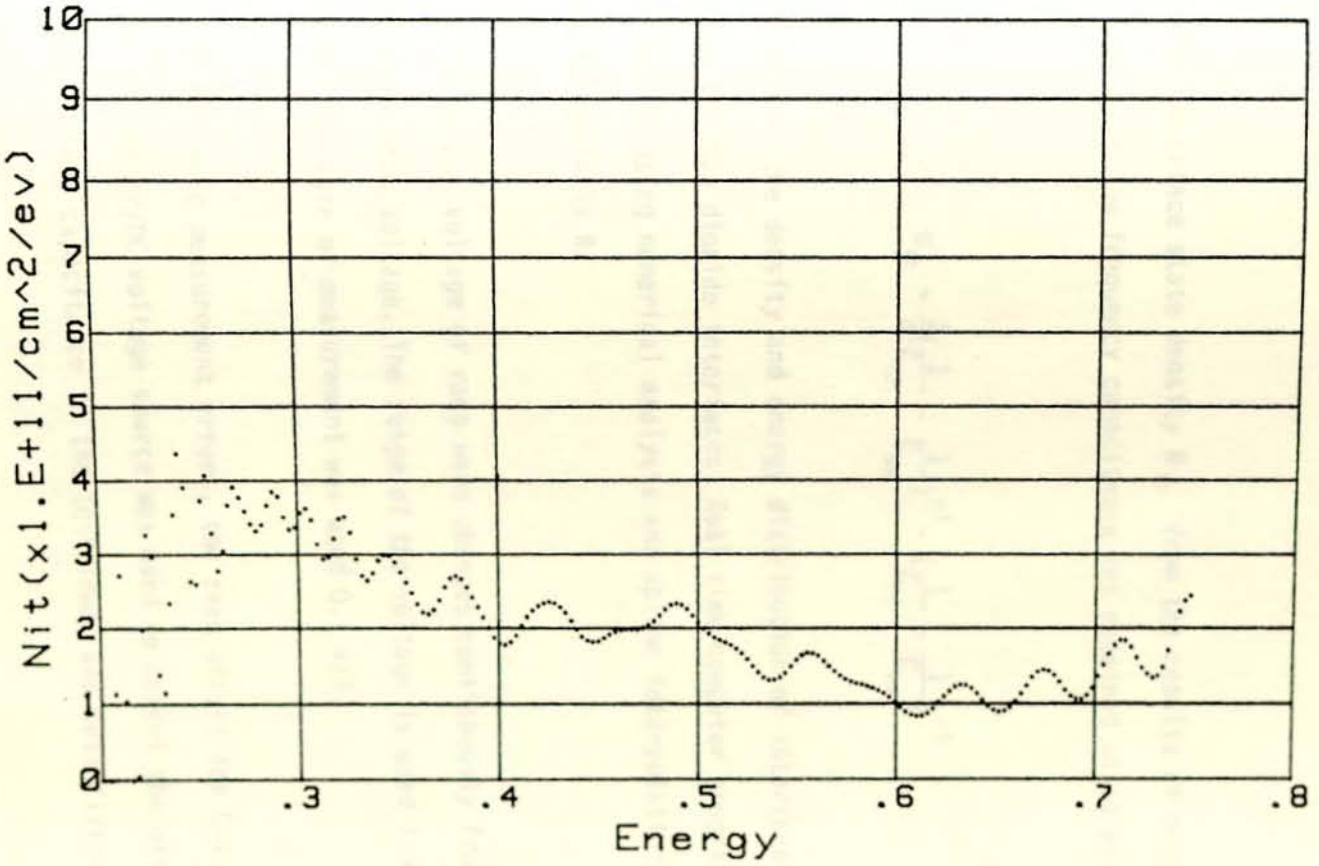

Fig.32 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 10

7.2 Combined High-Low Frequency MIS Capacitance Method

The interface state density can be extracted from the measurement of interface trap capacitance directly from the measured combined high-low frequency C-V curves without knowing the theoretical and calculated value of C_D .

The interface state density N_{it} from the results of measurements of combined high-low frequency capacitnace was obtained using equation (4.3.8) by

$$N_{it} = \frac{1}{q}\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \qquad (7.4)$$

To determine the density and energy distribution of interface states at silicon-silicon dioxide interfaces, Real time computer programme was constructed using numerical analysis and spline interpolation methods as shown in Appendix B.

The output voltage of ramp wave changes continuously from start voltage to stop voltage. The range of the voltage is used from -5V to 3V and the ramp rate of measurement was used 0.1 V/S.

To minimize measurement errors, the zero offset for C-V measurement of the ^{pA} meter/DC voltage source was used to cancel the offset error caused by stray capacitance in the test leads and test fixtures.

Using spline interpolation the combined high-low frequency MIS capacitance-voltage curve is shown in Fig.33 of sample 1 dry oxide MOS structure.

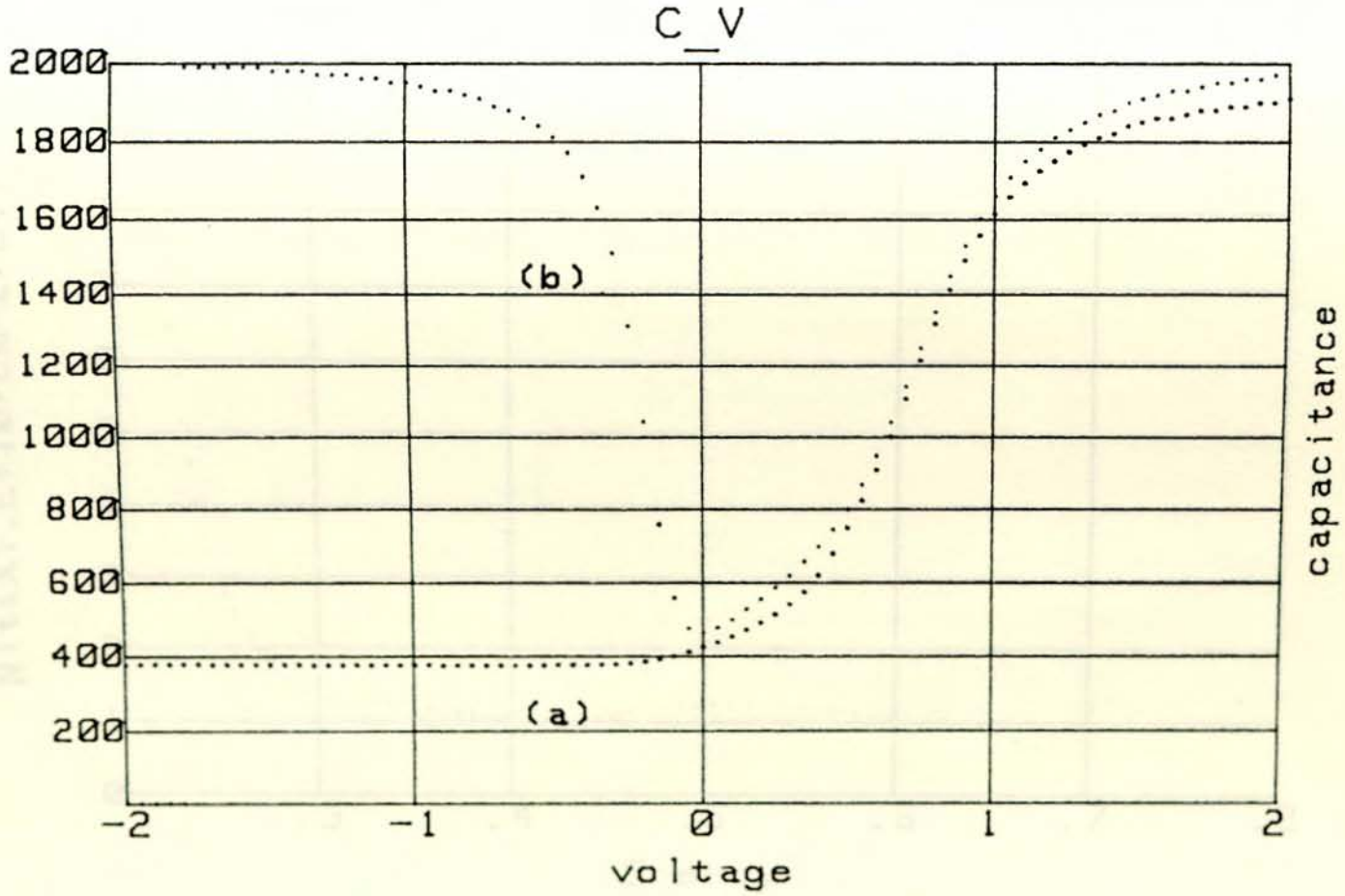

Fig.33 Combined High-Law Frequency MIS Capacitance-Voltage Curve
(a) High Frequency Curve (b) Low Frequency Curve
Sample 1

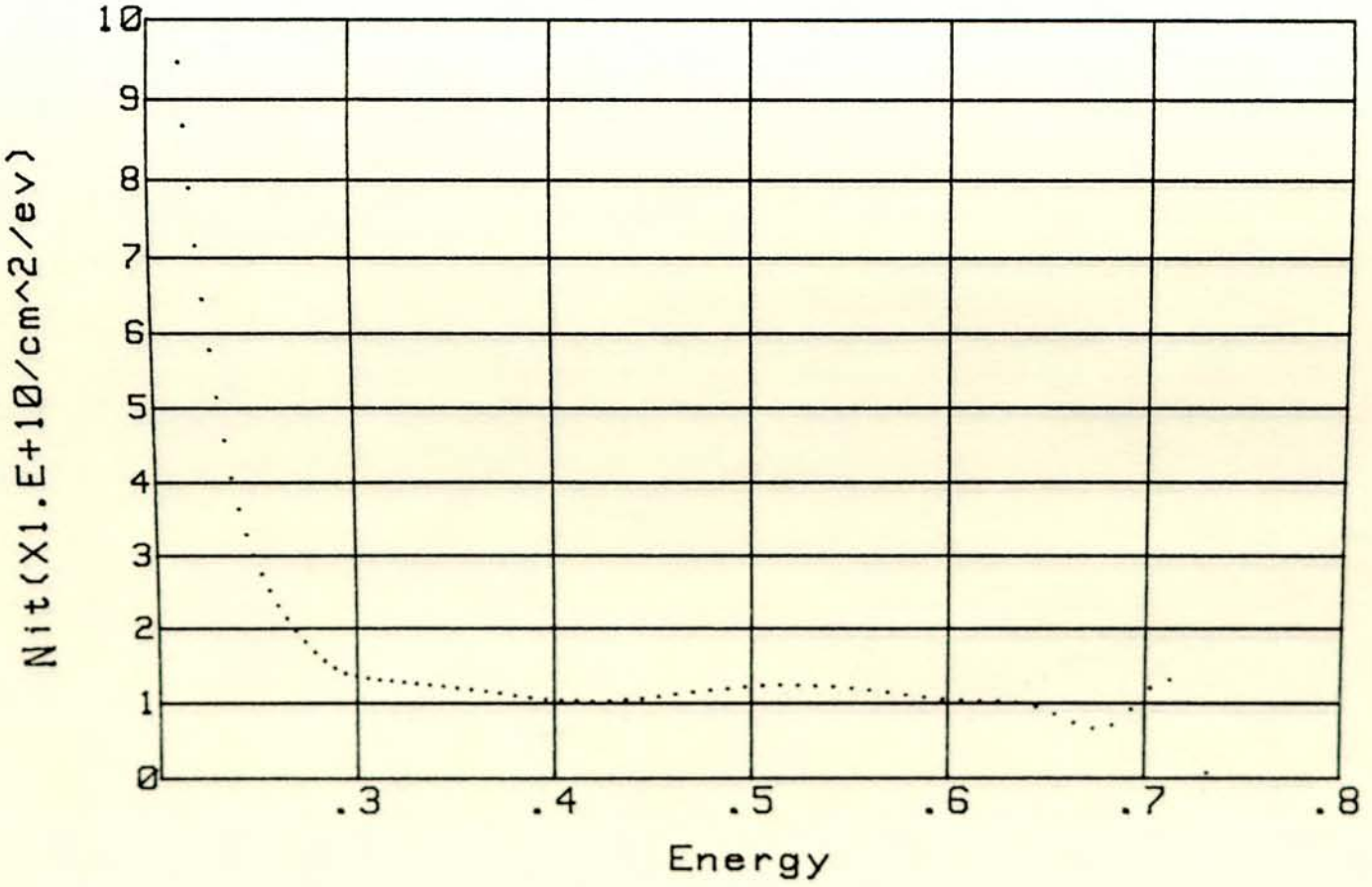

Fig.34 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 1

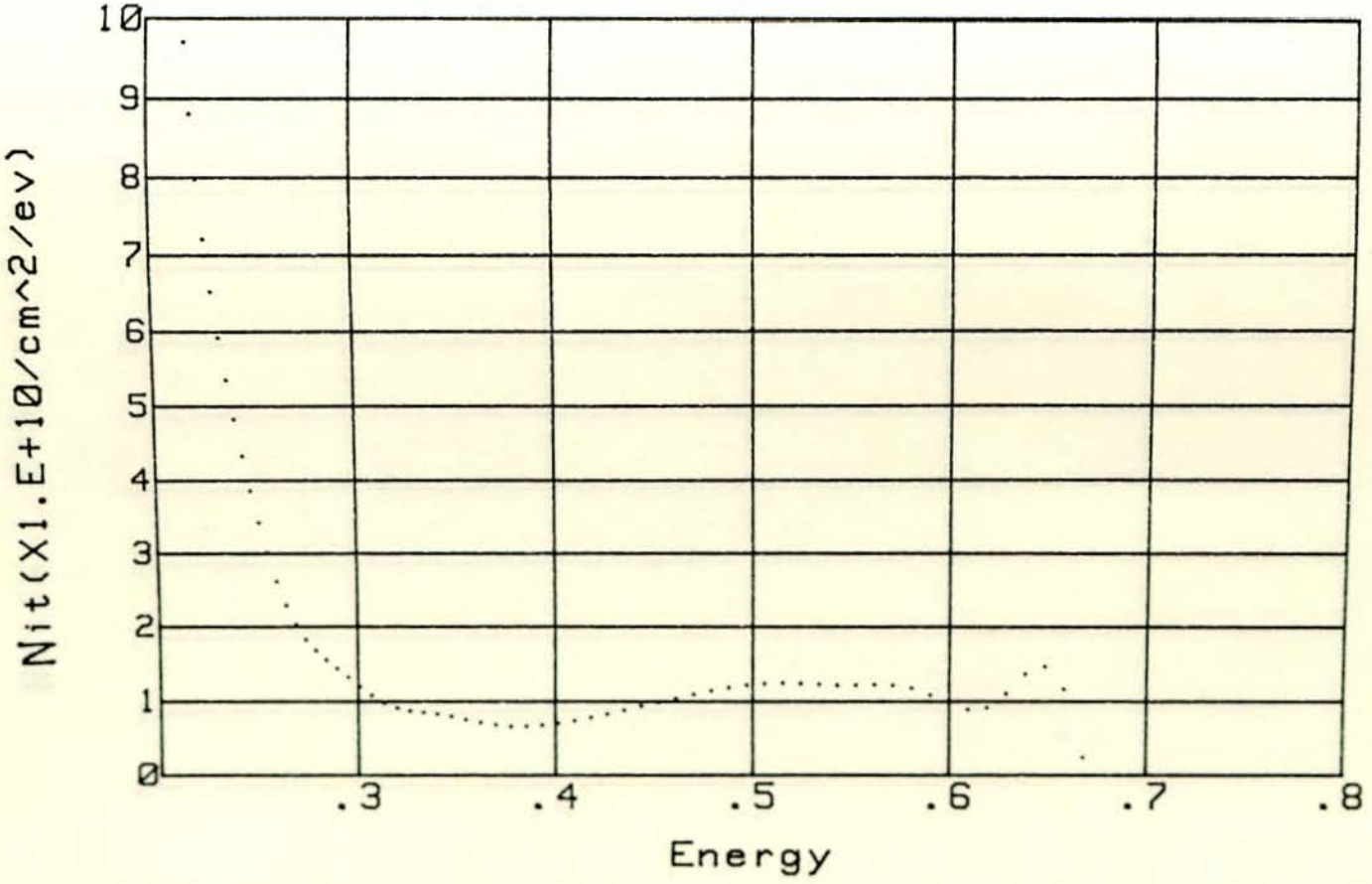

Fig.35 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 2

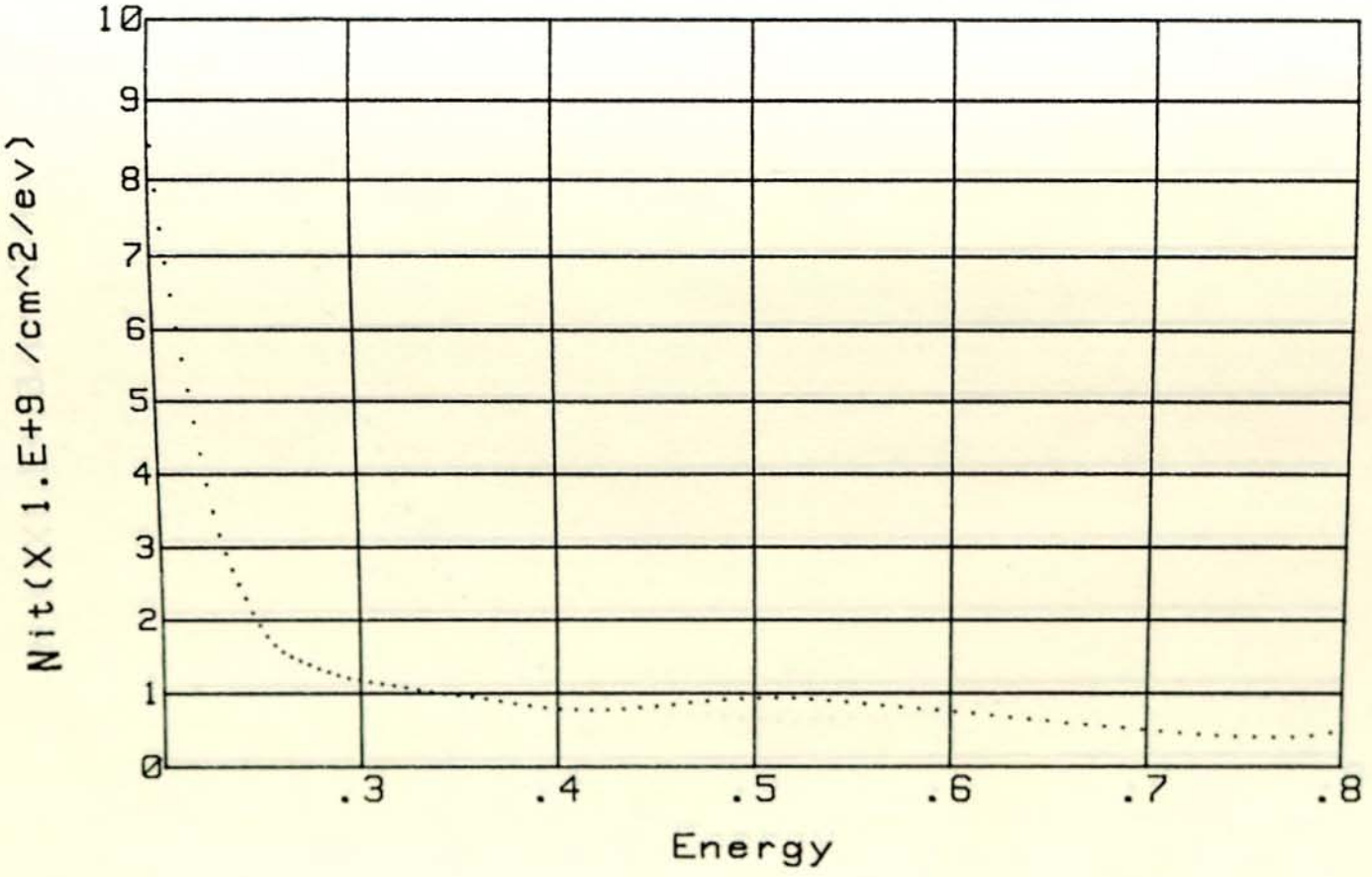

Fig.36 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 4

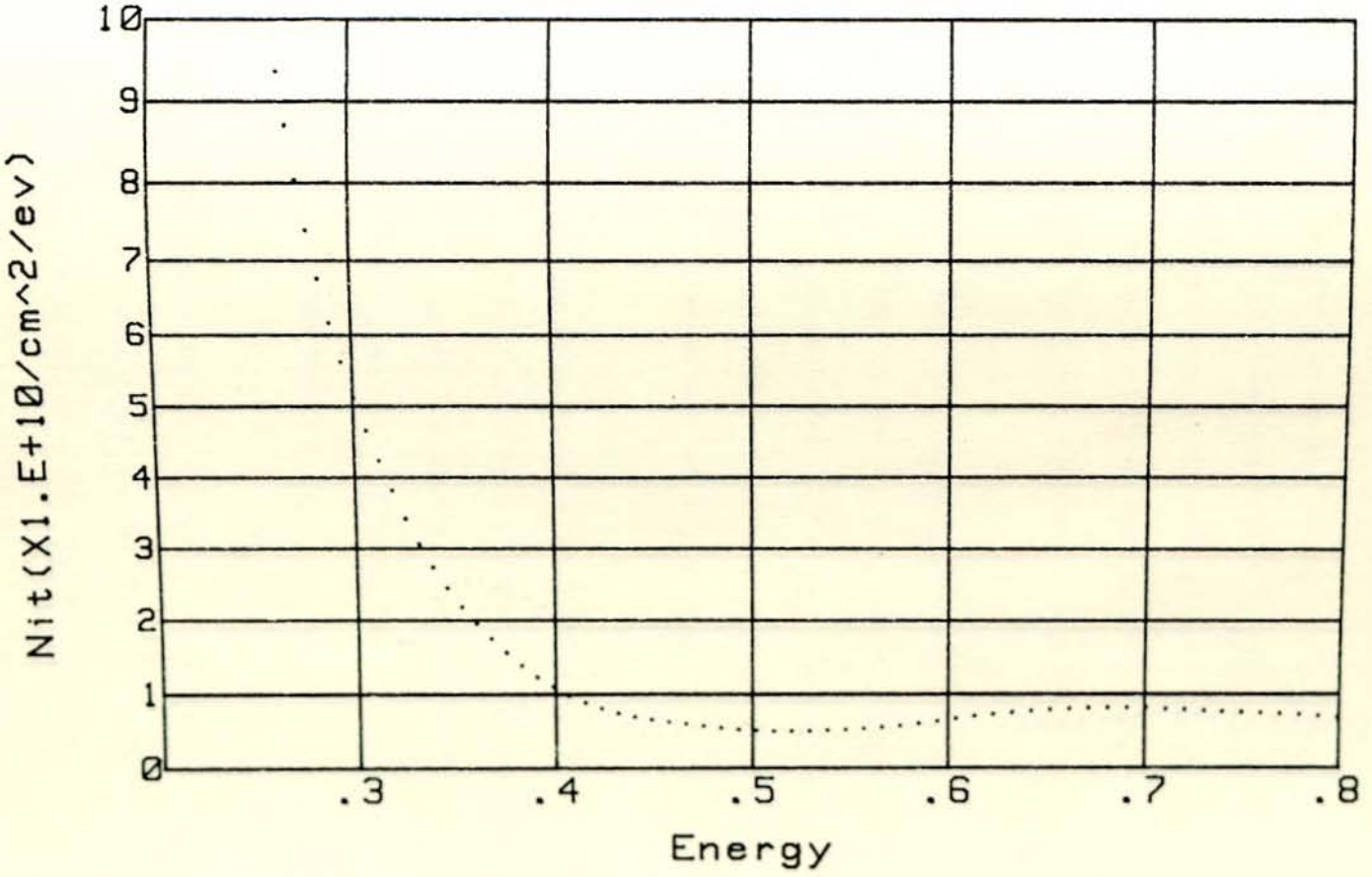

Fig.37 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 6

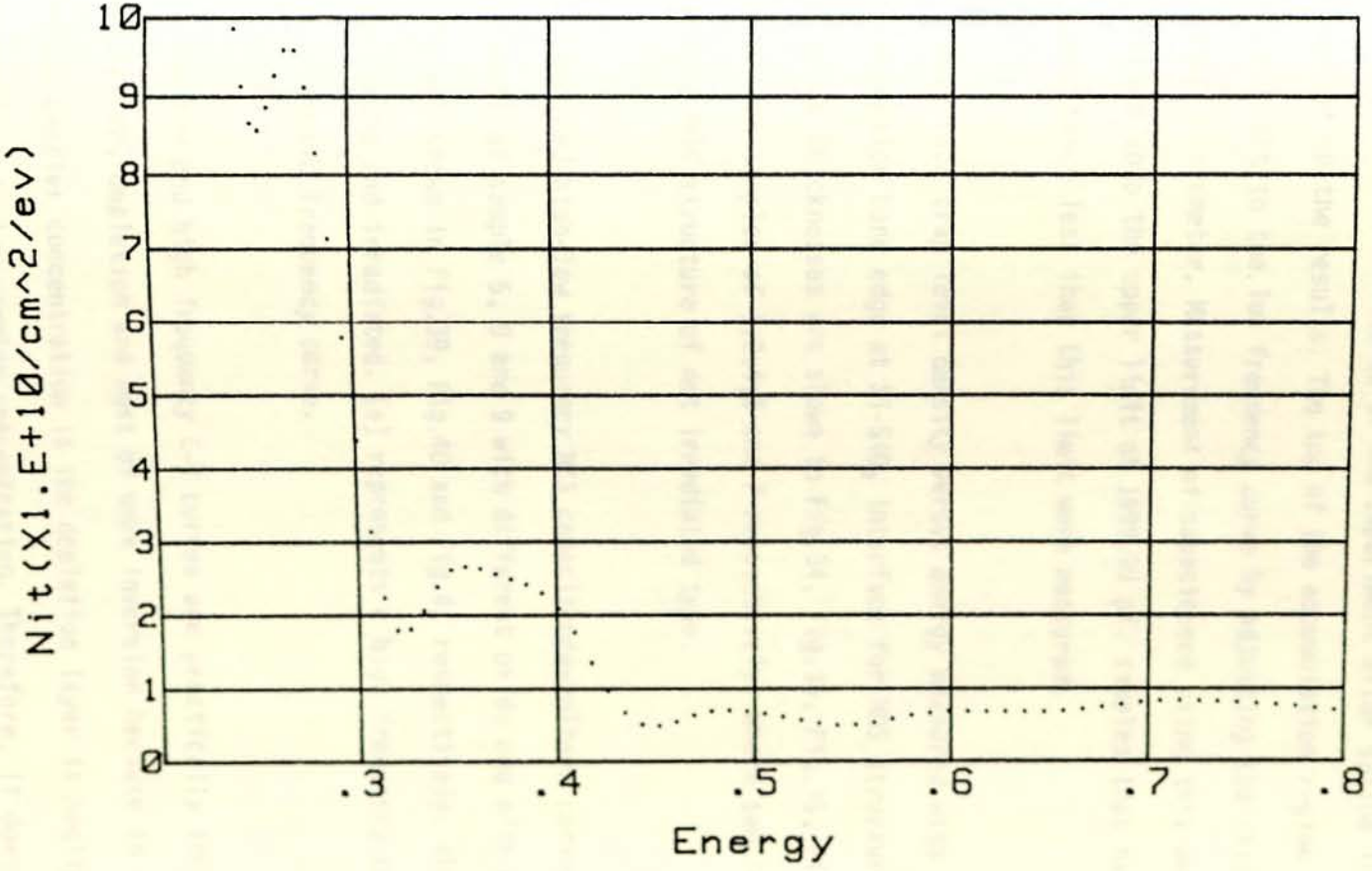

Fig.38 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 7

Where curve (a) is high frequency curve and curve (b) is quasistatic frequency curve. The combined high-low frequency MIS capacitance measurement was done at a quasistatic frequency with more accurate measurement but not at low frequency of measurement. Both high and quasistatic freqency curves are direct results of the experiment after spline interpolation was applied to the results. The top of the accumulation region of high frequency fit to the low frequency curve by adjusting the thickness of the oxide as a parameter. Measurement of capacitance using this method was restricted upto the upper limit of 1999.99 pf. samples that have the value of capacitance less than this limit were measured.

Interface trap level density versus energy measured with respect to the conduction band edge at $Si-SiO_2$ interface for MOS structures of different oxide thicknesses are shown in Fig.34, Fig.35, Fig.36, Fig.37 and Fig.38 for samples of 1,2,4,6 and 7 respectively. Where sample 2 is pyrogenic MOS structure of not irradiated type.

Combined high-low frequency MIS capacitance-voltage curves for MNOS structures of sample 5, 8 and 9 with different oxide and nitride thicknesses are shown in Fig.39, Fig.40 and Fig.41 respectively. Where sample 9 is pyrogenic and irradiated. (a) represents a high frequency curve and (b) is quasistatic frequency curve.

The low and high frequency C-V curves are practically identical in accumulation, depletion and most of weak inversion because in these regions, minority carrier concentration in the depletion layer is negligibly small compared to majority carrier concentration. Therefore, it does not matter where minority carriers respond to the ac voltage. The major difference

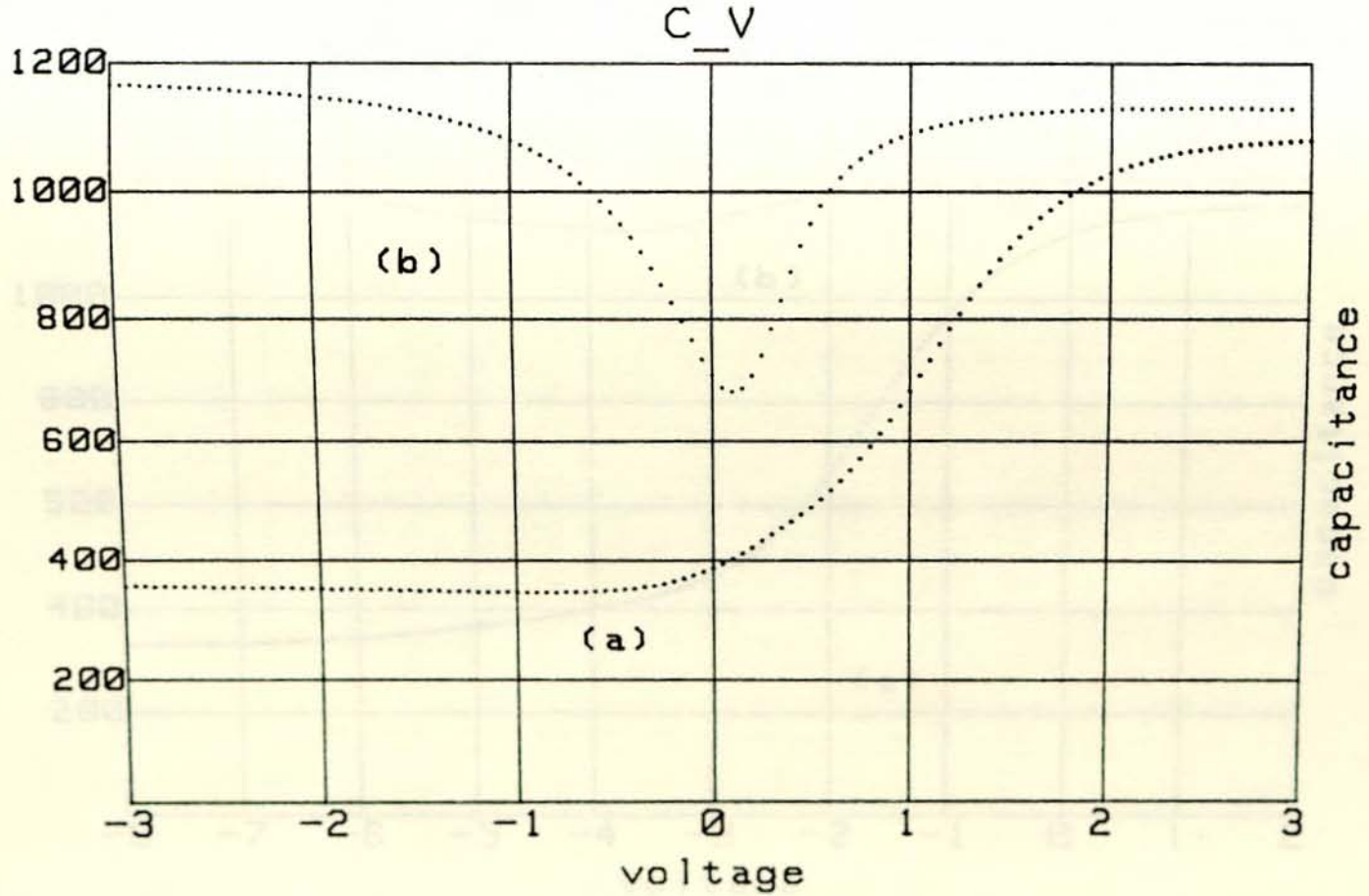

Fig.39 Combined High-Low Frequency MIS Capacitance-Voltage Curve
(a) High Frequency Curve (b) Low Frequency Curve

Sample 5

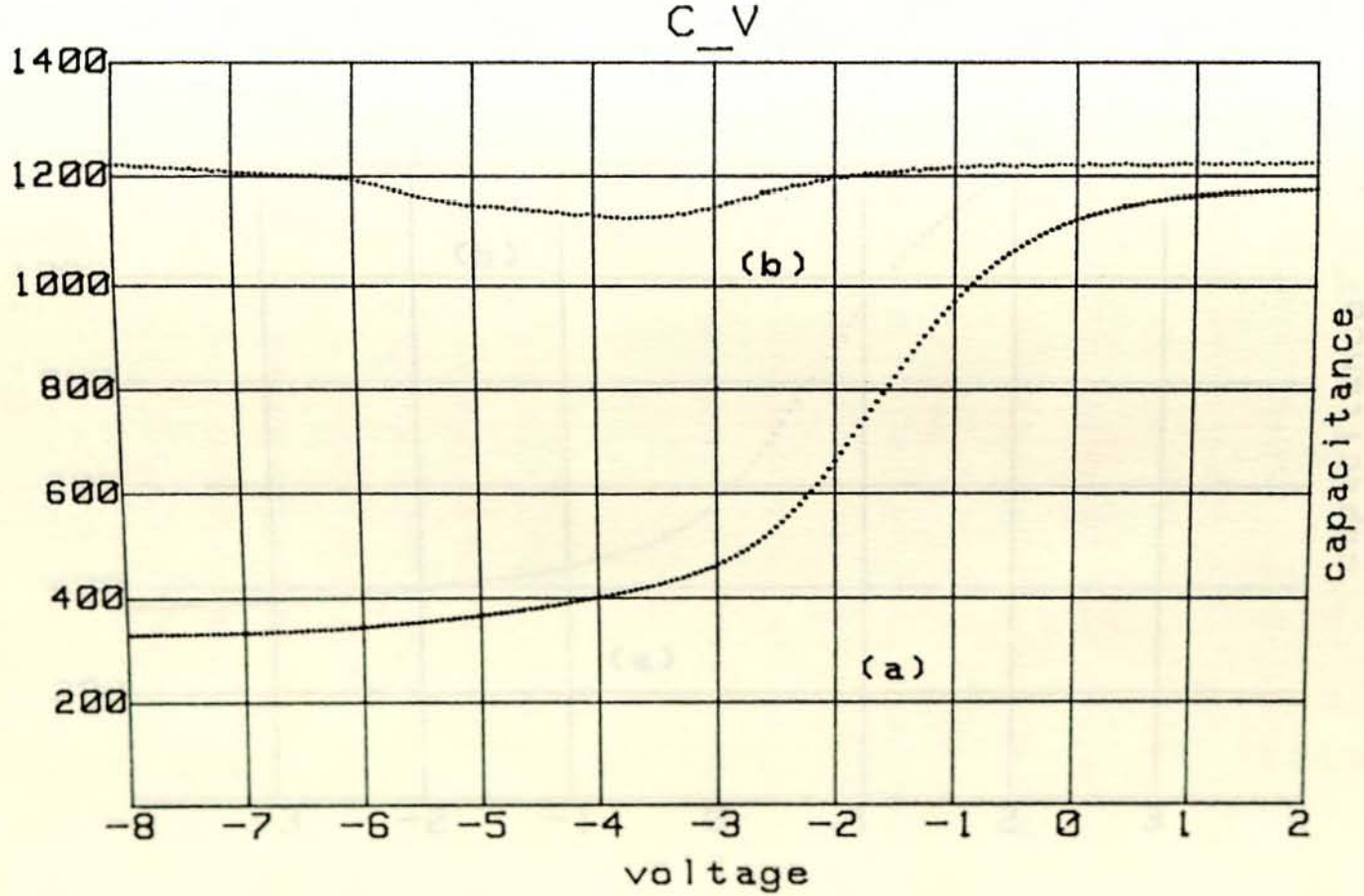

Fig.40 Combined High-Low Frequency MIS Capacitance-Voltage Curve
(a) High Frequency Curve (b) Low Frequency Curve

Sample 8

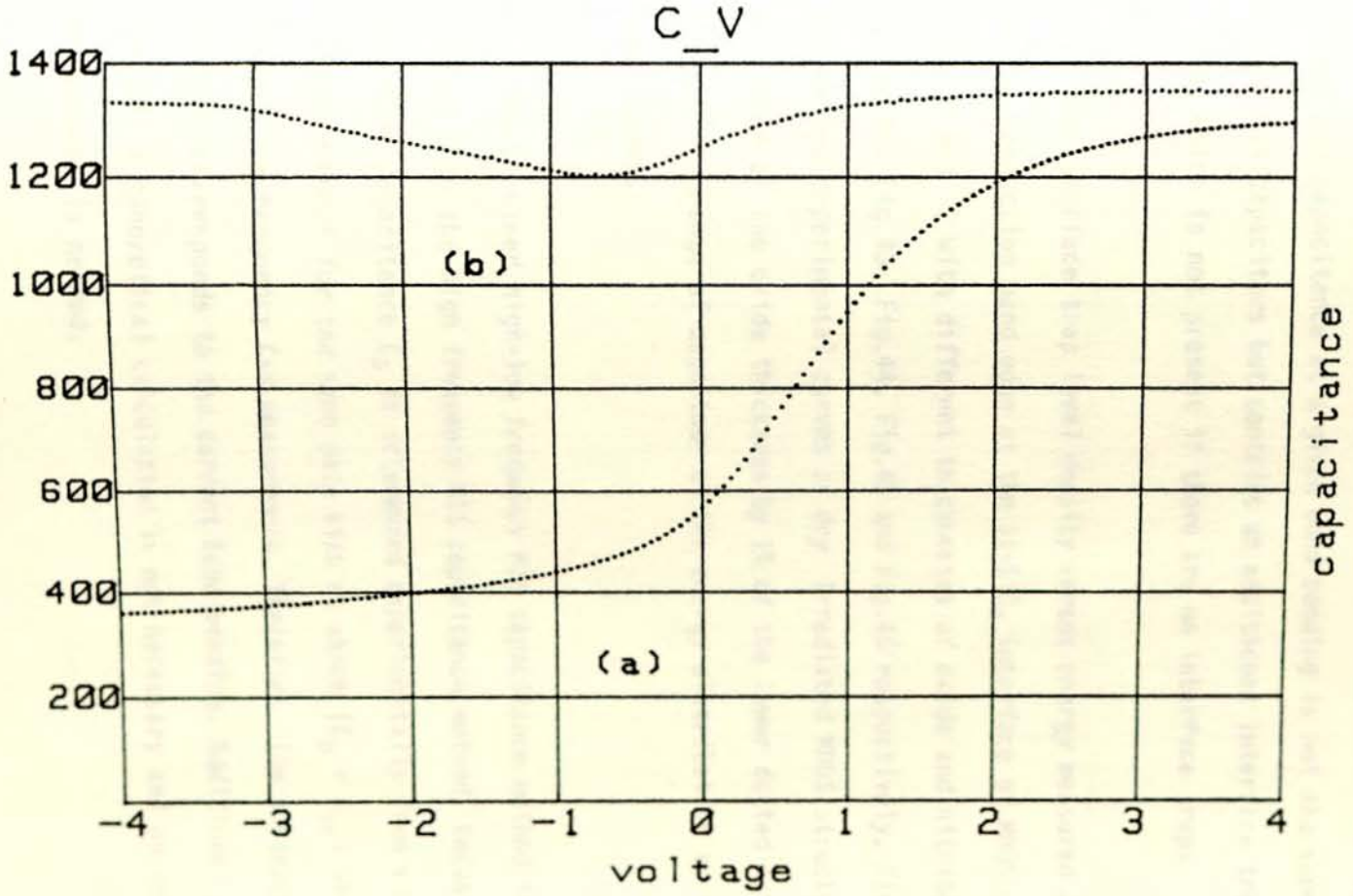

Fig.41 Combined High-Low Frequency MIS Capacitance-Voltage Curve
(a) High Frequency Curve (b) Low Frequency Curve
Sample 9

between low and high frequency C-V curves occurs in weak to strong inversion where minority carrier concentration in the depletion layer becomes comparable to and exceeds majority carrier concentration. Minority carrier effects in these regions are then important they cannot be neglected. Hence the capacitance at a given band bending is not the same in comparison of MIS capacitors but contains an additional interface trap capacitance, which is not present if there are no interface traps.

The interface trap level density versus energy measured with respect to the conduction band edge at the $Si-SiO_2$ interface of MNOS samples of 3,5,8,9 and 10 with different thicknesses of oxide and nitride are shown in Fig.42, Fig.43, Fig.44, Fig.45 and Fig.46 respectively. Fig.44 shows two dotted experimental curves of dry Irradiated MNOS structure of sample 8. Change of the oxide thickness by 1% of the lower dotted curve in Fig.44 results in change of magnitude of the energy distribution as shown in the upper curve.

The combined high-low frequency MIS capacitance method is more advantageous than the high frequency MIS capacitance method. Becuase the semiconductor capacitance C_D is determined experimentally from a high frequency C-V measurement for the same gate bias at which $(C_D + C_{it})$ was measured using a low frequency C-V measurement. Therefore, the subtracted C_D directly corresponds to the correct band bending. Additional advantages are that a theoretical calculation is not necessary and no doping profile measurement is needed.

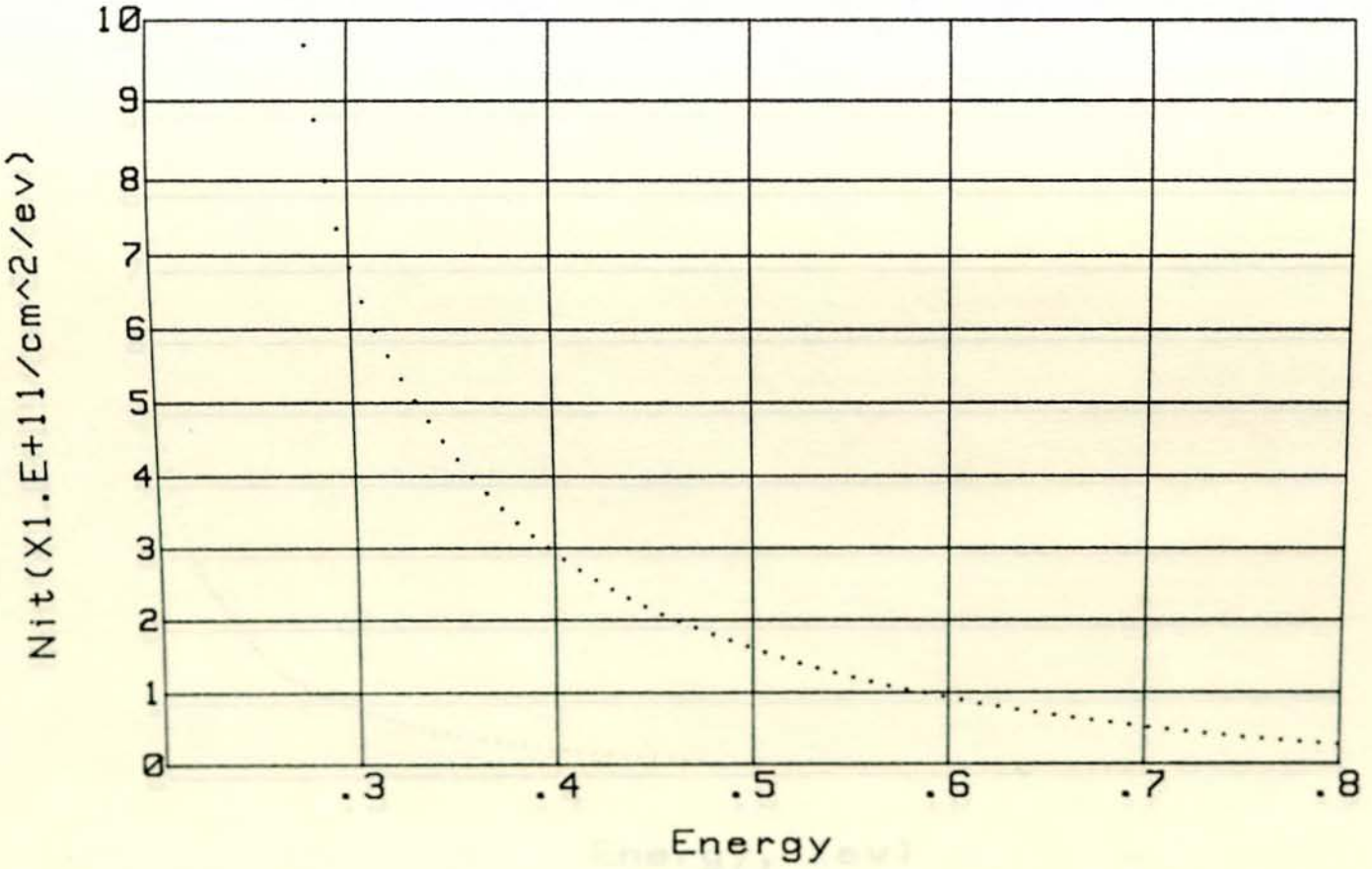

Fig.42 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 3

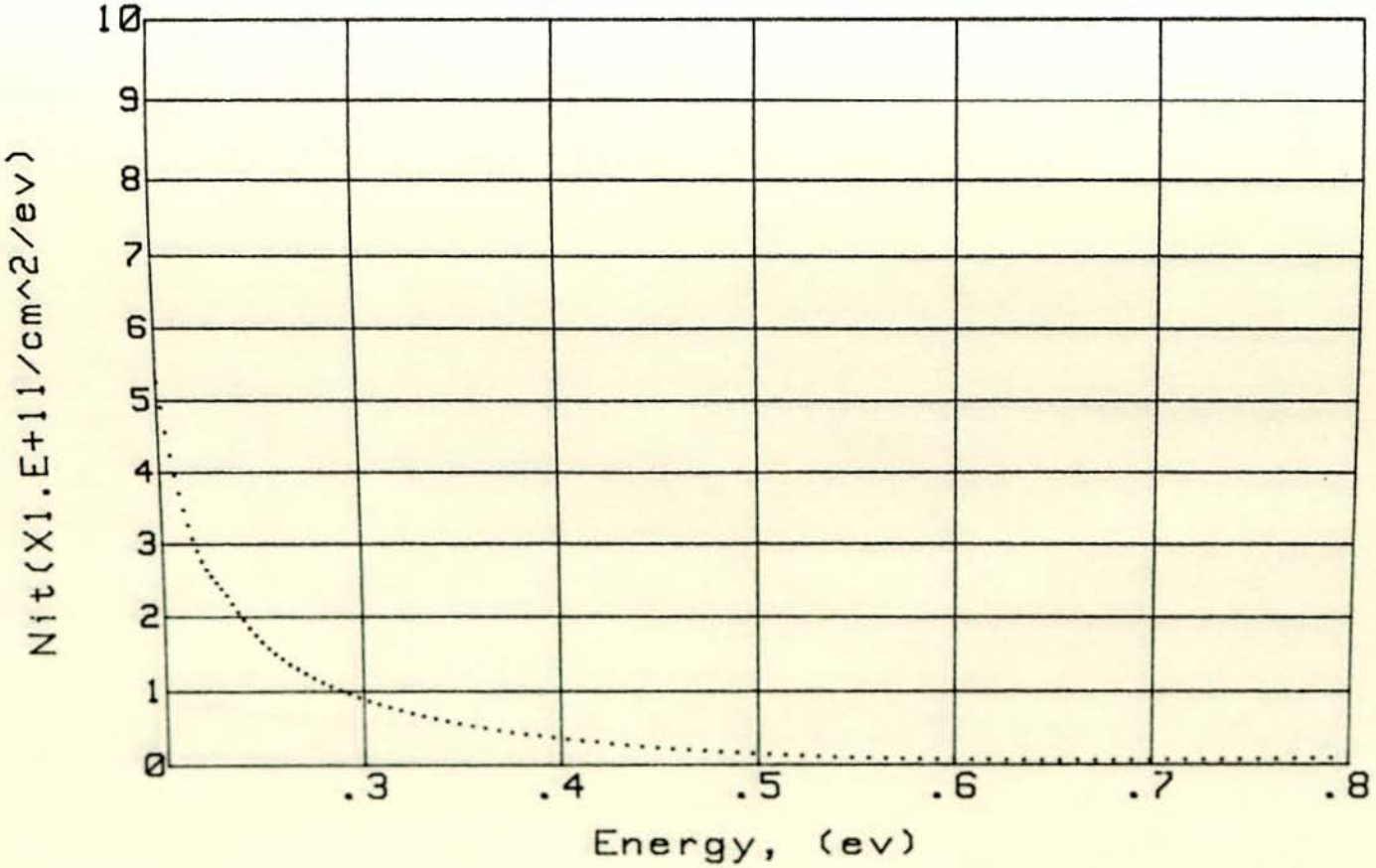

Fig.43 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 5

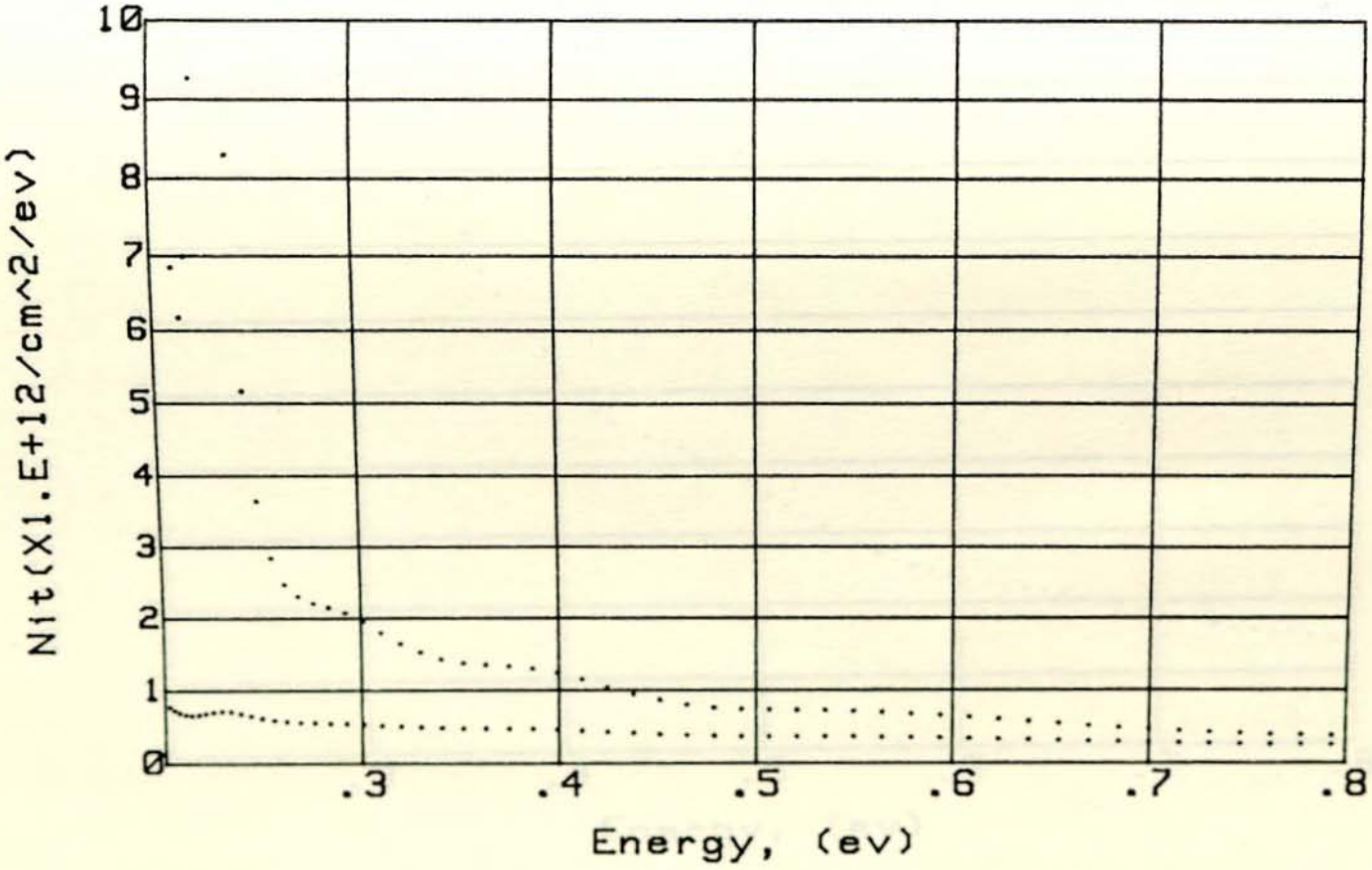

Fig.44 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 8

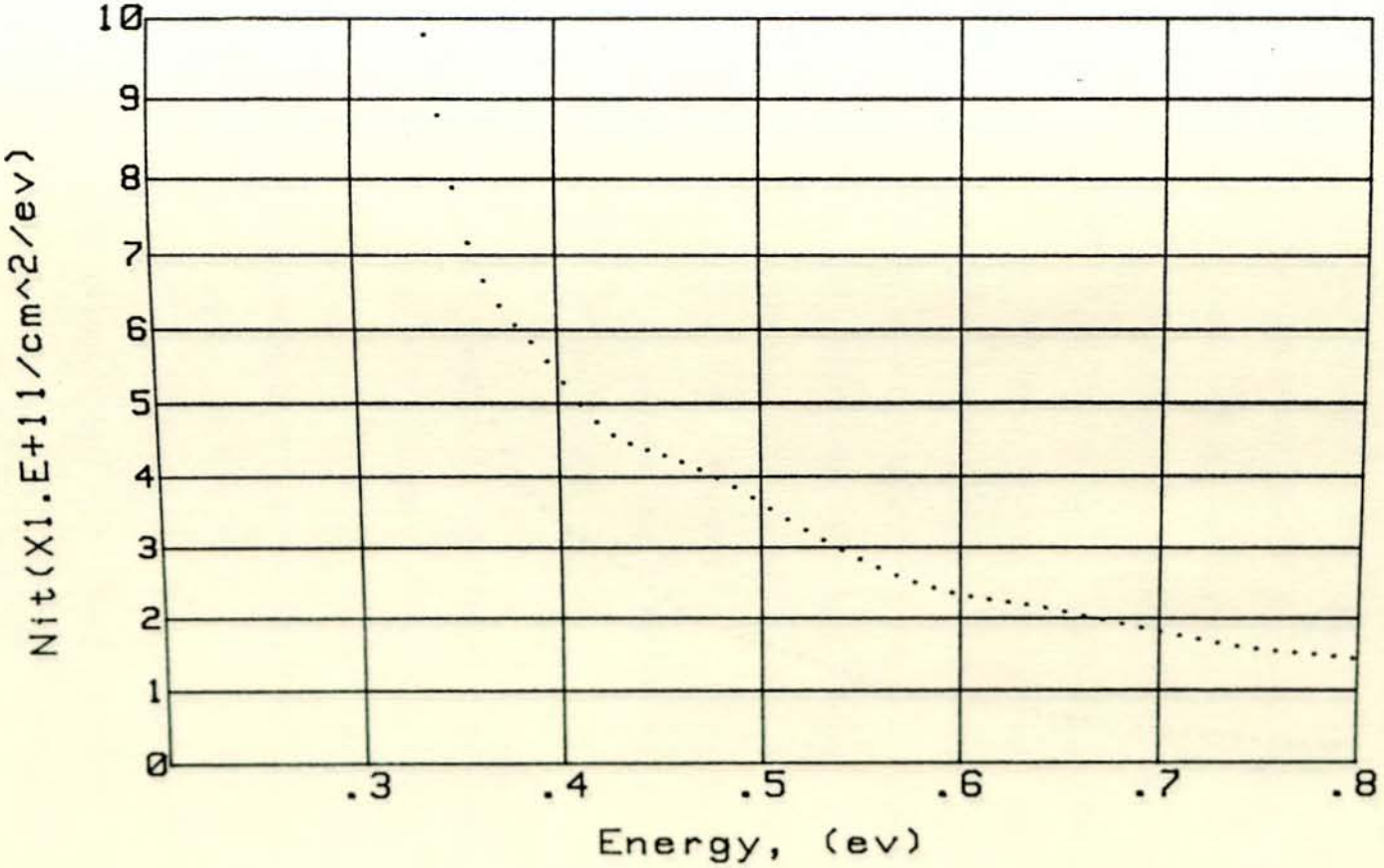

Fig.45 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 9

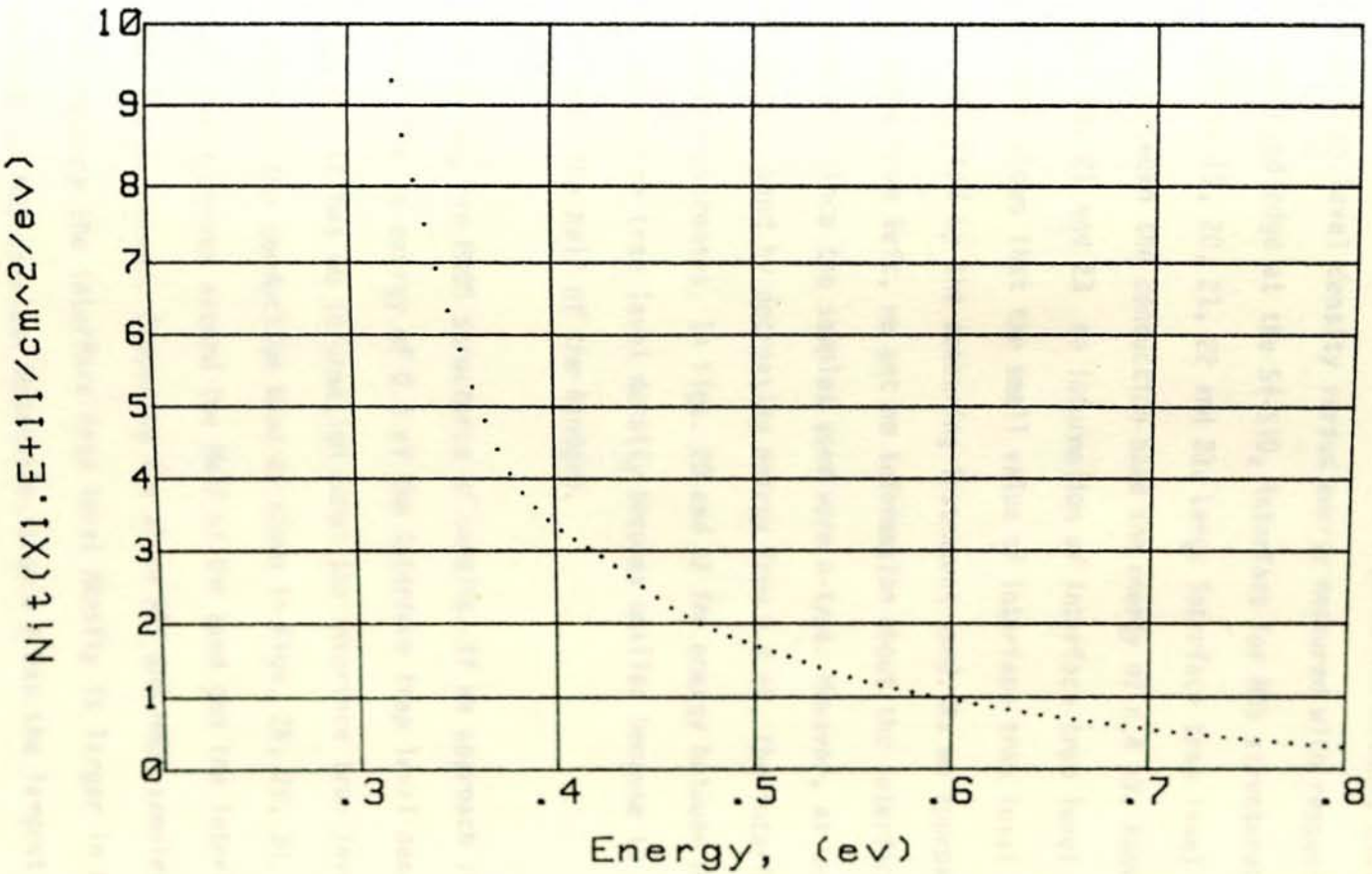

Fig.46 Interface trap level density Versus Energy Measured with respect to the Conduction band edge at the Si-SiO2 Interface Sample 10

7.3 Discussion of Results On Interface Charge Density Distribution

The total bandgap energy between the conduction band and the valence band of silicon at room temperature is 1.12 eV and the half of the bandgab is at 0.56 eV. Using high frequency MIS capacitance method, plots of the interface trap level density versus energy measured with respect to the conduction band edge at the $Si-SiO_2$ interface for MOS structures were shown in Figs.19, 20, 21, 22 and 23. Large interface trap level density was found between the conduction band and energy of o.4 eV. Above 0.4 eV for Figs. 19, 21 and 23 no information of interface trap level density exists. This shows that the small value of interface trap level density was not detected by the measuring instrument used. As we approach the valence band from left, we get no information about the interface trap level density since the samples used were n-type. However, as we approach the conduction band by decreasing energy from 0.4 eV, the interface trap level density increases. In Figs. 20 and 22 for energy between 0.4 eV and 0.5 eV, interface trap level density becomes smaller because it is a location near the half of the bandgap.

Similarly, for MNOS structures of samples, if we approach from the right hand side to energy of 0.3 eV the interface trap level density increases but it has no information about the interface trap level density at the edge of the conduction band as shown in Figs. 28, 29, 30, 31 and 32. In all of these curves around the half of the band gap the interface trap level density decreases. Comparing the above MOS and MNOS samples measured at high frequency the interface trap level density is larger in MNOS samples than in MOS samples. Meanwhile, sample 9 has the largest interface trap level density of all samples measured of the order greater than 10^{12}

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No.	SAMPLE	STRUCTURE AND TYPE	D_{ox} Å	D_{nt} Å	$C_{max(pf)}$	C_{min} (pf)	D_{OXE} Å	$N_D(cm^{-3})$ x 10^{15}	$N_{itf}(eVcm^2)^{-1}$	$N_{itm}(eVcm^2)^{-1}$
1	N8D-6	MOS,D	670	-	1996	386	690	1.5	1.7×10^{10}	1.2×10^{10}
2	N8P-18	MOS,P	620	-	2120	380	660	1.5	1.7×10^{10}	1.2×10^{10}
3	N8NP-19	MNOS,P	600	800	1350	350	650	1.2	9.7×10^{11}	1.3×10^{11}
4	N7D-9	MOS,D	690	-	1880	385	710	1.5	1.4×10^{9}	9.0×10^{8}
5	N7NP-10	MNOS,D	750	810	1090	353	815	1.2	1.1×10^{11}	1.0×10^{10}
6	r5-8	MOS,D	625	-	2200	380	665	1.5	7.4×10^{10}	5.2×10^{9}
7	N4D-13	MOS,D	400	-	4410	431	315	1.5	2.7×10^{10}	5.0×10^{9}
8	N8NP-8	MNOS,D*	660	850	1200	392	700	1.1	5.6×10^{11}	3.8×10^{11}
9	N8NP-12	MNOS,P*	600	800	1309	373	630	1.3	$> 10^{12}$	2.9×10^{11}
10	r7-14	MNOS,D	1000	800	962	342	1010	1.3	$> 10^{12}$	1.3×10^{11}

* = Irradiated samples by 10^7 rad D = dry and P = pyrogenic

Table 2. Results of measurements for MOS and MNOS samples

in flatband and in the order of 10^{11} in half of the bandgap. Because sample 9 is Irradiated MNOS structure of pyrogenic type with radiation of 10^7 rad.

Using combined high-low frequency MIS capacitance method the interface trap level density versus energy measured with respect to the conduction band edge at Si-SiO_2 interface for MOS structures are shown in Figs. 34, 35, 36, 37 and 38. As we approach from right to left, energy decreases but the interface trap level density increases. Sample 4 has the smallest interface trap level density of 1.4×10^9 at flatband condition and 9×10^8 at half of the bandgap. It is dry MOS structure of not irradiated type. Similar to MOS structures, energy distribution of the interface trap level density of MNOS structures is shown in Figs.42, 43, 44, 45 and 46. Samples 3, 9 and 10 have no information of the interface trap level density between conduction band and energy of 0.3 eV. Comparing the MOS and MNOS samples measured at combined high-low frequency similar to high frequency method, the largest interface trap level density was obtained for sample 9 of pyrogenic, Irradiated MNOS structure as discussed in the above high frequency method. The interface trap level density is smaller for sample 4 of MOS structure than MNOS structure which was found in the order of 10^9 in the flatband condition and in the order of 10^8 in the half of the bandgap.

Table 2 shows the experimental results obtained after thickness of the oxide and doping concentration of the sample were adjusted as a parameter. D_{ox} and D_{nt} are initial oxide and nitride thicknesses of the samples obtained from the factory. Similarly D_{OXE} and N_D are the oxide thickness and the doping concentration of the samples respectively after

adjustment was made. From the C-V measurement of the experiment using high frequency MIS capacitance and combined high-low MIS capacitance methods the maximum capacitances C_{max} and the minimum capacitance C_{min} were obtained. The interface trap level density at the flatband condition N_{itf} and at midgap N_{itm} were found and are shown in Table 2.

Comparing both methods of experimental measurements from the obtained results, high frequency MIS capacitance method gave more information about specific structure of energy but the combined high-low frequency method did not give information of the energy structure since its curve is smooth. Small values of interface trap level densities were not possible to be detected by high frequency MIS capacitance method which need adjustments of the doping concentration and the oxide thickness. However, this method detected large values of interface trap level densities. Using combined high-low frequency MIS capacitance method small interface trap level densities were measured by adjusting the oxide thickness. This method is very sensitive to the presence of small interface trap level density. For instance in Fig.44 changing the oxide thickness by 1% of the lower dotted curve results a change in the interface trap level density as shown in the upper dotted curve. Therefore, one method of measurement is not good enough to be used separately from the other method. Both methods should be used together. In addition to these methods the conductance MIS capacitance method was proposed to be done in this work but due to inadequate range of frequency from 10KHZ upto 10MHZ of the multifrequency LCR meter the experimental result was not presented. Dry and pyrogenic samples were compared, the interface trap level density for pyrogenic sample 9 was found in the order greater than 10^{12} and it is larger than the dry samples in which both methods gave similar results. Similarly, irradiated samples were obtained with larger interface trap level density than not-irradiated samples.

CONCLUSION

1. Real time computer program was constructed using numerical integration and spline interpolation methods to determine the energy distribution of interface charge density for MOS and MNOS structures at the Si-SiO_2 interface.

2. Interface charge density, N_{it} from the results of measurements and theoretical curve of the high frequency capacitance method as a function of bias was calculated using the new method of formula without including other parameters.

3. Measurement on different types of samples was done using the high frequency MIS capacitance method and combined high-low frequency MIS capacitance method and for each sample the interface charge density distribution was obtained. The obtained interface charge density was reached upto the order of 10^9 charges per eV cm^2 using the very sensitive experimental method with good accuracy of measurement.

4. Comparison of the high frequency MIS capacitance method with the combined high-low frequency method shows that one method is not good enough to be used separately from the other method. Both methods should be used together.

5. From the measured results of MOS and MNOS structures of pyrogenic and dry oxide of Irradiated and not Irradiated samples, the inteface charge density in MOS structure of dry not irradiated sample was found the smallest in the order of 1.4×10^9 at flatband condition and 9×10^8 at half of the band gap. Similarly the largest interface charge density was obtained for irradiated, pyrogenic MNOS samples in the order of 10^{12} in flatband condition and in the order of 10^{11} in the half of the band gap.

APPENDIX A

```
10  !        "HIGH FREQUENCY MIS CAPACITANCE METHOD"
11  !
20      OPTION BASE 1
30      DIM Integ(11:44)
40      DIM Ctot(0:44),Bp(44),Vth(44)
50      DIM Cth(500),Psi(500),Cex(500),Vex(500),Vtho(500),Bpo(500),Dth(500)
60      DIM Psio(500),Vexo(500),Dex(500),μ(500)
70      DIM Cy(500),Xy(500),Dit(500)
80          Myg=0
90          Cm=1350
100         Left=-5
110 REMOTE 717
120 CLEAR 717
130 OUTPUT 717;"A2B3C1M1"
140 OUTPUT 717;"BI";Left-.5;"E00V"
150 OUTPUT 717;"F15"
160 OUTPUT 717;"E"
170 PRINT "Close the light!"
180     PAUSE
190         Right=4
200         A=1.E-6
210         Aerr=1.E-100
220         Rerr=.1
230 !
240       Qe=1.60218E-19                    !Coul
250       Kb=1.38066E-23                    !J/K
260       Eps=11.9*8.85418E-14              !F/Cm  1.05E-12
270       Epo=3.9*8.85418E-14               !F/Cm  3.45E-13
280       Epn=7.5*8.85418E-14               !F/Cm
290    T=295                                !K
300    Dox=6.950E-6                         !Cm
310    Dnt=8.5E-6                           !Cm
320    Ni=1.45E+10                          !Cm^-3
330    Nd=1.20E+15                          !Cm^-3
340    !
350    Cox=Epo/Dox
360     Cnt=Epn/Dnt                         !F/Cm^2
370     Con=Cox*Cnt/(Cox+Cnt)               !F/Cm^2
380    β=Qe/(Kb*T)                          !β=38.6815 1/V
390    Ld=SQR(Eps/(Qe*Nd*β))                !Cm
400    Ao=SQR(2)*Eps/(β*Ld)                 !Coul/Cm^2
410    Co=(Ni/Nd)^2
420    Cfb=Eps/Ld
430    ! Ctfb=Cox*Cfb/(Cox+Cfb)*.04*1.E+12
440     Cfbtot=Con*Cfb/(Con+Cfb)*.04*1.E+12
450    Fai=LOG(Nd/Ni)/β
460    !
470           FOR I=11 TO 44
480             B=1.E-3+(I-11)
490            CALL Cadre(A,B,Aerr,Rerr,Err,Flg,Cadre)
500            PRINT I,DROUND(Cadre,3),Flg
510             Integ(I)=Cadre
520           NEXT I
530    !
```

```
540             CALL Graph(Cm,Left,Right,Myg)
550       PEN 2
560   !
570             Ctot(0)=10000
580       FOR I=1 TO 44
590          B=1.E-3+(I-11)
600          Term3=EXP(-B)+B-1
610          Term4=EXP(B)-B-1
620          Fo1=Term3+Co*Term4
630          Qs=SGN(B)*Ao*SQR(Fo1)
640          Vi=Qs/Con
650          V=Vi+B/β
660          Vth(I)=-V
670       IF I>10 THEN
680          Delta=FNFo(B)*(Integ(I)-1)/(EXP(B)-1)
690          Result=1/(1+Delta)
700          Cs=Cfb*(1-EXP(-B)+(Ni/Nd)^2*((EXP(B)-1)*Delta*Result+1))/FNFo(B)
710       ELSE
720          Cs=ABS(Cfb*(1-EXP(-B))/FNFo(B))
730       END IF
740          Ctot(I)=Cs*Con/(Cs+Con)*1.E+12*.04
750          IF Ctot(I)>Ctot(I-1) THEN Ctot(I)=Ctot(I-1)-.01
760          Bp(I)=-B
770          PLOT Vth(I),Ctot(I)
780       NEXT I
790       PENUP
800   !
810   Mode=1
820   T=.05
830          CALL Plot_c_v(Left,Right,Cm,Xy(*),Cy(*),Vshift,Imax,Cfbtot,Mode,T,Myg)
840       INPUT "Plotter?,  1",Myg
850       IF Myg=1 THEN 540
860       FOR I=1 TO Imax
870       Xy(I)=Xy(I)-Vshift
880       NEXT I
890          PAUSE
900   !
910   Eps=1.E-4
920       Narg=200
930       N=44
940       ALLOCATE X(N),Y(N),Domain(Narg),Deriv(Narg),Func(Narg)
950       FOR I=1 TO N
960         X(I)=Ctot(N+1-I)
970         Y(I)=Bp(N+1-I)
980       NEXT I
990       FOR I=1 TO Narg
1000        Domain(I)=380+(I-1)*(1150-380)/(Narg-1)
1010      NEXT I
1020      CALL Spline(N,Narg,X(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
1030      FOR I=1 TO Narg
1040        Cth(I)=Domain(I)
1050        Psi(I)=Func(I)
1060      NEXT I
1070      DEALLOCATE X(*),Y(*),Domain(*),Deriv(*),Func(*)
1080      !
1090      N=Imax
1100      ALLOCATE X(N),Y(N),Domain(Narg),Deriv(Narg),Func(Narg)
1110      Q=1
1120      X(1)=Cy(1)
1130      Y(1)=Xy(1)
```

```
1140   FOR I=2 TO N-1
1150   Q=Q+1
1160     X(Q)=Cy(I)
1170     Y(Q)=Xy(I)
1180     IF X(Q)<=X(Q-1) THEN Q=Q-1
1190   NEXT I
1200   N=Q
1210   FOR I=1 TO Narg
1220     Domain(I)=380+(I-1)*(1150-380)/(Narg-1)
1230   NEXT I
1240   CALL Spline(N,Narg,X(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
1250   FOR I=1 TO Narg
1260     Cex(I)=Domain(I)
1270     Vex(I)=Func(I)
1280   NEXT I
1290   DEALLOCATE X(*),Y(*),Domain(*),Deriv(*),Func(*)
1300   !
1310   INPUT "Ploter,   1",Myg
1320   IF Myg=1 THEN
1330   PLOTTER IS 705,"HP6L"
1340   OUTPUT 705;"VS7.5;"
1350   ELSE
1360    OUTPUT 2 USING "#,K";CHR$(255)&"K"
1370   GINIT
1380   END IF
1390   DEG
1400   VIEWPORT 10,60,30,90.001
1410   WINDOW -20,5,0,2000
1420   PEN 1
1430   GRID 5,500
1440   CLIP OFF
1450   LDIR 90
1460   LORG 6
1470   MOVE 5.9,2000
1480   CSIZE 3.5
1490   PEN 5
1500   LABEL "Capacitance"
1510   LDIR 0
1520   LORG 6
1530   MOVE -8,0
1540   LABEL "Potential"
1550   MOVE 22,0
1560   LABEL "Voltage"
1570   PEN 3
1580   MOVE 7,-400
1590   CSIZE 3.7
1600   LABEL "Fig.   A Theoretical Capacitance versus Potential and"
1610   MOVE 7,-800
1620   LABEL "Experimental Capacitance versus Voltage"
1630   CLIP ON
1640   PEN 2
1650   FOR I=1 TO Narg
1660   PLOT Psi(I),Cth(I)
1670   NEXT I
1680   !
1690   PEN 1
1700   VIEWPORT 68,118,30,90.001
1710   WINDOW -.8,.8,0,2000
1720   GRID .2,500
1730   PEN 4
```

```
1740  FOR I=1 TO Narg
1750  PLOT Vex(I),Cex(I)
1760  NEXT I
1770  PENUP
1780  PAUSE
1790  IF Myg=1 OR Myg=2 THEN 1310
1800  !
1810   N=44
1820   ALLOCATE X(N),Y(N),Domain(Narg),Deriv(Narg),Func(Narg)
1830   FOR I=1 TO N
1840     X(I)=Bp(N+1-I)
1850     Y(I)=Vth(N+1-I)
1860   NEXT I
1870   FOR I=1 TO Narg
1880     Domain(I)=-15.0+(I-1)*(3.7+15.0)/(Narg-1)
1890   NEXT I
1900   CALL Spline(N,Narg,X(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
1910   FOR I=1 TO Narg
1920     Bpo(I)=Domain(I)
1930     Vtho(I)=Func(I)
1940     Dth(I)=Deriv(I)
1950   NEXT I
1960   DEALLOCATE X(*),Y(*),Domain(*),Deriv(*),Func(*)
1970  !
1980  INPUT "Plotter,   1",Myg
1990  IF Myg=1 THEN
2000  PLOTTER IS 705,"HPGL"
2010  OUTPUT 705;"VS7.5;"
2020  ELSE
2030   OUTPUT 2 USING "#,K";CHR$(255)&"K"
2040   GINIT
2050   END IF
2060   VIEWPORT 20,110,25,85
2070   WINDOW -1,1,-20,5
2080   PEN 1
2090   GRID .2,5
2100   PEN 6
2110  CSIZE 3.25
2120  CLIP OFF
2130  LORG 6
2140  FOR I=-.8 TO 1 STEP .2
2150  MOVE I,-20
2160  LABEL PROUND(I,-1)
2170  NEXT I
2180  CSIZE 3
2190  LORG 8
2200  FOR I=-20 TO 5 STEP 5
2210  MOVE -1,I
2220  LABEL USING "#,K";I
2230  NEXT I
2240  LORG 4
2250  PEN 5
2260  CSIZE 4
2270  MOVE 0,5.4
2280  LABEL "Psi_V"
2290  DEG
2300  LDIR 90
2310  CSIZE 3.5
2320  MOVE 1.1,-8.5
2330  LABEL "Psi"
```

```
2340  LORG 6
2350  LDIR 0
2360  MOVE 0,-22
2370  LABEL "voltage"
2380  PEN 3
2390  CSIZE 3.25
2400  MOVE 0,-25
2410  LABEL "Fig.   Surface Potential Versus Applied Voltage"
2420  MOVE 0,-27
2430  LABEL "(a) Theoretical Curve  (b) Experimental Curve"
2440  CSIZE 3
2450  MOVE -.3,-12
2460  LABEL "(a)"
2470  MOVE -.5,-3
2480  LABEL "(b)"
2490   !
2500   Eps=1.E-6
2510  CLIP ON
2520   FOR I=1 TO Narg
2530   PEN 2
2540   PLOT Vtho(I),Bpo(I)
2550   NEXT I
2560   PENUP
2570  !
2580   N=Narg
2590   ALLOCATE X(N),Y(N),Domain(Narg),Deriv(Narg),Func(Narg)
2600   FOR I=1 TO N
2610     X(I)=Psi(I)
2620     Y(I)=Vex(I)
2630   NEXT I
2640   FOR I=1 TO Narg
2650     Domain(I)=-15.0+(I-1)*(3.7+15.0)/(Narg-1)
2660   NEXT I
2670   CALL Spline(N,Narg,X(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
2680   FOR I=1 TO Narg
2690     Psio(I)=Domain(I)
2700     Vexo(I)=Func(I)
2710     Dex(I)=Deriv(I)
2720   NEXT I
2730   DEALLOCATE X(*),Y(*),Domain(*),Deriv(*),Func(*)
2740   !
2750   PEN 4
2760   FOR I=1 TO Narg
2770   PLOT Vexo(I),Psio(I)
2780   NEXT I
2790   PENUP
2800  !
2810  PAUSE
2820  IF Myg=1 OR Myg=2 THEN 1980
2830        New=1.E+11
2840   INPUT "Plotter,  1",Myg
2850   IF Myg=1 THEN
2860   PLOTTER IS 705,"HPGL"
2870   OUTPUT 705;"VS7.5;"
2880     ELSE
2890     GINIT
2900     END IF
2910        VIEWPORT 20,110,25,85
2920        WINDOW .2,.8,0,10
2930        PEN 1
```

```
2940        GRID .1,1
2950        PEN 6
2960        CLIP OFF
2970        LORG 6
2980        CSIZE 3
2990        FOR I=.3 TO .8 STEP .1
3000        MOVE I,0
3010        LABEL I
3020        NEXT I
3030        LORG 8
3040        FOR I=0 TO 10 STEP 1
3050        MOVE .2,I
3060        LABEL USING "#,K";I
3070        NEXT I
3080        LORG 4
3090        DEG
3100        LDIR 90
3110        PEN 5
3120        CSIZE 3.5
3130        MOVE .18,5
3140        LABEL "Nit(x1.E+11/cm^2/ev)"
3150        LDIR 0
3160        LORG 6
3170        MOVE .5,-.50
3180        LABEL "Energy,(ev)"
3190        PEN 3
3200        CSIZE 3.25
3210        MOVE .5,-1.5
3220      LABEL "Fig.   Interface trap level density Versus Energy Measured with"
3230      MOVE .5,-2.2
3240      LABEL "respect to the Conduction band edge at the Si-SiO2 Interface"
3250    !
3260    CLIP ON
3270    PEN 2
3280   FOR I=1 TO Narg
3290    Dit(I)=Con*β*(Dex(I)-Dth(I))/Qe
3300    IF Dit(I)<0 THEN Dit(I)=0
3310    μ(I)=.56-Fai-Psio(I)/β
3320    PLOT μ(I),Dit(I)/New
3330    PENUP
3340   NEXT I
3350   IF Myg=1 OR Myg=2 THEN 2840
3360    !
3370 END !

3380 SUB Cadre(A,B,Aerr,Rerr,Err,Flg,Cadre)
3390 !       Subprogram for numerical integration
3400 !       Lines from 3380 to 6620
6620 SUBEND
6630  DEF FNF(X)
6640 F:    Num=EXP(X)-EXP(-X)-2*X
6650       F=Num/FNFo(X)^3
6660       RETURN F
6670       FNEND
6680  DEF FNFo(X)
6690       Nd=1.20E+15
6700       Ni=1.45E+10
6710       Ub=LOG(Ni/Nd)
6720       Term1=EXP(-X)+X-1
6730       Term2=EXP(X)-X-1
6740       F=Ub*(Term1+EXP(2*Ub)*Term2)
```

```
6750        Fo=SQR(Fo)
6760        RETURN Fo
6770        FNEND
6780  !
6790        SUB Graph(Cm,Left,Right,Myg)
6800        IF Myg=1 THEN
6810     PLOTTER IS 705,"HPGL"
6820     OUTPUT 705;"VS7.5;"
6830     ELSE
6840     GINIT
6850     OUTPUT 2 USING "#,K";CHR$(255)&"K"
6860     PLOTTER IS CRT,"INTERNAL"
6870     END IF
6880    VIEWPORT 20,110,25,85
6890 WINDOW Left,Right,0,Cm+.001
6900 GRID 1,150
6910  CSIZE 3.25
6920  CLIP OFF
6930  PEN 6
6940  LORG 6
6950  FOR I=Left TO Right STEP 1
6960  MOVE I,0
6970  LABEL USING "#,K";I
6980  NEXT I
6990  CSIZE 3
7000  LORG 8
7010  FOR I=150 TO Cm STEP 150
7020  MOVE Left,I
7030  LABEL USING "#,K";I
7040  NEXT I
7050  PEN 5
7060  CSIZE 3.5
7070  LORG 5
7080  MOVE (Left+Right)/2,Cm+Cm/20
7090  LABEL "C_V"
7100  DEG
7110  LDIR 90
7120  CSIZE 3.5
7130  MOVE Right+.2,Cm-Cm/3
7140  LABEL "capacitance"
7150  LORG 4
7160  LDIR 0
7170  MOVE (Left+Right)/2,-Cm/8
7180  LABEL "voltage"
7190  PEN 3
7200  CSIZE 3.25
7210  MOVE (Left+Right)/2,-Cm/4
7220  LABEL "Fig.   High-Frequency MIS Capacitance-Voltage Curves"
7230  MOVE (Left+Right)/2,-Cm/3
7240  LABEL "(a) Theoretical Curve   (b) Experimental Curve"
7250  CSIZE 3
7260  MOVE -.8,200
7270  LABEL "(a)"
7280  MOVE -.8,600
7290  LABEL "(b)"
7300  CLIP ON
7310  SUBEND
7320  !
7330          SUB Plot_c_v(Left,Right,Cm,Xy(*),Cy(*),Vshift,Imax,Cfbtot,Mode,T,M
yg)
7340          IF Myg=1 THEN 7730
```

```
7350  REMOTE 723
7360  OUTPUT 723;"F1RAN4"
7370 !INPUT "Fr:11 to 20",F
7380  F=15
7390  OUTPUT 717;"F";F
7400 !INPUT "Wait,sec:",W
7410  W=2
7420  PEN 5
7430  S=Left-.5
7440  E=Right-.5
7450  PRINT "Fr #";F,"W=";W;"sec"," Step=";T
7460  I=0
7470  FOR J=S TO E STEP T
7480  J=PROUND(J,-5)
7490  I=I+1
7500  OUTPUT 717;"BI";J;"E00V"
7510  WAIT W
7520  OUTPUT 717;"E"
7530  ENTER 717;A
7540  Cy(I)=A*1.E+12
7550  ENTER 723;V
7560  Xy(I)=V
7570  NEXT J
7580  Imax=I
7590  OUTPUT 717;"BI0E00V"
7600  PENUP
7610  !
7620              FOR I=2 TO Imax
7630          IF Cfbtot<Cy(I) THEN
7640        Cmax=Cy(I)
7650        Cmin=Cy(I-1)
7660        Vmax=Xy(I)
7670        Vmin=Xy(I-1)
7680        GOTO 7710
7690          END IF
7700              NEXT I
7710    Vshift=(Cfbtot-Cmin)*(Vmax-Vmin)/(Cmax-Cmin)+Vmin
7720   !
7730       PEN 4
7740         FOR I=1 TO Imax
7750       PLOT Xy(I)-Vshift,Cy(I)
7760       PENUP
7770          NEXT I
7780      PEN 1
7790    FOR I=1 TO Imax
7800      PLOT Xy(I),Cy(I)
7810      PENUP
7820    NEXT I
7830   !
7840     SUBEND
7850 SUB Spline(N,Narg,X_(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
7860 !    Subprogram for spline interpolation and derivative calculations
7870 !    Lines from 7850 to 8660
8660 SUBEND
```

APPENDIX B

```
10    !         "COMBINED HIGH-LOW FREQUENCY MIS CAPACITANCE METHOD
20    !
30    OPTION BASE 1
40    DIM C(500),V(500),Cy(500),Xy(500)
50    DIM Clf(500),Vlf(500),Chf(500),Vhf(500)
60    DIM Bias(100),μ(100)
70    DIM Vb(500),Eμ(500),Cit(500),Dit(500)
80    !
90      Cm=1400
100     Qe=1.60218E-19                    !C
110     Epo=3.9*8.85418E-14               !F/cm
120     Eps=11.9*8.85418E-14
130     Epn=7.5*8.85418E-14                !F/Cm
140   !
150     Dox=6.85E-6                        !cm
160     Dnt=8.5E-6                        !Cm
170     Cox=Epo/Dox*4.E-2                 !F/cm^2
180     Cnt=Epn/Dnt*4.E-2                 !F/Cm^2
190     Con=Cox*Cnt/(Cox+Cnt)             !F/Cm^2
200     Kb=1.38066E-23                    !J/K
210     T=295                             !K
220     Ni=1.45E+10                       !cm^(-3)
230     Nd=1.1E+15                         !cm^(-3)
240   !
250     β=Qe/Kb/T
260     Ld=SQR(Eps/(Qe*Nd*β))
270     Co=(Ni/Nd)^2
280     Ao=SQR(2)*Eps/(β*Ld)
290     Fai=LOG(Nd/Ni)/β
300     Cfb=Eps/Ld*4.E-2
310   ! Ctfb=Cox*Cfb/(Cox+Cfb)*1.E+12
320     Cfbtot=Con*Cfb/(Con+Cfb)*1.E+12
330   !
340   Left=-8
350   Right=2
360   Myg=2
370   IF Myg=1 THEN
380   PLOTTER IS 705,"HPGL"
390   OUTPUT 705;"VS7.5;"
400   ELSE
410   GINIT
420   END IF
430           CALL Graph(Left,Right,Cm)
440           CLIP ON
450   Mode=1
460   Step=.1
470       CALL Plot_c_v(Mode,Left,Right,Cm,Step,Cy(*),Xy(*),Vshift,Imax,Cfbtot,M
yg)
480       PAUSE
490       IF Myg=1 THEN 660
500   !
510   Rate=.1
520   PRINT "Step=";Step,"Rate=";Rate
530   CLEAR 727
540   DIM A$[30]
550   OUTPUT 727;"F3RA1I3A1B2L2M3"          !C-V,AUTO,MEDIUM,Va,Vb,1mA,10mA
```

```
560   OUTPUT 727;"PS";Left-2;";PT";Right+Step;";PE";Step;";PHI0;PV";Rate;";"
570   OUTPUT 727;"W1"
580   I=0
590   I=I+1
600   ENTER 727;A$
610   C(I)=VAL(A$[4,13])
620   V(I)=VAL(A$[16,21])
630   IF A$[2,2]<>"L" THEN 590
640       Cmax=MAX(C(*))
650   Im=I
660   PEN 4
670   FOR J=15 TO Im
680       PLOT V(J),C(J)*1.E+12
690       PENUP
700   NEXT J
710   PAUSE
720   INPUT "Repeet?,  1 or 2",Myg
730   IF Myg=2 OR Myg=1 THEN 370
740   !
750   PLOTTER IS CRT,"INTERNAL"
760   Eps=1.E-4
770   N=Imax
780   Narg=200
790   ALLOCATE X(N),Y(N),Domain(Narg),Deriv(Narg),Func(Narg)
800   FOR I=1 TO N
810     X(I)=Xy(I)
820     Y(I)=Cy(I)
830   NEXT I
840   FOR I=1 TO Narg
850     Domain(I)=-3+(I-1)*(1+3)/(Narg-1)
860   NEXT I
870   CALL Spline(N,Narg,X(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
880   FOR I=1 TO Narg
890     Vhf(I)=Domain(I)
900     Chf(I)=Func(I)
910     PEN 1
920     PLOT Vhf(I),Chf(I)*1.E+12
930     PENUP
940   NEXT I
950   DEALLOCATE X(*),Y(*),Domain(*),Deriv(*),Func(*)
960   !
970   N=Im-15
980   ALLOCATE X(N),Y(N),Domain(Narg),Deriv(Narg),Func(Narg)
990   FOR I=1 TO N
1000    X(I)=V(I+15)
1010    Y(I)=C(I+15)
1020  NEXT I
1030  FOR I=1 TO Narg
1040    Domain(I)=-3+(I-1)*(1+3)/(Narg-1)
1050  NEXT I
1060  CALL Spline(N,Narg,X(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
1070  FOR I=1 TO Narg
1080    Vlf(I)=Domain(I)
1090    Clf(I)=Func(I)
1100    PEN 1
1110    PLOT Vlf(I),Clf(I)*1.E+12
1120   PENUP
1130  NEXT I
1140  DEALLOCATE X(*),Y(*),Domain(*),Deriv(*),Func(*)
1150  PAUSE
```

```
1160  !
1170          FOR K=1 TO 100
1180      Psi=-.2+(K-1)*.01
1190      Trm1=EXP(-β*Psi)+β*Psi-1
1200      Trm2=EXP(β*Psi)-β*Psi-1
1210      Fo=Trm1+Co*Trm2
1220        IF Fo<=0 THEN 1280
1230      Qs=SGN(Psi)*Ao*SQR(Fo)
1240      Vi=Qs/Cox*.04
1250      Bias(K)=-Vi-Psi+Vshift
1260      Spot=-Psi
1270      μ(K)=.56-Fai-Spot
1280            NEXT K
1290 !
1300  N=100
1310  ALLOCATE X(N),Y(N),Domain(Narg),Deriv(Narg),Func(Narg)
1320  FOR I=1 TO N
1330    X(I)=Bias(N+1-I)
1340    Y(I)=μ(N+1-I)
1350  NEXT I
1360  FOR I=1 TO Narg
1370    Domain(I)=-3+(I-1)*(1+3)/(Narg-1)
1380  NEXT I
1390  CALL Spline(N,Narg,X(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
1400  FOR I=1 TO Narg
1410    Vb(I)=Domain(I)
1420    Eμ(I)=Func(I)
1430  NEXT I
1440  DEALLOCATE X(*),Y(*),Domain(*),Deriv(*),Func(*)
1450  !
1460 ! INPUT "Scale?,1E+12?",New
1470 Myg=3
1480    New=1.E+12
1490    IF Myg=1 THEN
1500   PLOTTER IS 705,"HPGL"
1510   OUTPUT 705;"VS7.5;"
1520   ELSE
1530   PLOTTER IS CRT,"INTERNAL"
1540   IF Myg=2 THEN 1930
1550   END IF
1560  VIEWPORT 20,110,25,85
1570  WINDOW .2,.8,0,10
1580  PEN 1
1590  GRID .1,1
1600  PEN 6
1610  CLIP OFF
1620  CSIZE 3.7
1630  LORG 6
1640  FOR I=.3 TO .8 STEP .1
1650  MOVE I,0
1660  LABEL USING "#,K";I
1670  NEXT I
1680  LORG 8
1690  CSIZE 3.2
1700  FOR I=0 TO 10 STEP 1
1710  MOVE .2,I
1720  LABEL USING "#,K";I
1730  NEXT I
1740  LORG 4
1750  DEG
```

```
1760  LDIR 90
1770  PEN 5
1780  CSIZE 3.5
1790  MOVE .15,5
1800  LABEL "Nit(X1.E+12/cm^2/ev)"
1810  LDIR 0
1820  LORG 6
1830  MOVE .5,-.8
1840  LABEL "Energy, (ev)"
1850  PEN 3
1860  CSIZE 3.25
1870        MOVE .55,-1.8
1880     LABEL "Fig.   Interface trap level density Versus Energy Measured with"
1890     MOVE .55,-2.6
1900     LABEL "respect to the Conduction band edge at the Si-SiO2 Interface"
1910  !
1920  CLIP ON
1930  PEN 2
1940   FOR I=1 TO Narg
1950     Cit(I)=1/(1/C1f(I)-1/Con)-1/(1/Chf(I)-1/Con)
1960     Dit(I)=Cit(I)/Qe
1970     PLOT Em(I),Dit(I)/New
1980     PENUP
1990   NEXT I
2000   PAUSE
2010   INPUT "Repeet ?,   1 or 2",Myg
2020   IF Myg=1 OR Myg=2 THEN 1490
2030  END
2040            SUB Graph(Left,Right,Cm)
2110  VIEWPORT 20,110,25,85
2120  WINDOW Left,Right,0,Cm
2130  PEN 1
2140  GRID 1,200
2150  PEN 6
2160  CLIP OFF
2170  CSIZE 3.7
2180  LORG 6
2190  FOR I=Left TO Right STEP 1
2200  MOVE I,0
2210  LABEL USING "#,K";I
2220  NEXT I
2230  LORG 8
2240  CSIZE 3.2
2250  FOR I=200 TO Cm STEP 200
2260  MOVE Left,I
2270  LABEL USING "#,K";I
2280  NEXT I
2290  LORG 4
2300  PEN 5
2310  CSIZE 4
2320  MOVE (Left+Right)/2,Cm+Cm/60     ! +Cm/10
2330  LABEL "C_V"
2340  DEG
2350  LDIR 90
2360  CSIZE 3.5
2370  MOVE Right*1.2,Cm/2
2380  LABEL "capacitance"
2390  LDIR 0
2400  LORG 6
```

```
2410  MOVE (Left+Right)/2,-Cm/15
2420  LABEL "voltage"
2430  PEN 3
2440  CSIZE 3.25
2450  MOVE (Left+Right)/2,-Cm/5
2460  LABEL "Fig.   Combined High-Low Frequency MIS Capacitance-Voltage Curve"
2470  MOVE (Left+Right)/2,-Cm/4
2480  LABEL "(a) High Frequency Curve  (b) Low Frequency Curve"
2490  MOVE -1.5,300
2500  LABEL "(a)"
2510  MOVE -2.5,Cm/1.3
2520  LABEL "(b)"
2530  SUBEND
2540  !
2550     SUB Plot_c_v(Mode,Left,Right,Cm,Step,Cy(*),Xy(*),Vshift,Imax,Cfbtot,Myg
)
2560     IF Myg=1 THEN 2980
2570  REMOTE 717
2580  CLEAR 717
2590  OUTPUT 717;"A2B3C";Mode;"M1"
2600  OUTPUT 717;"E"
2610  REMOTE 723
2620  OUTPUT 723;"F1RAN4"
2630  OUTPUT 717;"BI";Left-1;"E00V"
2640 !   INPUT "Fr:11 to 20",F
2650    F=15
2660  OUTPUT 717;"F";F
2670 !   INPUT "Wait,sec:",W
2680    W=1
2690  PRINT "Fr #";F,"W=";W;"sec"
2700  PAUSE
2710  S=Left-1
2720  E=Right
2730  I=0
2740  FOR J=S TO E STEP Step
2750  J=PROUND(J,-5)
2760  I=I+1
2770  OUTPUT 717;"BI";J;"E00V"
2780  WAIT W
2790  OUTPUT 717;"E"
2800  ENTER 717;A
2810  Cy(I)=A
2820  ENTER 723;V
2830  Xy(I)=V
2840  NEXT J
2850  Imax=I
2860  OUTPUT 717;"BI0E00V"
2870  Maxc=MAX(Cy(*))
2880              FOR I=2 TO Imax
2890     IF Cfbtot*1.E-12<Cy(I) THEN
2900     Cmax=Cy(I)
2910     Cmin=Cy(I-1)
2920     Vmax=Xy(I)
2930     Vmin=Xy(I-1)
2940     GOTO 2970
2950     END IF
2960              NEXT I
2970     Vshift=(Cfbtot*1.E-12-Cmin)*(Vmax-Vmin)/(Cmax-Cmin)+Vmin
2980   PEN 2
2990  FOR I=1 TO Imax
3000  PLOT Xy(I),Cy(I)*1.E+12
```

```
3010  PENUP
3020  NEXT I
3030  PENUP
3040      SUBEND
3050 SUB Spline(N,Narg,X_(*),Y(*),Domain(*),Func(*),Deriv(*),Int,Eps)
3060 !     Subprogram for spline interpolation and derivative calculations
3070 !     Lines from 3050 to 3740
3740 SUBEND
```

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DECLARATION

The thesis is my original work, has not been presented for a degree in any other university and that all sources of materials used for the thesis have been duly acknowledged.

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This thesis has been submitted for examination with my approval as University Advisor.

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