ADDIS ABABA UNIVERSITY
SCHOOL OF GRADUATE STUDIES
ADDIS ABABA INSTITUTE OF TECHNOLOGY (AAiT)

MODELING OF SILICON NANOWIRE FIELD EFFECT TRANSISTORS

A thesis submitted to the School of Graduate Studies of Addis Ababa University in partial fulfilment of the requirements for the degree of Master of Science in Electrical Engineering (Microelectronics)

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July 2011

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ACKNOWLEDGEMENTS

I would like to express my heartiest gratitude to my advisor, Dr. Adeyabeba Abera for her invaluable advice. I would like to acknowledge that without her advice and critical reading, this thesis would not have been completed at all.

Next, I thank Almighty God for always being there to guide me through thick and thin. I would also like to thank my family especially my mother for her endless support, love and patience. Her love, care and support over so many years have really helped to shape my future. Also, my thanks goes to my best friend Rakeb, for being there for me when I need help. Finally, I would like to thank AAiT for its financial support to undergo my thesis work.

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DECLRATION

I, the undersigned, here by declare that this thesis is my original work performed under the supervision of Dr. Adeyabeba Abera has not been presented as a thesis for a degree program in any other university and all source of materials used for the thesis are duly acknowledged

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This thesis has been submitted for examination with our approval as university advisor.

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ABSTRACT

Modeling and simulation of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is very essential in order to understand the device physics, electrostatics and other important phenomena occurring in this device. Therefore, in this thesis the modeling and simulation of Silicon Nano Wire field Effect Transistors (SiNW FETs) is done. The modeling is done assuming both ballistic transport and transport in the presence of scattering. The modeling of SiNW FETs assuming ballistic transport is an extension of the Natori's theory of ballistic MOSFETs. The second part of the modeling, which is developed on the assumption of scattering transport, is based on McKelvey's flux method. When the scattering effects are assumed to be absent, the scattering model reduces to the ballistic model. Therefore, the main novelty introduced in this thesis is the extension of the previous models and the incorporation of these two models together. After the derivation of the model, its benchmarking is also done. This is accomplished by comparing the simulation results of the developed model, which is implemented using MATLAB programming, with that of the experimental and numerical simulation results. Various important parameters are extracted and used for comparison, the main ones being the On-state current (I_{on}), the Off-state current (I_{off}), the Subthreshold Slope (SS) and drain induced barrier lowering (DIBL). The comparison shows that there is a good agreement between the simulation results of the developed model and the experimental and numerical simulation results, which indicates the validity of the model. Finally, the effect of scaling of the physical parameters on the device performance is investigated. The main parameters chosen for this investigation are the diameter of the Nano Wire (NW) and the gate oxide thickness. When a simulation is done by varying these parameters, I_{on} and I_{off} currents are found to be affected greatly.

CHAPTER ONE : INTRODUCTION

This thesis presents compact modeling of SiNW FETs assuming both ballistic and scattering transport mechanisms. The modeling of the device assuming ballistic transport is based on Natori's theory of ballistic MOSFETs and extended to include two dimensional electrostatic effects. On the other hand, the modeling which assumes transport in the presence of scattering is based on McKelvey's flux theory. The compact modeling is benchmarked by comparing its simulation results with that of the device experimental results. In addition, in order to further assess the validity and accuracy of the model, its simulation results are compared with that of the numerical simulation results. Finally, in this thesis, the effect of varying the different parameters of SiNW FET on its performance is discussed.

1.1 Background of the Study

Among many great inventions made in the 20th century, electronic circuits, which later evolved into Integrated Circuits (Ics), are probably the biggest, when considering their contribution to human society. Entering the 21st century, the importance of Ics has increased even more [1]. In fact, without the help of Ics, recent high-technology society with the internet, cellular phone, car navigation, digital camera, and robot would never have been realized. Nowadays, Ics are indispensable for almost every activity of our society [2]. Ics are combinations of various active and passive components; among the main active components the MOSFET takes the major place. The basic principle of the MOSFET was first proposed by Julius Edgar Lilienfeld in 1925. However it was not until 1960 that the first MOSFET was fabricated and demonstrated by Dawon Kahng and Martin Atalla at the Bell Labs [3].

The constant request for performance improvement of electronic devices is mainly satisfied by reducing the size of their active components, the transistors. Scaling of semiconductor devices to the nanoscale regime can lead to device performance improvements. These include reduction in operating voltage, increased speed and greater packaging densities [4]. The more an IC is down scaled, the higher becomes its packing density, the higher its circuit speed, and the lower its power dissipation [5]. Generally speaking, thirty years of aggressive scaling have pushed the device

dimensions close to the atomic range. Recently reported structures of MOSFETs already have channel lengths in the order of 10 nm or even smaller [6]. SiNW FET has been one of the most important inventions in the last few years in order to overcome the various undesirable effects met at this very small scale. Therefore, a modeling and simulation work is very important in order to understand this new device and make its designing very easy, hence, enabling fast and accurate fabrication of the device. In this section the classical scaling laws of MOSFETs, alternative architectures to the planar MOSFETs and a brief introduction of NW FETs is presented. Also, the different approaches used in the modeling of NW FETs and their advantages and limitations will be given.

1.1.1 Scaling of MOSFETs

The transistor scaling has been successfully predicted by Moore's law. It stated that the number of transistors on one IC chip has quadrupled every three years and the feature size of each transistor has shrunk to half of its original value at the same time [7]. To date, microprocessors with more than 100 million transistors have been realized. Also, the corresponding MOSFET gate lengths in modern IC chips have entered the sub-100 nm regime. Continued success in device scaling is necessary for maintaining the successive improvements in IC technology [5].

Classically the scaling has been guided by a few approaches with specific application objectives in view. Based on the assumption of (i) dimensional miniaturization of the device through the improvement of lithography, and (ii) invariance of the basic structure of the MOS transistor, the scaling laws may be classified into many groups. Among these constant field scaling (CFS), constant voltage scaling (CVS), quasi constant voltage scaling (QCVS) and generalized scaling (GS) take the major place [8]. This is summarized in Table 1.1.

In Table 1.1, λ is the scaling factor and shows how the different parameters are scaled according to the classical scaling laws namely, CFS, CVS and GS laws. Even though these classical scaling laws served as standards in the scaling of MOSFETs up to the 32 nm node [1], they will be invalid beyond this technology node. Therefore, in order to continue the scaling process, alternative architectures and materials are being investigated recently.

1.1.2 Alternative Architectures and Materials

The request for increasing performance and reduced area occupancy for both active and passive electronic components pushes the scaling process every day closer to the physical limits of the silicon-based MOS technology. However, the classical MOSFET is approaching its minimum channel length due to the limit imposed by strong short channel effects (SCEs), ultra-thin gate

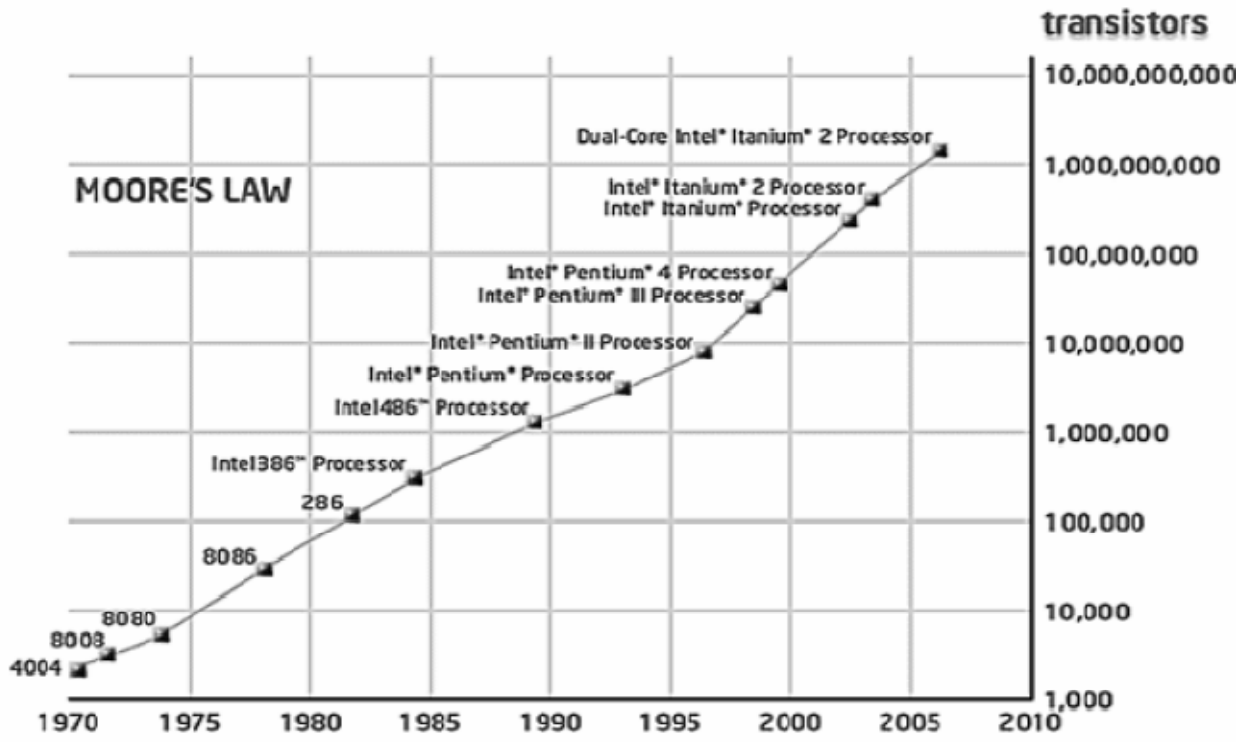


Figure 1.1 The dramatic increase of transistor number with each microprocessor technology according to Moore's law [7].

oxide tunneling, and higher channel doping [9]. To further maintain the performance improvement by scaling the device dimension, various technologies, such as mobility enhancement, metal gate with high dielectrics, optimal doping profile design, vertical-channel transistor, etc., have been proposed [10]. Among these advanced technologies, succession of device structure from planar to vertical-channel transistors is the main trend in Very large Scale Integration (VLSI) technologies. The vertical-channel transistors with multiple-gate surrounded have inherently good suppression of SCEs, high transconductance (g_m) and ideal SS. Additionally, they provide more effective suppression of I_{off} and enhanced I_{on}. Also, the vertical-channel transistors are more compact than

conventional planar transistors, enabling higher transistor density which translates to smaller overall nanoscale electronics. Figure 1.2 plots an evolution of transistor architecture from planar MOSFETS to ultrathin-body (UTB), silicon-on-insulator (SOI), double-gate (DG), omega gate, and NW fin-type FETs (FinFETs) [11].

Table1.1 Effect of scaling laws on MOSFET device/circuit performance [1]

Parameter	**Notation**	**Constant-Field**	**Generalized-Field**	**Constant-Voltage**
Physical Dimensions	W, L, $\boldsymbol{t_{ox}}$	1/λ	1/λ	1/λ
Doping concentration	$\boldsymbol{N_B}$	λ	$\boldsymbol{\lambda^2/k}$	$\boldsymbol{\lambda^2/1}$
Voltage	$\boldsymbol{V_{DD}}$,$\boldsymbol{V_{th}}$	1/λ	1/k	1
Electric Field	E	1	λ/k	λ
On-current	$\boldsymbol{I_D}$	1/λ	$\boldsymbol{\lambda/k^2}$	λ
Capacitance	$\boldsymbol{C_G = A\frac{\varepsilon_{ox}}{t_{ox}}}$	1/λ	1/λ	1/λ
Power Dissipation	$\boldsymbol{V_{DD}I_D}$	$1/\lambda^2$	1/kλ	1/λ
Gate delay	$\boldsymbol{t_{gate}}$	1/λ	k/λ^2	$1/\lambda^2$

Numerous examples of NW fabrication and integration have been recently reported. In addition, the use of different channel materials (e.g. Si, Ge, GaAs) and lateral dimensions and shapes are demonstrated [11]. Among the various possibilities, Si is still reported as the leading investigation material. This is due to the compatibility with the standard electronic industry. SiNW FET is generally viewed as a promising next generation device, exhibiting high I_{on}/I_{off} ratio, excellent gate controllability through gate-all-around (GAA) structure, and the immunity from SCEs [13]. Also, SiNWs are natural extensions of the scaling process of MOSFET devices. In particular, the use of a top-down fabrication approach, combining advanced chemical and lithographic process, has proved its technological compatibility with the standard Complementary MOS (CMOS) process [14].

NW FETs have recently attracted considerable attention as a possible next-generation candidate to replace the conventional planar MOSFETs. This is mainly due to its capability to enhance the

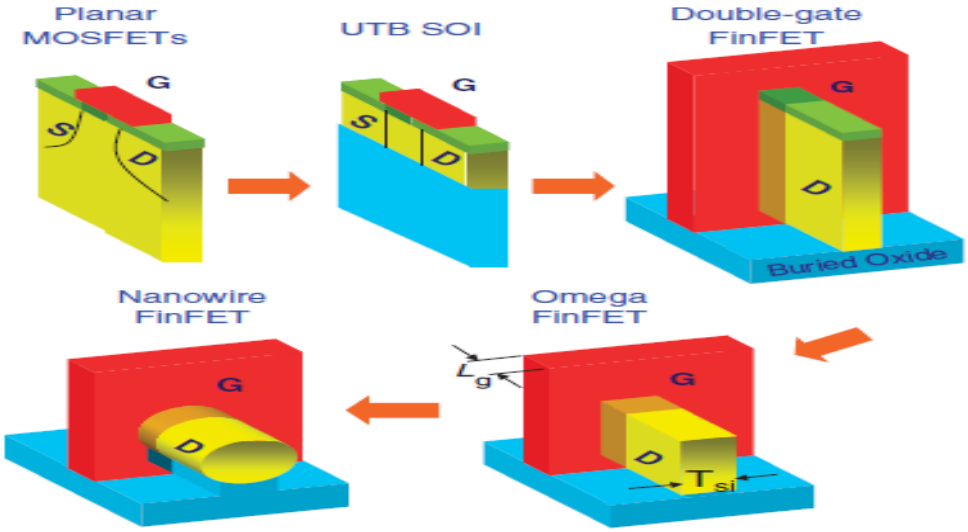


Figure 1.2 The evolution of transistor architecture from planar MOSFETs to ultrathin-body

gate control and hence to suppress the SCEs. N-type as well as p-type prototypes of such NW transistors with feature sizes of a few nanometers have been fabricated and their device performance has been explored [12].

1.1.3 Modeling Approaches

In order to understand the device physics, electrostatics, transport and other phenomena, modeling and simulation is very important. MOSFET models play an important part in the development of an efficient chip industry. These models have been continuously developed and improved over the past many years. These improvements resulted in the increase of the model parameters to cover additional effects [15]. The circuit designer's efficiency to develop a circuit depends mainly on the device model. The accuracy and simplicity of the model has a deep influence on the designing and fabrication of the circuit. Thus device models act as a bridge between the IC designers and those working for process technology development as shown in Figure 1.3 [16].

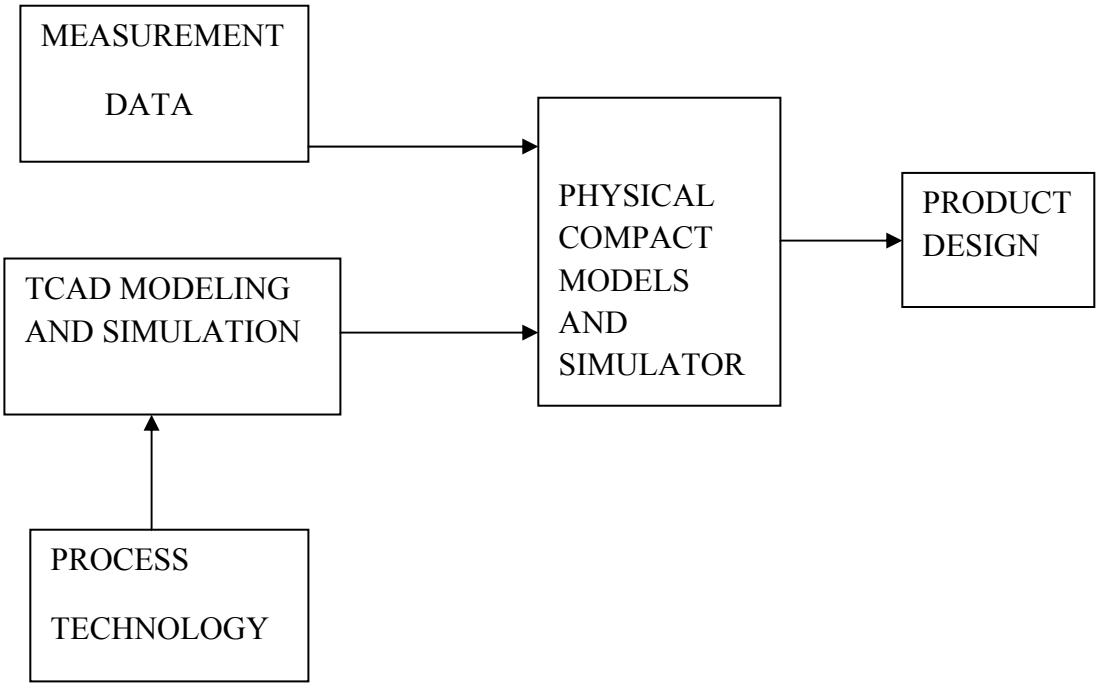


Figure 1.3 Complete flow of the Technology, Modeling and Design [16].

In the modeling of nanoscale MOSFETs, there are generally, two types of modeling approaches; the numerical modeling approach and the compact modeling approach [6].

1.1.3.1 The Numerical Modeling Approach

In physical numerical modeling, the nonlinear partial differential Equations (PDEs) that describe charge distribution, charge transport, current continuity, and so forth, in the transistor structure are solved in the simulator. In the simulation, the transistor geometry is discretized in two or three dimensions. Then, the solution of the PDEs and Quantum Mechanical (QM) Equations is performed for each cell or node in the structure. This requires complex solution techniques to be used, such as finite-difference and finite-element methods. The solution of these nonlinear PDEs takes a long time. The accuracy of the solution depends on how well the physical properties and dimensions of the device are estimated, on the approximations used in the fundamental semiconductor Equations, and on the numerical techniques applied in the solution of the system of Equations. Therefore, these models are computationally intensive, complex and take a lot of computation time to solve the circuits [17].

1.1.3.2 The Compact Modeling Approach

While physical numerical modeling provides a viable route for detailed device design and technology development and optimization, it is generally impractical for circuit design. Aside from the computational overhead involved, it is usually expected that the transistor or the IC process has been determined by the time circuit design begins. Therefore, we can devise a more appropriate model that can be used in the circuit simulator for the design of the IC or discrete transistor product. Such models generally fall under the rubric compact [17]. In fact, in many new device technology developments, compact models can be created from the physical model simulations. The compact models can be updated as the technology develops. Therefore, the circuit design is always in step with the latest technology improvements, enabling a much reduced new product introduction cycle [18].

There are a couple of approaches for selecting the types of compact modeling, which are based on the charge based model or the Surface Potential (SP) based models as shown in Table 1.2. These two categories of advanced MOSFET model are being a model today and are available commercially as Electronic and Electrical Computer Aided Design (ECAD) tools [15].

Table 1.2 Approaches of Compact Modeling [15].

Charge- Based Models	**Surface-Potential Based Models**
ACM (Advanced Compact Model)	HiSIM (Hiroshima-University STARC IGFET Model)
EKV (Enz-krummenacher-Vittoz Model)	MM 11 (MOS Model 11)
BSIM (Berkeley Short-channel IGFET Model)	SP (an advanced Surface Potential Based Compact MOSFET Model)

1.2 Problem Statement

Continuous shrinking of channel length (Lc) in silicon CMOS devices to increase performance has led to the development of non-planar devices. Nanowire based Field- Effect-Transistors (FETs) are an attractive candidate in this area due to better electrostatic gate control. Recently many

experimental groups have demonstrated fabrication of silicon nanowire (SiNW) transistors of diameters even down to 3nm [19]. To understand the working of such small devices it is important to have proper theoretical model which encapsulates quantum transport mechanisms. In this task, modeling and numerical simulation play an important role to predict the behavior of these important devices. Therefore, in order to fully assess the ultimate performance of SiNW FETs, proper modeling is essential in understanding the electrical characteristics of SiNW transistors.

Currently, there exists well known numerical modeling approaches such as the atomistic Tight binding modeling [20], which understands the finite number of atoms in the structure, their local arrangement with details such as strain distribution and disorder, and the Non Equilibrium Green's function formalism (NEGF) [14] which is also a detailed and efficient numerical approach. However, these modeling approaches are very difficult to implement in conventional circuit simulators and are computationally time consuming. Therefore a compact analytical modeling scheme is appropriate for the modeling of these devices.

For silicon CMOS technology, the present industry compact modeling standards for circuit simulation, such as BSIM3 [1], BSIM4 [2], EKV [3], MOS Model 9 [8], and MOSA1 [8], are based on one-dimensional (1D) theory, initially developed for long-channel FETs. However, the steady reduction in feature size, with gate lengths presently well into the sub-100 nm regime [9], has strongly enhanced a number of phenomena, collectively known as short-channel effects, related to the two- and even the three-dimensionality of the device structures. To keep pace with technology, this has necessitated extensive, phenomenological modifications of the 1D models. Therefore, as a prerequisite to obtaining very precise descriptions of the next generations of MOSFETs, the consideration of 2D models has become necessary. Another issue is that of the appropriate transport model for nanowire transistors. As demonstrated in [21], silicon MOSFETs with effective channel length smaller than 50 nm will not be fully ballistic, so it is reasonable to assume that even for SiNW FETs a degree of scattering will be present. This implies that a compact analytical modeling scheme which is used to model ballistic transport and which incorporates scattering mechanisms is necessary. Therefore, in this thesis a compact analytical modeling scheme which incorporates two dimensional electrostatic effects and scattering mechanisms is proposed.

1.3 Objectives

SiNW FETs are the main candidates of post CMOS devices to continue the down scaling process and hence for achieving performance improvements. The International Technology Roadmap for Semiconductors (ITRS-2001) has identified a series of challenges that must be solved before these devices can enter the manufacturing of CMOS-based ICs [23]. Among them, a complete compact modeling of these structures remains an issue. Therefore, the general objective of this thesis is the derivation of an analytical compact model for SiNW FETs. The main novelty introduced in this thesis is the extension of existing models and the incorporation of the ballistic and scattering modelings together.

The specific objectives include:

- Benchmarking of the developed compact model by comparing its simulation results with that of the experimental device and the numerical modeling simulation results.
- Evaluation of the performance of SiNW FETs by comparing its parameters with that of the planar MOSFETs.
- Assessing the effect of scaling of the diameter and oxide thickness on the performance of the device.

1.4 Scope of the Study

This thesis focuses on the derivation of an analytical compact model for SiNW FETs considering both ballistic transport and scattering limited transport. Generally, based on available resources and limited time frame, this thesis is narrowed down to the following scope of work:

1. Derive an analytic compact model for ballistic SiNW FETs by extending Natori's theory of ballistic MOSFETs to include two dimensional electrostatic effects.
2. Derive an analytic compact model considering scattering transport mechanism by modifying Mckelvey's flux method for one dimensional SiNW FETs.
3. Incorporate the model equation into MATLAB program (code) and implement (simulate) the program in the MATLAB software. MATLAB software is chosen for the simulation because it's convenient to incorporate the model equations and it take less CPU computation time than other conventional circuit simulators.

4. Analyze the simulation result by comparing the simulation results of the developed model with that of the experimental and numerical simulation results.
5. Observe the effect of varying the nanowire diameter and oxide thickness on the performance of the device.

1.5 Significance and Relevance of the Study

Device modeling can be very useful even if it is not fully 'predictive', because it can provide optimization guidelines, explanations of the characterization results, and insights of the transport mechanisms. Several issues can be understood with the help of modeling tools, such as for example the relevance of drain-to-source tunnelling, the subthreshold behaviour, and the Drain-induced Barrier Lowering (DIBL) [22]. Therefore the significance of this thesis is the contribution of a compact analytical model which can be incorporated into conventional circuit simulators, such as SPICE, so that it is used in the device design developments. This model can be used by those individuals and companies (Universities) for designing and further study of these important post CMOS devices.

1.6 Thesis Outline

There are five chapters included in this thesis. In the following paragraphs, the outline of each chapter is presented starting from the first chapter.

Chapter one starts by giving a general introduction and background of the thesis. It then describes the problem statement of the thesis, its objectives, scope and finally it gives its significance.

In the second chapter, an overview of NWs, the different types of NWs being fabricated today, their electrical properties and their applications is presented first. It then proceeds to present an introduction of SiNW FETs, their transport mechanism and different operation modes they possess. Finally the evaluation of its performance and its advantages over planar FETs is discussed.

The third chapter is the model derivation part of the thesis and is divided in to two sections. The first section is development of the model for SiNW FETs assuming ballistic transport. It starts by describing the very principles the Natori's theory is based up on. It then proceeds to describing the development of the model. The second section describes the development of the model by assuming

scattering assisted transport. It starts by describing McKelvey's flux theory and then proceeds to the main model derivation.

Chapter four is the simulation results and discussion part of the thesis. It begins by benchmarking the simulation results of the derived model with the experimental simulation results. Then, it proceeds the benchmarking to comparing the simulation results with the numerical simulation results. Finally, the effect of the scaling of NW diameter and oxide thickness on the device performance is investigated using the simulation of the device.

The final chapter, chapter five, concludes the main works done and results obtained in this thesis and direct some ideas for future work.

CHAPTER TWO : SiNW FET TECHNOLOGY AND LITERATURE REVIEW

The NW transistor is one candidate which has the potential to overcome the problems caused by SCEs in SOI MOSFETs and has gained significant attention from both device and circuit developers. In addition to the effective suppression of SCEs due to the improved gate strength, the multi-gate SiNW FETs show excellent current drive and have the merit that they are compatible with conventional CMOS processes [24].

In this chapter we will review FETs made from NWs. The chapter is divided in to two main sections. The first section presents the various types of NWs, their electrical properties and the different applications they have. In the second section, an introduction about SiNW FETs is presented. In addition, in this section, the transport mechanism and the operation modes of SiNW FETs is discussed. Finally a review of performance evaluation of this device and its advantages over planar FETs is addressed.

2.1 Overview of Nano Wires

Following the discovery of Carbon Nanotubes (CNTs) by Iijima [24], there has been great interest in the synthesis and characterization of other One Dimensional (1D) structures, which include NWs, nanorods and nanobelts [25]. Inorganic NWs can act as active components in devices, as revealed by recent investigations. In the last 4–5 years, NWs of various inorganic materials have been synthesized and characterized [11]. A NW is an object with a 1D aspect in which the ratio of the length to the width is greater than 10 and the width does not exceed a few tens of nanometers [26]. Today, this definition has been extended to atomic and molecular wires, which have proved to exhibit very interesting physical properties without necessarily having the geometrical characteristics, defined earlier. NWs represent the smallest dimension for efficient transport of electrons and excitons. Thus, they will be used as interconnects and critical devices in nano-electronics and nano-optoelectronics [7]. They are especially attractive for nano-science studies as well as for nanotechnology applications. NWs, compared to other low dimensional systems, have two quantum confined directions, while still leaving one unconfined direction for electrical conduction [27]. Today, different types of NWs are being investigated and are being fabricated.

2.1.1 Types of NWs

NWs can be prepared from metals, semiconductors, organic molecules, etc. and offer prospects in mechanical, electronic, optical, or medical applications. Therefore, depending on the materials they are made, NWs are classified as: metallic NWs, semiconductor NWs and molecular NWs [28]. They can also be classified as elemental, metal oxide, metal nitride, metal carbide and metal Chalcogenide. Thus, NWs of elements, oxides, nitrides, carbides and chalcogenides have been generated by employing several strategies [25]. Figure 2.1 shows the images of different semiconductor NWs imaged using high-angle annular dark-field scanning transmission electron microscopy and Table 2.1 summarizes the different types of NWs together with their specific examples.

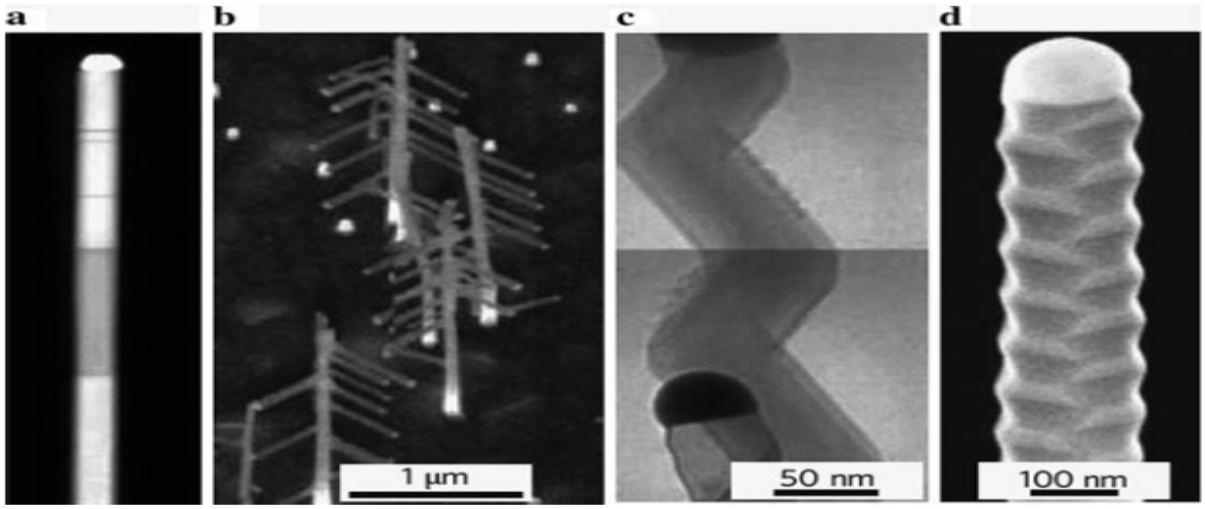


Figure 2.1 Images of different semiconductor NWs. (a) Axially modulated InAs/In NW (30 nm in diameter), (b) GaP NWs, (c) SiNWs, (d) Periodically twinned InP NW [28].

Although many different types of semiconductor NWs have been investigated, SiNWs have become prototypical NWs. This is because they can be readily prepared, the Si/SiO_2 interface is chemically stable, and SiNWs are utilized in a number of device demonstrations that have well-known silicon-technology-based counterparts [12].

Table2.1 The different types of NWs.

Types of NWs	**Specific Examples**
Elemental	Ge, B, In, Sn, Pb, Sb, Bi, Se, Te, Au, Ag, Fe, Co, Ni and Cu
Metal Oxide	MgO, Al_2O_3 ,Ga $_2O$ In_2O_3, SnO_2, SiO_2, GeO_2, TiO_2, MnO_2, Mn_3O_4, Cu_xO and ZnO
Metal Nitride	BN, AlN, GaN, InN, Si_3N_4 and Si_2N_2O
Metal Carbide	BC and SiC
Metal Chalcogenide	CdS, CdSe, CdTe, PbS, PbSe, Bismuth Chalcogenides, CuS, CuSe, ZnS and ZnSe, NbS_2 and $NbSe_2$

2.1.2 Electrical Properties of NWs

The effects of size on electrical conductivity of nanostructures and nanomaterials are complex, since they are based on distinct mechanisms. These mechanisms can be generally grouped into four categories: surface scattering including grain boundary scattering, quantized conduction including ballistic conduction, Coulomb charging, tunneling and widening of the band gap. In addition, increased perfection such as reduced impurity, structural defects and dislocations, would affect the electrical conductivity of nanostructures and nanomaterials [29].

When the size of a material is smaller than the de Broglie wavelength, electrons and holes are spatially confined and electric dipoles are formed. In addition, discrete electronic energy level would be formed in all materials. Similar to a particle in a box, the energy separation between adjecent levels increases with decreasing dimensions. Also, the electron Density of States (DOS) depends dramatically on the dimensionality of nanostructures [30]. Whereas for bulk systems a square-root dependence of energy prevails, a staircase behavior is a characteristic for Two Dimensional (2D) quantum well structures, spikes are found in 1D quantum wires (QWs), and discrete features appear in Zero Dimensional (0D) quantum dots [28]. The DOS for Three Dimensional (3D) (bulk), 2D (quantum well), 1D (QW) and 0D (quantum dots) is illustrated in Figure 2.2.

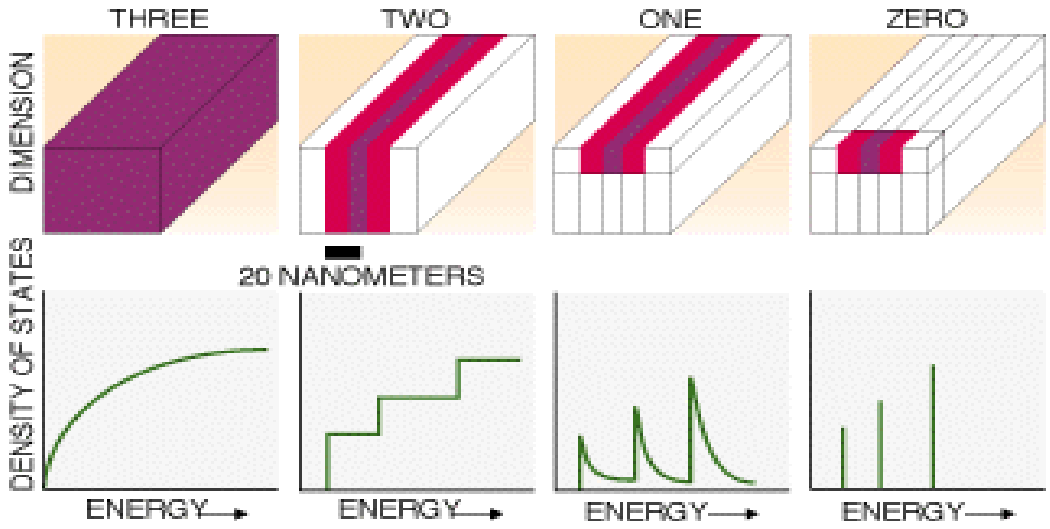


Figure 2.2 Electron density of states for 3D, 2D, 1D and 0D structures [30].

The other mechanism that occurs in quantum wires is ballistic conduction. It occurs when the length of device is smaller than the electron mean-free path. In this case, each transverse waveguide mode or conducting channel contributes Go = $2e^2/h$ = 12.9 kW to the total conductance. Another important aspect of ballistic transport is that no energy is dissipated in the conduction, and there exist no elastic scattering. The latter requires the absence of impurity and defects. When elastic scattering occurs, the transmission coefficients, and thus the electrical conductance will be reduced, which is then no longer precisely quantized [29]. Finally, tunneling conduction is a phenomenon that affects the electrical conductivity of NWs. Tunneling involves charge transport through an insulating medium separating two conductors that are extremely closely spaced. It occurs when the electron wave functions from two conductors overlap inside the insulating material, at extremely thin thickness of the insulator [30].

2.1.3 Applications of NWs

In the early 1980s it was theoretically predicted that QWs may have applications in high-performance transport devices due to their saw tooth like DOS [11]. Semiconductor NWs are emerging as a powerful class of materials that, through controlled growth and organization, are opening up novel opportunities for nanoscale electronic and photonic devices. From these QWs, logic gates such as inverters or oscillators can be built. QW FETs have emerged as powerful sensors

for label free detection of biological and chemical species. Crossed NWs can also be used to fabricate nanoscale p-n diodes, for example, for band-edge emission Light Emitting Diodes (LEDs) at the nanoscale cross-points [28].

SiNWs have been demonstrated as one of the promising building blocks for future nano-devices such as FETs, solar cells, sensors and lithium battery [24].

Generally, NWs have been pursued for their intrinsic ability to make smaller devices for several years. Vertically grown NWs have been shown in several materials, and hetero structures have been embedded within these wires to create quantum dots and resonant-tunneling diodes [30].

2.2 SiNW FETs

NW FETs have been proposed and now studied by many research groups around the world. This is because, they are promising candidate to sustain the relentless progress in scaling for CMOS devices [31]. Several key factors have contributed to the boom of NW research. First, semiconductor NWs can be prepared in high-yield with reproducible electronic properties as required for Large Scale integrated (LSI) systems. Second, compared with "top–down" nanofabricated device structures, "bottom–up" synthesized NW materials offer well controlled size; that is at or beyond the limits of lithography. In addition, the crystalline structure, smooth surfaces and the ability to produce radial and axial NW hetero structures can reduce scattering. These results in higher carrier mobility compared with nanofabricated samples with similar size. Finally, the body thickness (diameter) of NWs can be controlled down to well below 10 nm. Therefore, electrical integrity of NW-based electronics can be maintained even as the gate length is aggressively scaled. This is a feature that has become increasingly difficult to achieve in conventional MOSFETs [32].
GAA SiNW FETs have attracted significant interest because of their excellent electrostatic integrity even at the nanoscale. Various types of SiNW FETs are being explored as a promising candidate for future transistors replacing planar MOSFETs in logic and Dynamic Random Access Memory (DRAM) applications, and their fabrication is being studied either from top-down or bottom-up approaches [29]. The schematic of a GAA SiNW FET is shown in Figure 2.3.

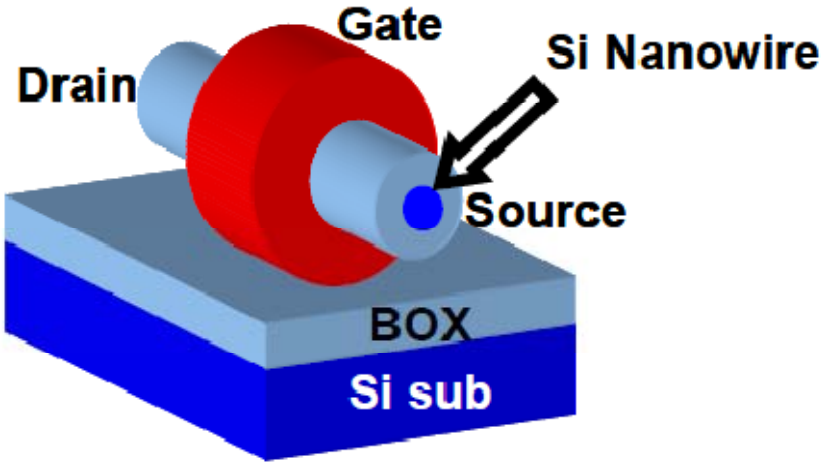


Figure 2.3 Schematic of GAA SiNW FET Structure [34].

SiNW FETs, unlike planar MOSFETs, have metal source and drain contacts. That is, the source and drain contacts are made from metals instead of degenerately doped semiconductors. Typically, positive Schottky barriers are observed at the metal/semiconductor interface due to the combined effect of metal work function and Fermi level pinning by surface states [12]. As a result, the device performance is to a large degree affected by contact properties. Because of this property, application of annealing can lead to the formation of essentially ohmic contacts and dramatically increase On-state currrent and the apparent field effect mobility. This is illustrated in Figure 2.5. A SiNW FET with aluminum source/drain contact is shown in Figure 2.4. Figures 2.5(a) and (b) show the output characteristics (I_{ds} - V_{ds}) graph and the transfer characteristics graph (I_{ds} - V_{gs}) graph respectively. From these graphs we can see that there is a huge increase of On-state current after annealing.

2.2.1 Transport Mechanisms of NW FETs

If the device length is smaller than the mean free path, it is very probable for carriers not to undergo any scattering event during their motion within the device and the transport is ballistic [15]. Since SiNW FETs have lengths in the order of nanometers their transport mechanism can be mainly described by ballistic transport. However, in general, electronic-carrier mobility in real

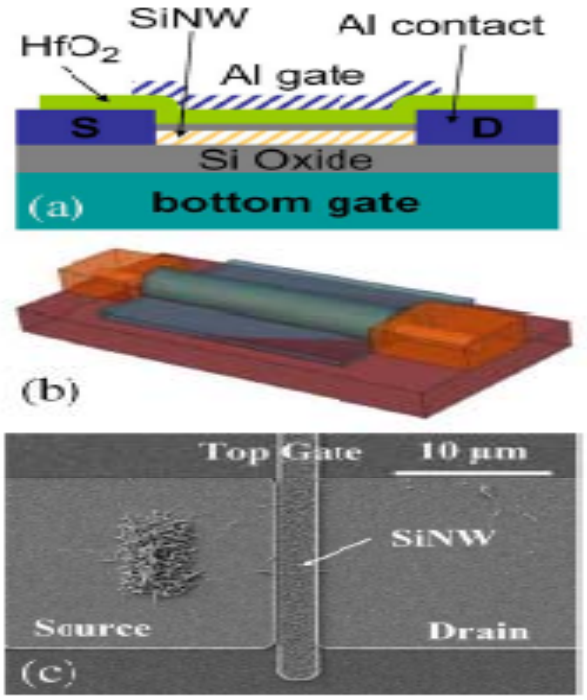


Figure 2.4 SiNW FET (a) Schematic drawing of device cross section along the length of the SiNW. (b) Three-dimensional schematic of top-gated SiNW FET. (c) Scanning electron beam micrograph of a typical top-gated SiNW FET with no gate-to-source/drain overlap [12].

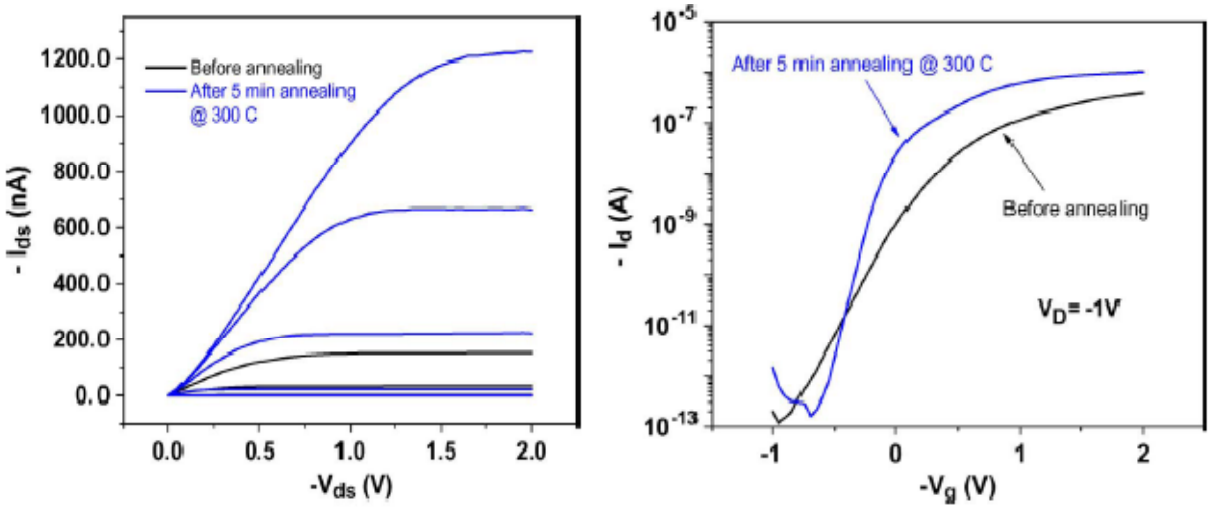


Figure 2.5 Electrical characterization of a typical top-gated SiNW FET before annealing and rapid thermal annealing for 300 sec at 300 ^{0}C. (a) $I_{ds} - V_{ds}$ curves at V_{gs} = +0.5 to −1.5 V in −0.5V steps. (b) I_{ds} as a function of V_{gs} (before and after annealing) for V_{ds}=-1V [12].

systems can be affected by the scattering of carriers in a number of ways. These include, scattering by other carriers, by surfaces, by interfacial roughness, by acoustic phonons, optical phonons, impurities and by plasmons [35].

Significant theoretical and experimental work involving electronic transport in CNTs has helped in distinguishing ballistic and diffusive modes of transport. However, for free-standing semiconductor NWs, experimental and theoretical consensus of carrier-scattering mechanisms that are most significant in single- and multi component coaxial semiconductor NWs is less clear. In some cases, carrier mobilities in SiNW FETs and g_m values have been reported to exceed those associated with conventional Si planar technology devices [36].

Although many studies pointed out that transport in nanoscale transistors is ballistic, in practice there is some sort of scattering in these devices. In reference [14], scattering mechanisms affecting the performance of SiNW FETs are studied. The Non Equilibrium Green's Function (NEGF) formalism within parabolic Effective Mass Approximation (EMA) and the coupled mode space approach is applied in the analysis of this device. In addition, various scattering mechanisms are analyzed, namely, the Surface-Roughness (SR), the Remote-Coulomb Scattering (RCS), and phonon scatterings. SR and RCS are investigated by using a non-perturbative approach, considering devices with specific random realizations of rough Si/SiO_2 interfaces and fixed-charge center distributions at the high-κ/SiO_2 interface. A general analysis is thus statistically carried out on a set of device samples. The impact of the SR and RCS on the transport properties of SiNW FETs was analyzed with special attention devoted to the effective mobility. Effective mobility is found to be an important performance metric also in the quasi-ballistic regime, showing findings in accordance with the main semi-classical models. Finally, a global analysis of the interplay of the different scattering mechanisms has been performed. This shows interesting results on the mobility trend for devices scaled down to 10 nm channel length [37]. Figure 2.6 shows the effective mobility versus overdrive voltage curve for ballistic and SR limited transport for the $5\times5nm^2$ and $7\times7nm^2$ section SiNW FET.

2.2.2 Operation Modes of SiNW FETs

The operation of NW FETs is similar to that of planar FETs and UTB FETs [38]. However due to its 2D confinement structure, transport characteristics in NW MOSFETs are different from those in planar and UTB MOSFETs. Also, NW FETs show some differences as compared to the conventional planar MOSFETs. Among these differences, the presence of ambipolar conduction in NW FETs is major one. This property is due to the fact that source and drain contacts are made

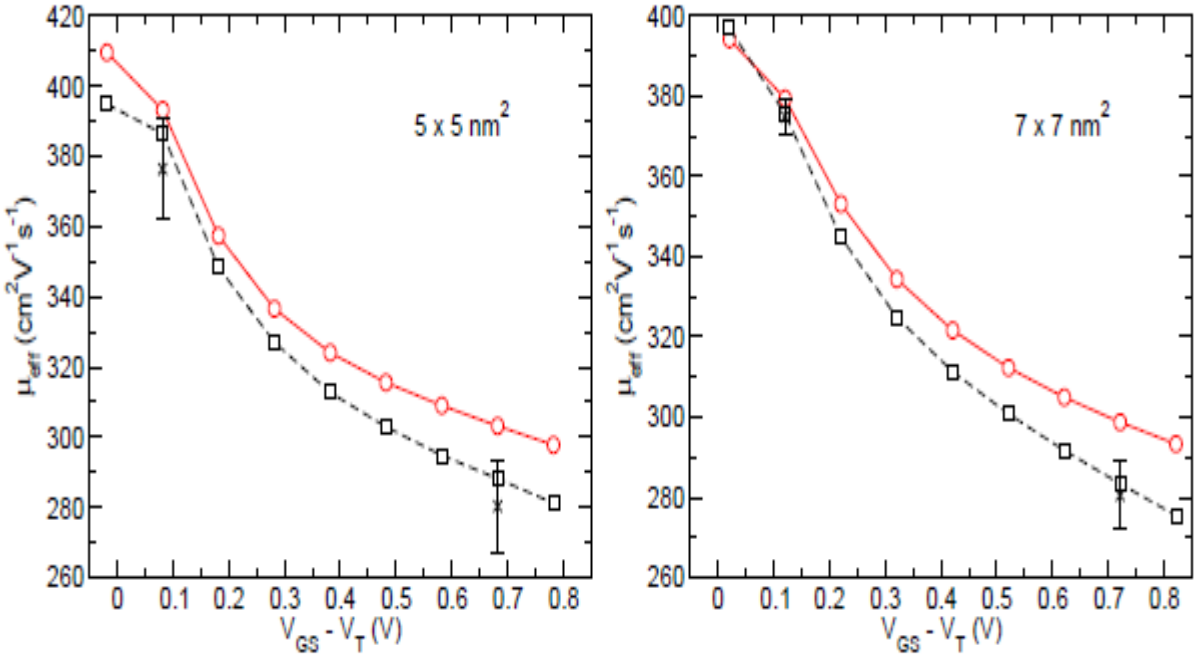


Figure 2.6 Ballistic mobility (circle) and SR–limited mobility (square) for a (left) 5 × 5 nm^2 and a (right) 7 × 7 nm^2 section wire [14].

from metals instead of degenerately doped semiconductors. Ambipolar behavior in FETs is defined as both n- and p-type conduction in a single device at the appropriate gate bias conditions [39]. Ambipolar conduction in n-SiNW FETs is shown in Figure 2.7. As we can see from this Figure, there is both p-type and n-type conduction in this device, depending on the bias applied to the gate voltage. With the application of negative gate bias (for $V_{gs}<0$), there is strong p-type conduction in the device and with zero gate bias ($V_{gs}=0V$) application, there is a weak p-type conduction. Finally for a positive gate bias ($V_{gs}>0$), n-type conduction is seen in the device [31].

Generally, there are two types of operation modes for SiNW FETs. These are the Junction FET (JFET) like operation and the MOSFET like operation [31]. In JFET like operation of NW FETs, the NW region is treated as a bulk volume of charge whereas in MOSFET like operation, the NW channel is treated as a thin sheet of charge. Figure 2.8a shows the JFET like operation of the SiNW FET. The MOSFET like operation is depicted in Figure 2.8b.

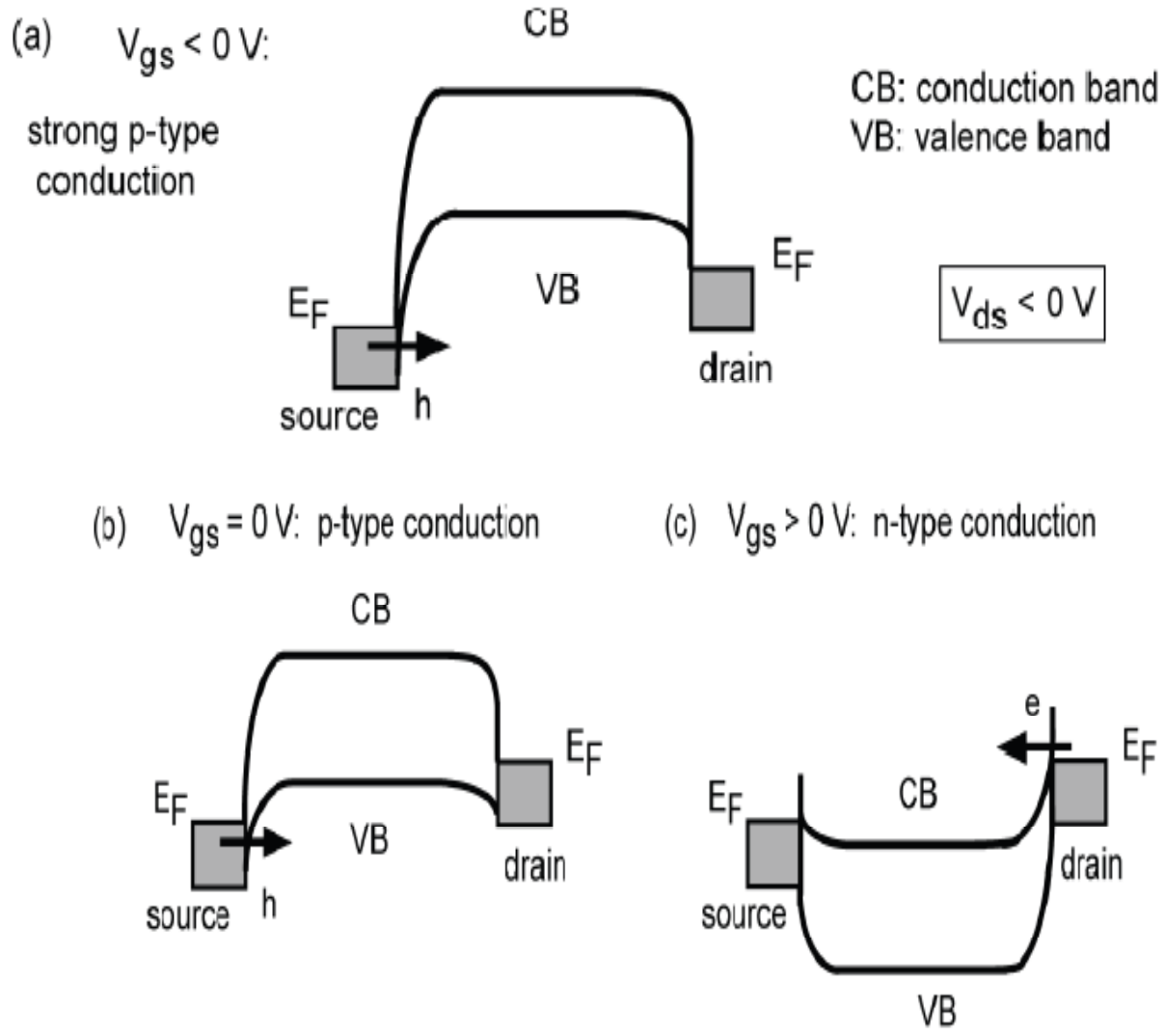


Figure 2.7 a schematic showing ambipolar conduction in n-SiNW FETs (a) strong p-type conduction for Vgs < 0 V. (b) p-type conduction at Vgs = 0 V. (c) n-type conduction for Vgs > 0 [31].

2.2.3 Review of Performance Evaluation of SiNW FETs

In order to assess the performance of SiNW FETs, we will compare the different parameters of this device with that of the planar MOSFETs. The simulation results of reference [40] are used for comparing the performance of SiNW FET with that of DG planar FET.

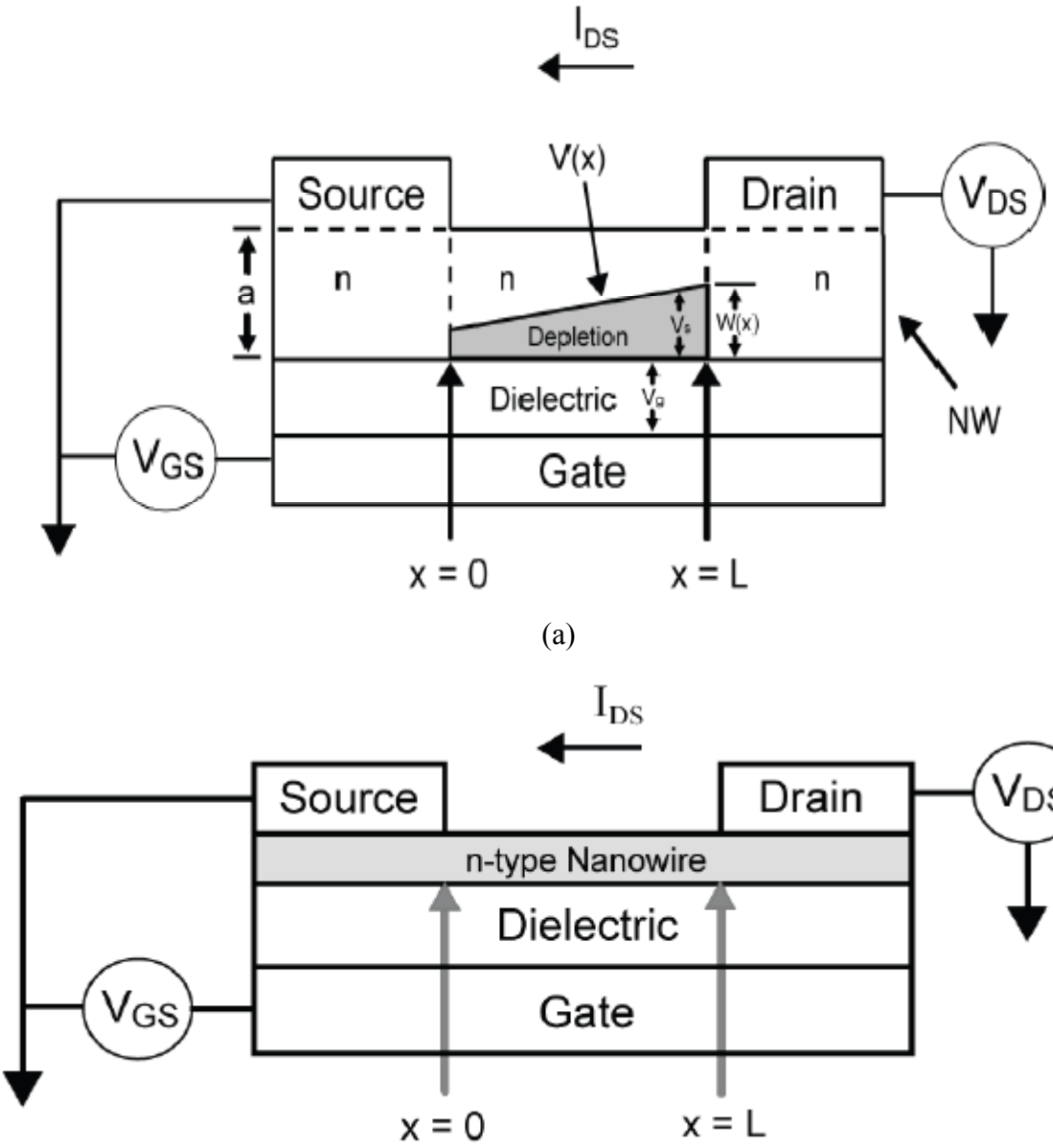


Figure 2.8(a) Diagram of a Bottom-Gated NW-based FET showing (a) JFET like operation of SiNW FETs (b) MOSFET like operation of SiNW FETs [31].

In reference [40], $I_{ds} - V_{gs}$ graph of SiNW FET and planar DG FET is simulated. The simulation is done assuming ballistic quantum transport using two different models. These models are the EMA model and the Nonparabolicity model (NP). In addition, there are simplifications of these models included in the simulation namely, the MC which is a model for increasing the conduction mass alone and ALPHA model for increasing the NP mass alone. Neglecting both effects yields the EMA

case while inclusion of both effects is still referred to as the NP case [40]. In this reference, simulation of the transfer characteristics is done for investigation of the impact of band structure effects on transfer characteristics of SiNW FET and planar FETs. However we use these simulation results for comparing the transfer characteristics and parameters of these two transistors.

The simulated NW FET has square GAA structure with a Si NW channel. The source and drain regions are both n-doped with a concentration of $N_D = 10^{20}cm^{-3}$ and the lengths are ls = ld = 10 nm. The gate contact surrounds the FET as shown in Figure 2.9(a) (GAA). Like wise, the planar FET considered is a DG structure as shown in Figure 2.9(b). Both transistors have a body thickness of t_c and an oxide thickness t_{ox}. For the calculation of Threshold Voltage (V_{th}), I_{on}, and SS the values $I_{off} = 10^{-7}$ A, $\Delta V_{on} = 0.2$ V, and $\Delta V_{SS} = 0.2$ V, respectively, are employed.

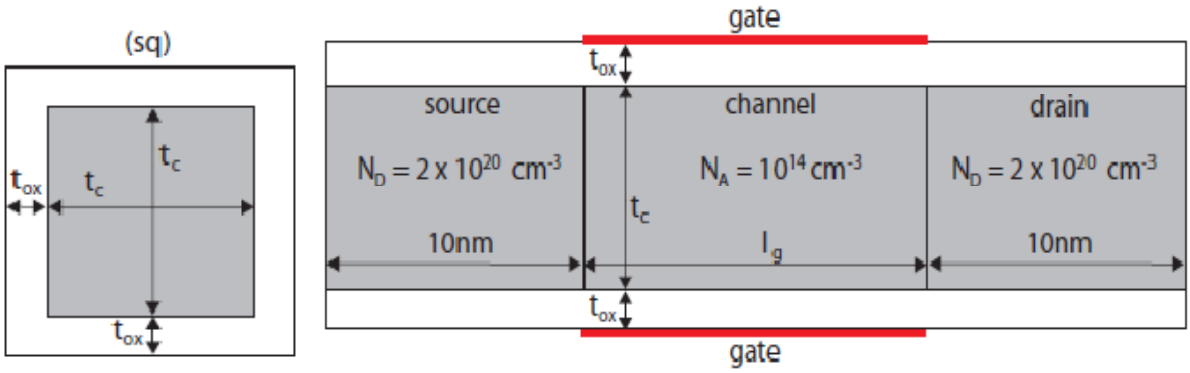


Figure 2.9(a) Profile specifications of the square (sq) NW and (b) DG FET with oxide thickness of tc = 0.6 nm [40].

In the analysis to follow in subsequent sections, the calculation will be based on the simulation results of the NP model. This is because it correctly estimates the subband energies and the conduction masses.

2.2.3.1 Comparison of the Off-state Current

The $I_{ds} - V_{gs}$ graphs of the SiNW and the planar transistor are given in Figure 2.10(a) and (b). The body thickness and NW diameter are taken to be equal to 2 nm and the gate length (l_g) is taken as 10 nm for both transistors. From the first graph (Figure 2.10(a)), Off-state current is found to be approximately 0.8525 pA/µm for the NW FET and from Figure 2.10(b) I_{off} is found to be approximately 0.415 nA/µm for the planar FET. From these results we can conclude that the Off-state current of the planar FET is greater by a factor of 1000. This result implies that NW FETs

have greater gate control than the planar FETs. This is because of the GAA structure of the NW FET compared to its planar counter part which has only a double gate.

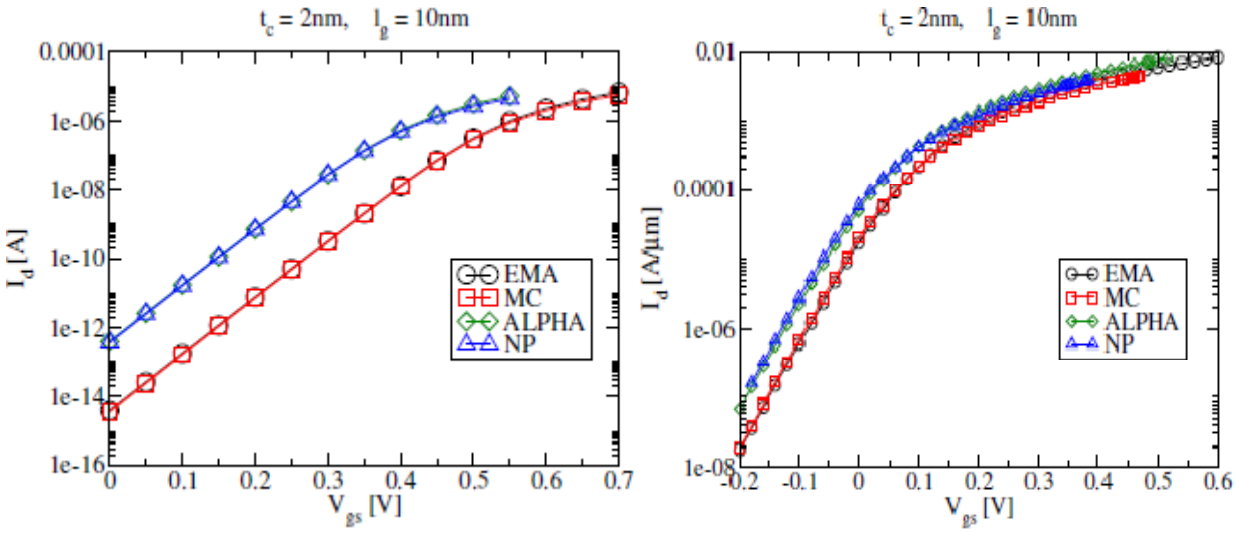


Figure 2.10 Transfer characteristics (sub threshold regime) of (a) sq NW transistor. (b) Planar FETs by various models [40].

2.2.3.2 Comparison of Subthreshold Slope

Figure 2.11(a) and (b) show the graph of SS versus t_C for a gate length of 10 nm for the NW and planar FETs respectively. From these graphs the SS is found as approximately 61.5 mV/dec for NW FET and 65 mV/dec for the planar FET at t_C of 2 nm. Similarly SS at t_C of 4 nm is found to be approximately 67.5 mV/dec and 77.5 mV/dec for the NW and the planar FETs respectively. From these values of SS we can see that the SS value of planar FETs is much higher than that of the NW FETs. In addition the SS value for the planar FET increases very rapidly as the channel thickness increases as compared to the NW FET.

2.2.3.3 Comparison of Threshold Voltage

Figure 2.12(a) and (b) shows the graph of v_{th} versus t_C for the NW FET and for the planar FET at a gate length of 10 nm. The v_{th} value for t_C of 2 nm is approximately 0.348 V for the NW FET and -0.058 V for the planar FET. Similarly, at t_C of 3 nm, the value of v_{th} is found to be approximately

0.097 V and -0.125 V for the NW and planar FETs respectively. Here again, we can deduce that the NW FET has very high gate control than that of the planar FET.

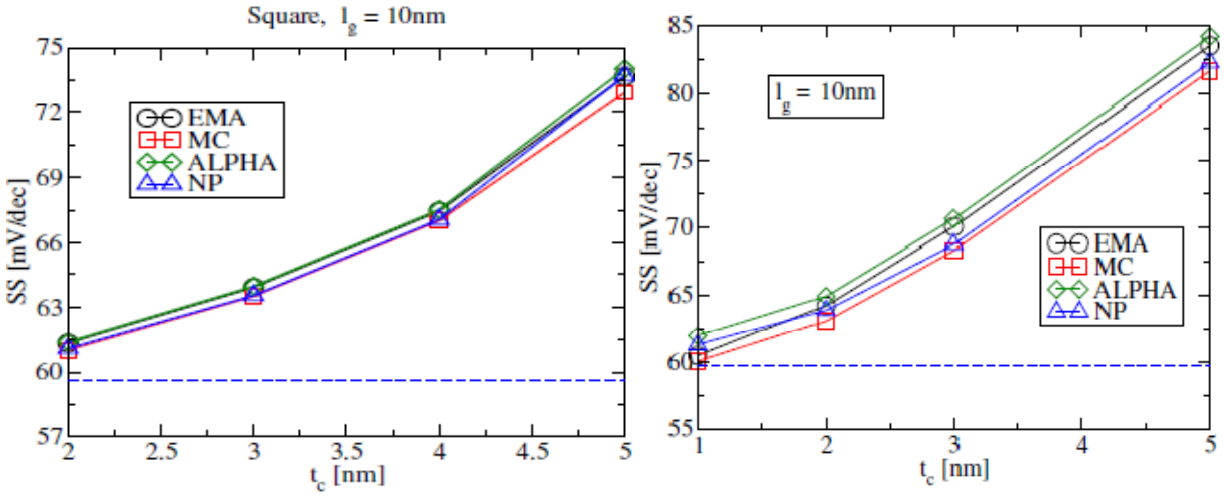


Figure 2.11 Subthreshold Slope versus body thickness of (a) NW FETs and (b) planar FETs [40].

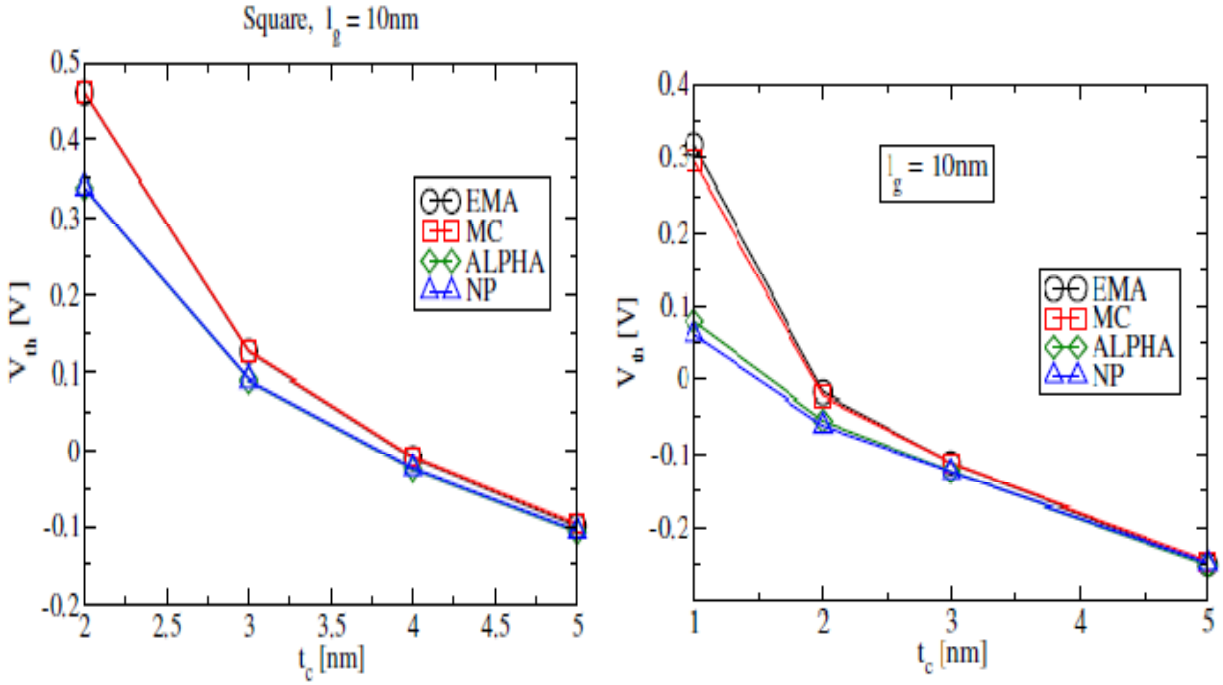


Figure 2.12 Threshold voltage versus body thickness of (a) NW FETs and (b) planar FETs [40].

Therefore, we can conclude that SiNW FETs have higher performance when compared to conventional planar FETs. The advantages of SiNW FETs over planar FETs are summarized in the following subsection.

2.2.4 Advantages of SiNW FETs Over Planar FETs

SiNW FETs have several advantages as the candidate of main stream CMOS devices for 2020s as shown in Figure 2.13.

First of all, the ability of the suppression of the short channel effects and thus, the suppression of the off-leakage current of SiNW FETs are expected to be very good, because of the gate surrounding configuration. Secondly, Si NW FETs are expected to have high on current because of the following 3 reasons [41].

I. The nature of quasi-1D conduction of thin NW with small freedom of the carrier scattering angle [42]; because of the small freedom of the carrier scattering, its conduction will be high.

II. The use of multi-quantum channels for the conduction; the band structure of SiNWs is quite different from that of the bulk and many conduction sub-bands appear near the lowest sub-band [43]. Those sub-bands contribute to the conduction as the gate voltage increase.

III. Multilayer NWs can be implemented easily by utilization of Si/Ge multi-layers as shown in Figure 2.13 [44]. For the fabrication, basically, today's conventional Si CMOS IC production process can be used almost as it is to fabricate SiNW FET, although process tuning kind of developments are necessary. This is a very big advantage for the production to minimize the risk and cost of the new process technology development. Furthermore, the number of SiNW FET fabrication process will be smaller than that of today's planar CMOS. It is assumed that no channel implantation including that of halo is necessary because of good SCEs control of the NW structure, assuming that threshold voltage control can be done by the work function control of gate stack. In some future, metal or silicide source/drain is assumed to be introduced into ultra-short channel SiNW FETs because of the necessity of abrupt junction, resulting in the further elimination of source/drain doping [41].

The advantages of SiNW FETs over planar FETs are summarized in Figure 2.14.

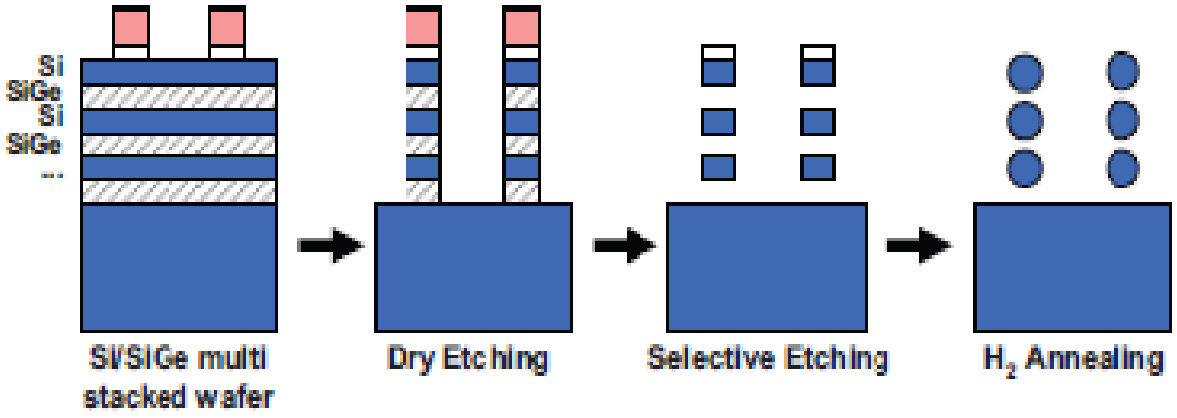


Figure 2.14 Fabrication of Multilayer NW [41]

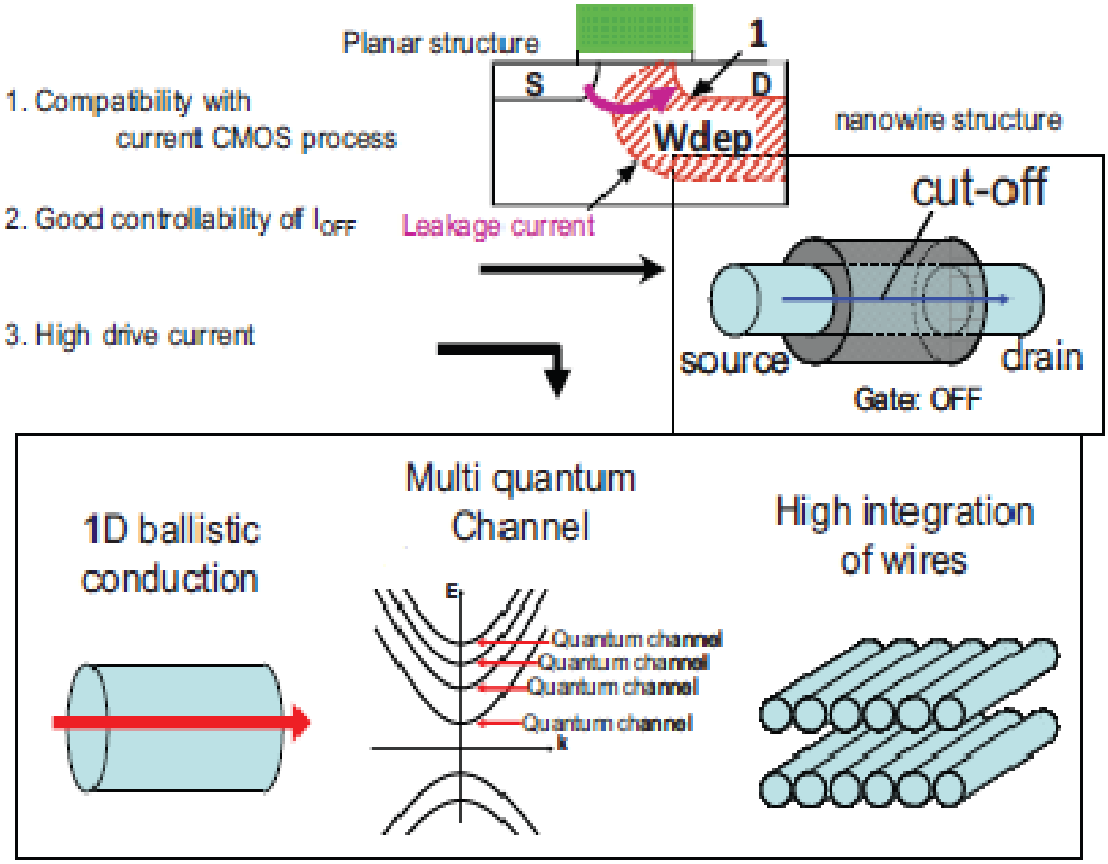


Figure 2.14 Advantages of SiNW FETs over Planar [41].

CHAPTER THREE : METHODOLOGY OF MODELING OF SiNW FET

In this chapter, the compact modeling for SiNW FETs is developed and described together with the theoretical back ground. The model is divided in to two parts, namely, a modeling approach which assumes ballistic transport and that assuming transport in the presence of scattering. The former part is developed based on Natori's theory of ballistic MOSFETs and modified to include two dimensional effects. The latter part is based on McKelvey's flux theory. We begin by describing the basic Natori's model for ballistic transport in the first section and proceed to the model derivation. In the second section, we will derive our model for transport in the presence of scattering.

3.1 Modeling of SiNW FET Assuming Ballistic Transport

This section describes an analytical compact modeling of ballistic SiNW FETs. The model is derived by extending an analytical approach proposed by Natori et al [45]. Before we go to the mathematical derivation of this model, let's describe Natori's theory of ballistic MOSFETs.

3.1.1 Natori's Theory of Ballistic MOSFETs

According to Natori's theory of ballistic MOSFETs, ballistic transport is a special kind of equilibrium. Each k-state is in equilibrium with the contact from which it was populated. Using this reasoning, one can compute the distribution function and any moment of it (e.g. carrier density, carrier velocity, etc.) at any location within the device. There are basically three conclusions drawn from Natori's theory of ballistic MOSFETs [46], these are:

For a ballistic MOSFET,

1) The carrier distribution function at the top of the source-channel barrier consists of two thermal equilibrium halves, one injected from the source and the other from the drain,

2) For an electro statically well-designed MOSFET, the total carrier density at the top of the barrier is maintained at an approximately constant value, and

3) The average velocity at the top of the barrier saturates at a limiting value.

These are the core theoretical derivations of Natori's theory of ballistic MOSFETs. The top of the barrier has a special significance in this model. This is because at that point the carrier and current population is divided in to two halves, the positive half and the negative halve. This makes the computation simpler by allowing the treatment of the equations in terms of directed moments. Directed moments are integrals over only the positive k-states or only the negative k-states. Figure 3.1 illustrates the concept of the directed moments. As we can see from this figure, the positive k-state is populated according the Fermi energy $E_{F1.}$ Similarly, the negative k-state is occupied by the drain Fermi energy, E_{F1}-$qV_{DS.}$ These concepts form the basis of the Natori's model and we will rely heavily on these concepts throughout our model derivation.

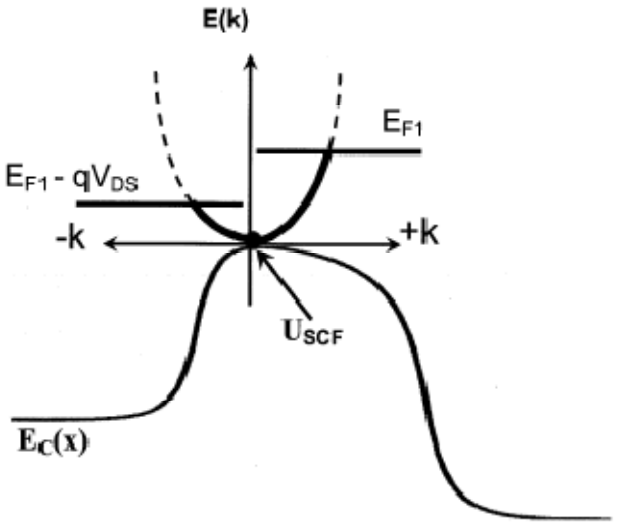


Figure 3.1 illustration of the k-states at T=0K and the definition of the directed moments [47].

3.1.2 Model Derivation

The model derivation begins by describing the different directed moments describing the ballistic transport of NW FETs. According to Natori's theory of ballistic MOSFETS, the directed moments to be evaluated in order to derive the important parameters of the SiNW FET are [46]:

1. The electron concentration at the top of the barrier, populated according to the source Fermi level , $n_L^+(0)$ given by:

$$n_L^+(0) = \frac{1}{L}\sum_{k>0} f_0\ (E_f) \qquad 3.1$$

2. The electron concentration at the top of the barrier, populated according to the drain Fermi level, $n_L^-(0)$ is given by:

$$n_L^-(0) = \frac{1}{L}\sum_{k<0} f_0\ (E_f - qV_D) \tag{3.2}$$

3. The positive directed current due to source injection, I^+, given by:

$$I^+ = \frac{1}{L}\sum_{k>0} qvf_0\ (E_f) = \mathrm{q}n_L^+(0)v^+(0) \tag{3.3}$$

4. The negative directed current due to drain injection, I^-, given by:

$$I^- = \frac{1}{L}\sum_{k<0} qvf_0\ (E_{f-}qV_D)\ \mathrm{q}n_L^-(0)v^-(0) \tag{3.4}$$

Assuming a simple parabolic energy band structure and also assuming that only on subband is occupied, the directed moments given in Equations 3.1 to 3.4 are evaluated to give [46]:

$$n_L^+(0) = \frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F) \tag{3.5}$$

$$n_L^-(0) = \frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F - U_D) \tag{3.6}$$

$$I^+ = \frac{qk_BT}{\pi hbar} F_0(\eta_F) \tag{3.7}$$

$$I^- = \frac{qk_BT}{\pi hbar} F_0(\eta_F - U_D) \tag{3.8}$$

Describing the positively populated electron concentration, $n_L^+(0)$, negative populated electron concentration, $n_L^-(0)$, the positive directed current, I^+ , and the negative directed current, I^- respectively.

Where:

$$\eta_F = \left(\frac{E_F - \varepsilon_1(0)}{k_BT}\right) \tag{3.9}$$

$$U_D = \frac{qV_D}{k_B T} \tag{3.10}$$

$$v_T = \sqrt{\frac{2k_B T}{\pi m^*}} \tag{3.11}$$

and N_{1D} is the 1D Effective DOS given by:

$$N_{1D} = \sqrt{\frac{2m^* k_B T}{\pi hbar^2}} \tag{3.12}$$

F_0 and $F_{-1/2}$ are the Fermi-Dirac integrals of 0 and -1/2 order respectively. The Fermi-Dirac integral of any order is generally defined as [48]:

$$F_j(\eta_F) = \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{\varepsilon^j d\varepsilon}{1 + exp\,(\varepsilon + \eta_F)} \tag{3.13}$$

Where, Γ is the gamma function. The Γ function is just the factorial when its argument is a positive integer [44], for an integer n,

$$\Gamma(\mathrm{n}) = (\mathrm{n}-1)! \tag{3.14}$$

Also

$$\Gamma\left(\frac{1}{2}\right) = \sqrt{\pi} \tag{3.15}$$

$$\Gamma(\mathrm{p}+1) = \mathrm{p}\Gamma(\mathrm{p}) \tag{3.16}$$

Throughout this chapter, we will use these equations for the derivation of the current and charge density equations of SiNW FET. Assuming 1D electrostatics and neglecting 2D electrostatics, the gate voltage is the sum of the surface potential and the voltage drop across the oxide:

$$V_G^{'} = \psi_S - \frac{Q}{C_{ox}} \tag{3.17}$$

Substituting the expressions for the surface potential and the charge density at the top of the barrier Equation 3.17 becomes:

$$V_G = \frac{\varepsilon_1(0)}{q} - \frac{qn_L}{C_{ox}} \qquad 3.18$$

After solving Equation 3.18 for $\boldsymbol{\varepsilon_1(0)}$ we get:

$$\varepsilon_1(0) = qV_G + \frac{q^2 n_L}{C_{\text{ox}}} \qquad 3.19$$

3.1.2.1 Modeling of the Gate Capacitance

Before further continue the derivation, the expression for the oxide capacitance, C_{ox}, is derived first. The SiNW FET structure we will consider is shown in Figure 3.2. It is a FET having a cylindrical NW as a channel. This configuration gives the highest performance of the NW transistor because of the strong control of SCEs. Because the NW transistor has a cylindrical cross section, its capacitance can no longer be calculated using a simple parallel-plate model.

The capacitance C of the capacitor is defined, in general, as the ratio of the magnitude of the charge on one of the plates to the potential difference between them [49]; that is,

$$C = \frac{Q}{V} = \frac{\varepsilon \oint E.dS}{\int E.dL} \qquad 3.20$$

Using Equation 3.20, C can be obtained for any given two-conductor capacitance by following either of these methods [50]:

1. Assuming Q and determining V in terms of Q (involving Gauss's law)

2. Assuming V and determining Q in terms of V (involving solving Laplace's Equation)

The former method is used here and it involves taking the following steps:

1. Choose a suitable coordinate system.

2. Let the two conducting plates carry charges + Q and - Q.

3. Determine E using Coulomb's or Gauss's law and find V from $V = -\int \mathrm{E} \bullet \mathrm{d}\,l$ The negative sign may be ignored in this case because we are interested in the absolute value of V.

4. Finally, obtain C from C = Q/V.

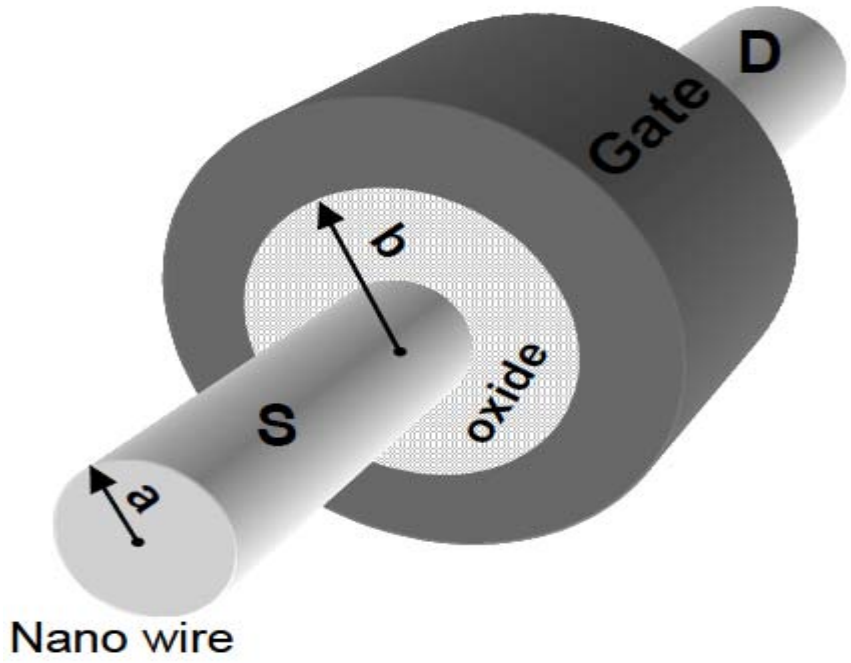


Figure 3.2 Illustration of a SiNW FET; the gate stack is wrapped around the semiconductor NW; a is the radius of the NW [49].

Considering Figure 3.3, the inversion charge in the NW can be approximated by a charge sheet on the outer surface of the wire. The charge on the gate is on the inner wall of the gate electrode. The capacitance can be obtained by calculating the voltage drop across the gate oxide [50].

The charge per unit length at the surface of the wire is given by:

$$Q = \varepsilon \oint E.dS = \varepsilon E_{\rho} 2\pi\rho \qquad 3.21$$

Where, for an infinite line charge if we apply Gauss's law to an arbitrary length l of the line:

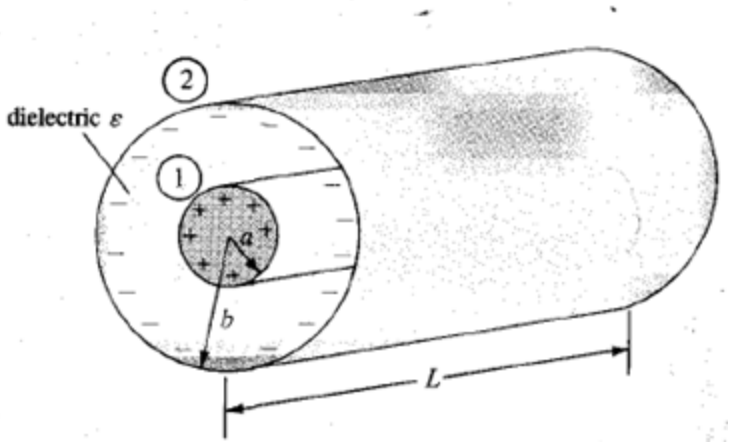


Figure 3.3 A Coaxial Capacitor [50].

$$\rho_l l = Q = \oint D.dS = D_\rho \oint dS = D_\rho 2\pi\rho l \qquad 3.22$$

where, ρ is the radius of the NW and $\oint dS = 2\pi\rho l$ is the surface area of the Gaussian surface, we obtain the electric field as:

$$E = \frac{Q}{2\pi\rho l} a_\rho \qquad 3.23$$

Neglecting flux fringing at the cylinder ends,

$$V = -\int_2^1 E.dl = -\int_b^a [\frac{Q}{2\pi\varepsilon\rho L} a_\rho].d\rho\, a_\rho$$

$$\mathrm{V} = \frac{Q}{2\pi\varepsilon L} ln\frac{a}{b} \qquad 3.24$$

Thus the capacitance of the cylindrical NW is given by:

$$C = \frac{Q}{V} = \frac{2\pi\varepsilon L}{ln\frac{b}{a}} \qquad 3.25$$

Where, a is the radius of the NW and b is given by: b=a + t_{ox}. Where, t_{ox} is the thickness of the insulator.

Finally, the capacitance per unit length of the NW is given by:

$$\frac{C}{L} = \frac{2\pi\varepsilon}{ln\frac{b}{a}} \tag{3.26}$$

Equation 3.26 indicates the effective gate capacitance of the NW transistor is a function of the NW radius as well as the gate oxide thickness. This relationship can be exploited to reduce the effective gate oxide thickness without using higher k dielectric.

Having derived the capacitance of the insulator for the cylindrical NW FET, let's proceed to the derivation for the other parameters.

Since $\boldsymbol{\eta_F}$, defined in Equation 3.9, enters in to the equation of charge and current, its expression is derived here.

Rearranging Equation 4.9, we get the energy for the first subband, $\varepsilon_1(0)$, as:

$$\varepsilon_1(0) = E_F - \eta_F * k_B T \tag{3.27}$$

Substituting the value of $\varepsilon_1(0)$ from Equation 3.19 and assuming 1D electrostatics $\boldsymbol{\eta_F}$ is given by:

$$\eta_F = \frac{E_F - qV_G}{k_B T} - \frac{q^2 n_L(0)}{k_B T C_{ins}} \tag{3.28}$$

3.1.2.2 Modeling of the Drain Current

In order to derive equation for the current, we use the directed moments derived in Equation 3.1-Equation 3.4 and the various equations derived in the previous section.

The drain current is the difference between the negative and positive going currents, $\boldsymbol{I^+}$ and $\boldsymbol{I^-}$ respectively. Therefore, the drain current for a SiNW FET is found using Equations 3.7 and 3.8 as,

$$I_D = I^+ - I^- \tag{3.29}$$

$$I_D = \frac{2qk_BT}{h}\{F_0(\eta_F) - F_0(\eta_F - U_D)\} \tag{3.30a}$$

$$I_D = I_0\{F_0(\eta_F) - F_0(\eta_F - U_D)\} \quad 3.30b$$

Where

$$I_0 = \frac{2qk_BT}{h} \quad 3.30c$$

In order to find the drain current, Equations 3.28 and 3.30 must be solved iteratively until convergence is achieved.

Note that Equation 3.28 is derived by only taking the contribution of the gate control. However, in order to model the real device performance 2D electrostatic effects must be included. A capacitive model for inclusion of 2D electrostatic effects in short channel MOSFETs is shown in Figure 3.4.

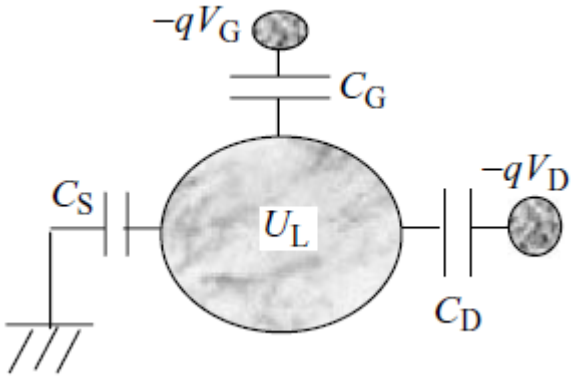


Figure 3.4 A Simple Capacitive Model for inclusion of 2D electrostatic effects [39].

Inclusion of Two Dimensional Effects

In the derivations of model Equations so far, only the gate electrode is assumed to control the electrostatics, neglecting the contributions of the source and drain. However, 2D electrostatics is an important factor for short channel MOSFETs [2], so we seek a way to extend our analytical model to include 2D electrostatics. The potential at the top of the barrier is controlled, in general, by all three electrodes. We solve for the potential at the top of the barrier by superposition. First, we

ignore the mobile charge to calculate the Laplace solution from voltage division among the capacitors as [39]:

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \qquad 3.31a$$

Where,

$\alpha_G = \frac{C_G}{C_\Sigma}, \alpha_D = \frac{C_D}{C_\Sigma}, \alpha_S = \frac{C_S}{C_\Sigma}$, and $C_\Sigma = C_G + C_D + C_S$

Note that C_G, C_S, and C_D refer to the three capacitors that describe the electrostatics control of the three electrodes. The first one is just $C_G = C_{ox}$, and C_D is chosen to reproduce the measured DIBL or output conductance (g_d) of the transistor.

The next step is to ground the three terminals and compute the potential at the top of the barrier due to the mobile charge as:

$$U_p = \frac{q^2}{C_\Sigma} n_L(0) \qquad 3.32$$

Finally, the complete solution,

$$\varepsilon_1(0) = U_L + U_p = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + U_C n_L(0) \qquad 3.33$$

is the sum of the Laplace solution and the charging energy and can be recognized as a generalization of Equation 3.19. In practice, E_F is set to give the correct off-current, α_G to get the correct gate control, and α_D to produce the correct DIBL.

Finally substituting Equation 3.33 into Equation 3.28, the Equation for $\boldsymbol{\eta_F}$ is found to be:

$$\eta_F = \frac{E_F}{k_B T} - \frac{\varepsilon_1(0)}{k_B T} \qquad 3.34a$$

$$\eta_F = \frac{1}{k_B T}\{E_F + q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) - U_C n_L(0)\} \qquad 3.34b$$

Therefore Equation 3.30 and the Equation for $\boldsymbol{\eta_F}$ are calculated to find the drain current of the NW FET.

3.1.2.3 Modeling of the Charge Density

In order to calculate the charge density at the top of the barrier, we add the contributions of the positive and the negative halves. Therefore the electron concentration at the top of the barrier is given by, using Equations 3.5 and 3.6:

$$n_L(0) = n_L^+(0) + n_L^-(0) - N_0 \qquad 3.35a$$

$$n_L(0) = \frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F) + \frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F - U_D) - N_{1D} F_{-\frac{1}{2}}\left(\frac{E_F}{k_B T}\right) \qquad 3.35b$$

Where,

$$N_0 = N_{1D} F_{-\frac{1}{2}}\left(\frac{E_F}{k_B T}\right) \qquad 3.35c$$

is the electron concentration at the top of the barrier in the neutral device.

The charge density at the top of the barrier is found by multiplying Equation 3.35b by the electron charge:

$$Q(0) = q n_L(0) \qquad 3.36a$$

$$Q(0) = q\left\{\frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F) + \frac{N_{1D}}{2} F_{-\frac{1}{2}}(\eta_F - U_D) - N_{1D} F_{-\frac{1}{2}}\left(\frac{E_F}{k_B T}\right)\right\} \qquad 3.36b$$

Finally, similar to the evaluation of current, the charge density for the NW FET can be evaluated by iteratively solving Equation 3.34 and 3.36, until convergence is achieved.

3.2 Modeling of SiNW FET in the Presence of Scattering

In this section, the modeling of SiNW FET is derived assuming that the transport is accompanied by various scattering events. The model is based on McKelvey's flux method. In reference [51], the model is done for a DG MOSFET assuming 2D transport. We modify this model to be suitable for 1D transport since the transport in SiNW FETs is basically 1D.

3.2.1 McKelvey's Flux Method

McKelvey's flux method captures the essential physics of carrier transport in transistors and has been previously used for thin-base diodes and bipolar transistors [52]. Conventional transport models are based on the net current, but McKelvey's flux method decomposes the current into directed fluxes traveling in the positive and negative directions [51]. Similar to Natori's model, the McKelvey's flux method evaluates current and charge at the top of the barrier as shown in Figure 3.5. Here the top of the barrier is defined as the beginning of the channel.

3.2.2 Model Derivation

In this subsection the model derivation of the drain current and the charge at the top of the barrier is derived for the SiNW FET in the presence of scattering.

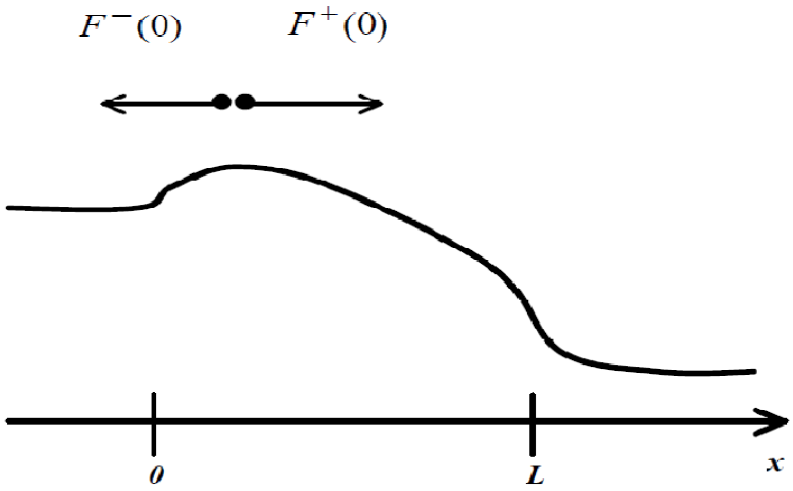


Figure 3.5 Positive and Negative going fluxes at the top of the barrier [51].

3.2.2.1 Modeling of the Current

As we can see from Figure 3.5, the positive directed flux, $\boldsymbol{F^+(0)}$, due to source injection and the negative directed flux, $\boldsymbol{F^-(0)}$, due to drain injection form the basis for our model derivation. The source injected flux, $\boldsymbol{F^+(0)}$, and the charge density in this flux, $n_0^+(0)$, can be expressed as:

$$F^+(0) = N_{1D} v_T F_0(\eta_F) \qquad 3.37$$

and

$$n_0^+(0) = N_{1D} F_{-\frac{1}{2}}(\eta_F) \tag{3.38}$$

The negative going flux, $\boldsymbol{F^-(0)}$, at the source end is composed of two components. The first component is the fraction of $\boldsymbol{F^+(0)}$ that is backscattered from the channel. The second component is the fraction due to carrier injection from drain. In the case of ballistic transport, the latter part and the charge density in it can be expressed as:

$$F_b^-(0) = N_{1D} v_T F_0(\eta_F - U_D) \tag{3.39}$$

and

$$n_b^-(0) = N_{1D} F_0(\eta_F - U_D) \tag{3.40}$$

Where $\boldsymbol{v_T}$ is the non degenerate thermal velocity given by:

$$v_T = \sqrt{\frac{2k_B T}{m_t \pi}} \tag{3.41}$$

The presence of scattering, in the McKelvey's flux treatment, is mainly described by the backscattering coefficient, r, a real number between 0 and 1. It quantifies various scattering events occurring in the device. Basically there are two different backscattering coefficients namely, the backscattering coefficient for source injected carriers, $\boldsymbol{r_{SD}}$ and that for drain injected carriers,$\boldsymbol{r_{DS}}$. The transmitted drain flux at x = 0 (in Figure 4.4) rapidly approaches zero as drain bias exceeds few k_BT/q, and so its contribution to the total current is not significant. Therefore, though in general, the backscattering coefficients $\boldsymbol{r_{SD}}$and $\boldsymbol{r_{DS}}$ are different, we take the backscattering coefficient, r, to be same for the two oppositely directed fluxes. When scattering is present, therefore, $F^-(0)$ can be expressed as [47]:

$$F^-(0) = rF^+(0) + (1-r)F_b^-(0) \tag{3.42}$$

Combining Equations 3.37, 3.39 and 3.42, we get:

$$\frac{F^-(0)}{F^+(0)} = r + (1-r)\frac{F_0(\eta_F - U_D)}{F_0(\eta_F)} \tag{3.43}$$

According to McKelvey's flux theory, the current injected at the top of the barrier is given by the expression:

$$I_{DS} = q\{F^+(0) - F^-(0)\} \tag{3.44a}$$

$$I_{DS} = qF^+(0)\left\{1 - \frac{F^-(0)}{F^+(0)}\right\} \tag{3.44b}$$

Substituting Equations 3.37, 3.39 and 3.6 into Equation 3.7b, we finally obtain an expression for the drain current of the device in the presence of scattering as:

$$I_{DS} = qN_{1D}v_T F_0(\eta_F)\left\{(1-r) + (1-r)\frac{F_0(\eta_F - U_D)}{F_0(\eta_F)}\right\} \tag{3.45a}$$

$$I_{DS} = qN_{1D}v_T F_0(\eta_F)(1-r)\left\{1 + \frac{F_0(\eta_F - U_D)}{F_0(\eta_F)}\right\} \tag{3.45b}$$

3.2.2.2 Modeling of the Charge Density

The electron concentration, n(0), at x = 0 (in Figure 3.5) is the sum of charges in the opposite-going fluxes at that point, i.e.,

$$n(0) = n^+(0) + n^-(0) \tag{3.46}$$

By rearranging and equating Equations 3.37 and 3.38, we get an expression for the degenerate velocity of the positive going fluxes as:

$$v_T^+ = v_T\frac{F_0(\eta_F)}{F_{-1/2}(\eta_F)} \tag{3.47}$$

Similarly, from Equations 3.39 and 3.40 we get an expression for degenerate velocity of the negative going flux as:

$$v_T^- = v_T \frac{F_0(\eta_F - U_D)}{F_{-1/2}(\eta_F - U_D)} \tag{3.48}$$

Assuming near equilibrium conditions at the top of the barrier, v_T^+ and v_T^- are assumed to be equal. That is, $v_T^+ = v_T^- = v_T$.

Now, dividing Equation 3.42 by v_T, we get:

$$\frac{F^-(0)}{v_T} = \frac{F^+(0)}{v_T} + (1-r)\frac{F_b^-(0)}{v_T} \tag{3.49}$$

This Equation is equivalent to:

$$n^-(0) = rn^+(0) + (1-r)n_b^-(0) \tag{3.50}$$

Substituting the Equations for $n^+(0)$ and $n_b^-(0)$ and after some rearrangement we get the expression for $n_b^-(0)$ as:

$$n_b^-(0) = n^+(0)\frac{F_{-\frac{1}{2}}(\eta_F - U_D)}{F_{-\frac{1}{2}}(\eta_F)} \tag{3.51}$$

Substituting this into Equation 3.46 and after some rearrangement, we get the expression for the electron density as:

$$n(0) = N_{1D}F_{-\frac{1}{2}}(\eta_F)(1-r)\left\{1 + \left(\frac{1-r}{1+r}\right)\frac{F_{-\frac{1}{2}}(\eta_F - U_D)}{F_{-\frac{1}{2}}(\eta_F)}\right\} \tag{3.52}$$

Finally, the Equation for the charge density at the top of the barrier for the SiNW FET is obtained as:

$$Q(0) = qN_{1D}F_{-\frac{1}{2}}(\eta_F)(1-r)\left\{1 + \left(\frac{1-r}{1+r}\right)\frac{F_{-\frac{1}{2}}(\eta_F - U_D)}{F_{-\frac{1}{2}}(\eta_F)}\right\} \tag{3.53}$$

CHAPTER FOUR : SIMULATION RESULTS AND DISCUSSION

Due to the surrounding gate configuration, the cylindrical NW FET described in the previous sections has the greatest gate control when compared to other gate configurations. Therefore, a cylindrical NW FET is chosen in the simulation.

The main parameters of FETs are carrier mobility, transconductance, subthreshold slope (SS), on-state current (I_{on}), off-state current (I_{off}), threshold voltage (V_{th}), gate length (L_G) etc. The higher the carrier mobility and the shorter the gate length, the higher is the on-state current and thus the rapider is the device speed. The values of I_{off} and V_{th} reveal the energy dissipation of the devices. Higher I_{on}/I_{off} ratio would be better for the FETs. Increase of transconductance and decrease of subthreshold slope mean gate voltage offers more effective control on FETs. Therefore, in this chapter these important parameters are calculated and the output and transfer characteristic graphs are generated. In addition, to benchmark the model developed in the previous chapter, its simulation results are compared with that of the experimental results reported in literature.

In the first section of this chapter, our simulation results are compared with the experimentally reported results. This helps to benchmark our simulation results and hence to prove the validity of the developed model. In the second section, our simulation results are compared with the numerical simulation results from NanoHub reported in [53]. Finally, the effect of varying the NW diameter and gate oxide thickness on the performance of the device is discussed in the third section of this chapter.

4.1 Benchmarking the Developed Model

The developed model is benchmarked both against the actual SiNW FET device experimental results and the numerical simulation results. In the first sub section of this section, the simulation results of the developed model are compared with the device experimental results. In the second sub section, the simulation results of the developed model are compared with that of the numerical simulation results.

4.1.1 The Device Structure

In the simulation, the NW transistor structure that we studied in the previous chapter is considered as shown in Figure 4.1. It is a cylindrical gate all around structure having an n-doped channel and a radius of a. The source and drain are kept at uniform high n-type doping level of $2x10^{20}$ /cm^3. The diameter of the NW and the gate oxide thickness are taken to be 10 nm and 2 nm respectively. In addition, the gate material is assumed to be a mid gap material having a gate work function of 4.4 eV and the gate length is taken to be 30 nm. For all simulations, the temperature is kept at 300K, the drain voltage is varied between 0.05 V and 1 V and the transverse effective mass is assumed. Also, to get the upper performance limit of our simulated device, the simulation is done assuming ballistic transport. In addition, the value of the gate control parameter is taken to be 0.88 and that of the drain control parameter 0.035.

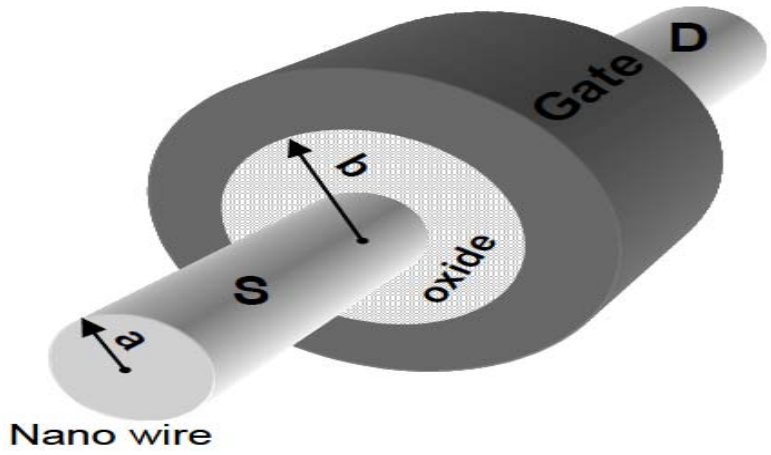


Figure 4.1 Illustration of a SiNW FET. The gate stack is wrapped around the semiconductor NW; a is the radius of the NW [49].

The cross section of the experimental SiNW FET is shown in Figure 4.2. It has an n-doped channel having a diameter of 5 nm and an oxide thickness of 2 nm. The device was reported by the Samsung group in the International Electron Devices Meeting (IEDM), 2005. TiN, which has a mid gap work function, was used as a gate material [53].

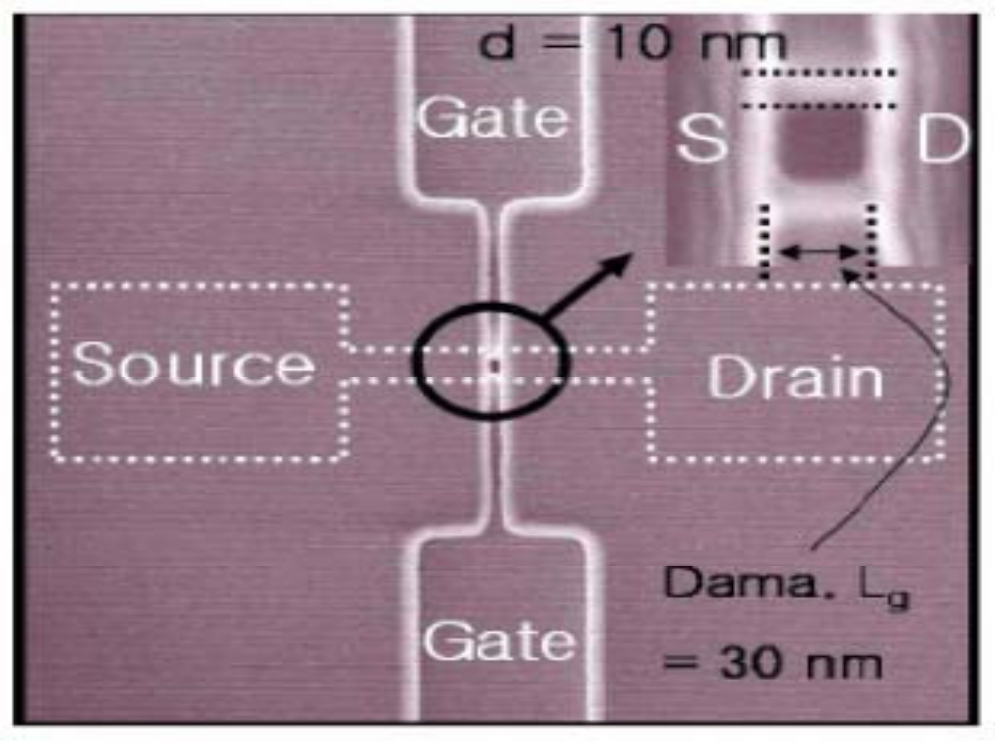
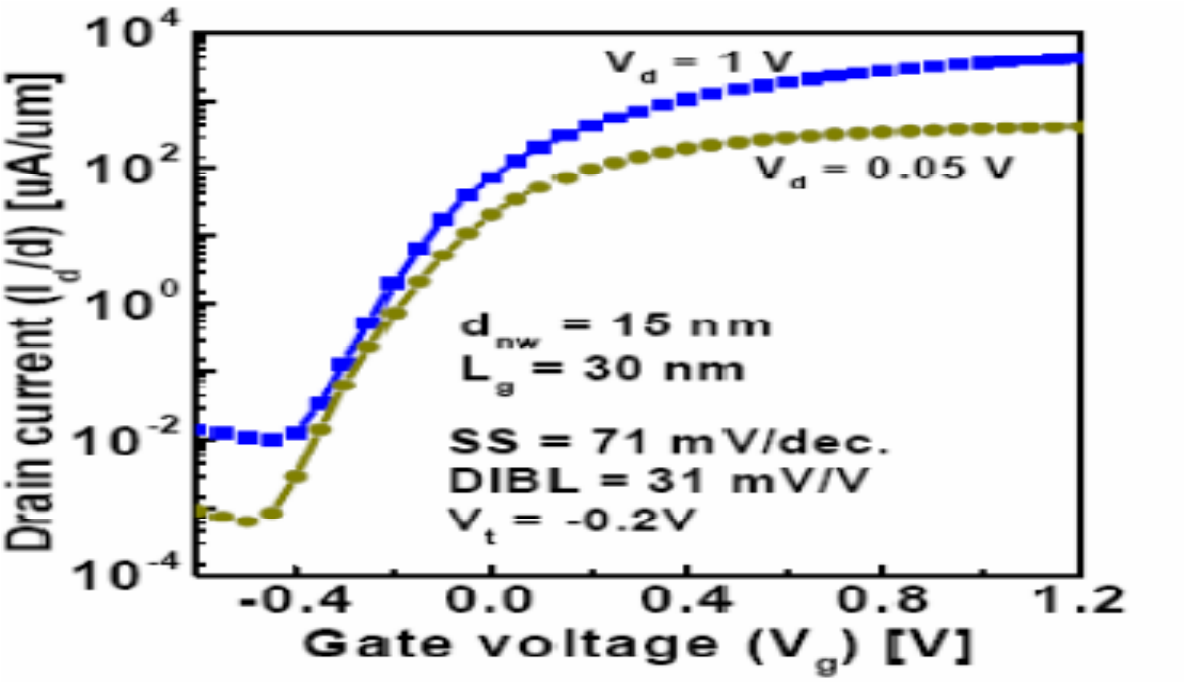


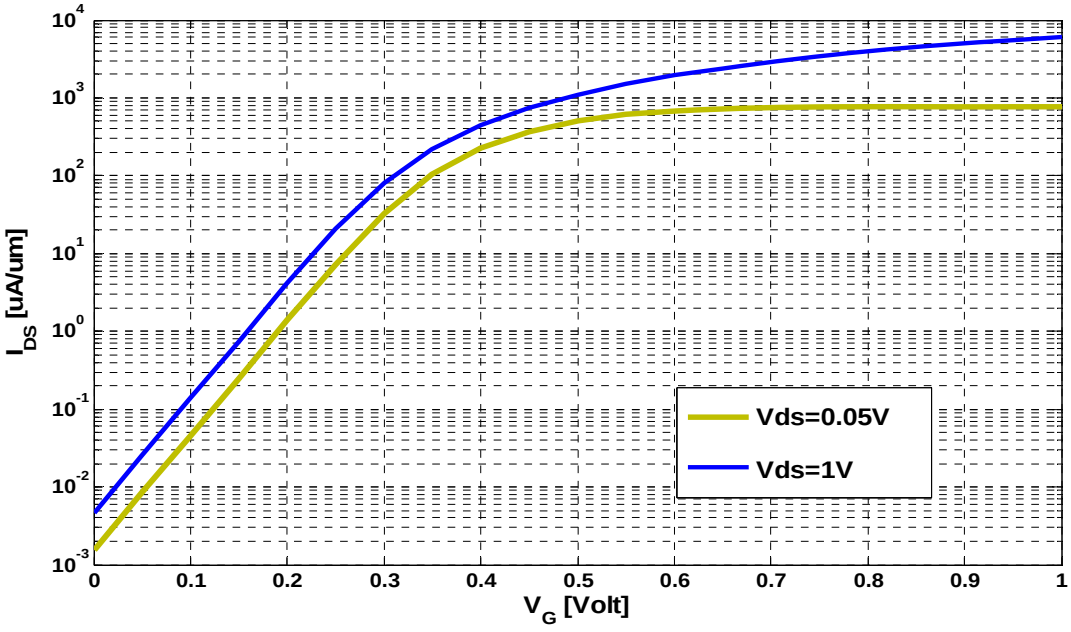
Figure 4.2 Fabricated 30 nm long Si GAA NW FET [53].

4.1.2 Comparison with Experimental Device Results

The transfer characteristics, log I_{dS} - V_{gS}, of the fabricated and simulated SiNW FET are depicted in Figures 4.3(a) and (b) respectively. In the simulation, the gate supply voltage, V_G, is varied from 0V to 1V in steps of 0.1 while keeping the drain supply voltage, V_D, at fixed voltages of 0.05V and 1V. Note that the current have been normalized to the NW diameter, which is in this case 10 nm. The value of I_{off} and the SS are derived from these transfer characteristics. The value of the Off-state current is taken to be the drain current at the minimum gate and at the maximum drain voltages (V_G=0V and V_D=1V) taken in the simulation.



(a)

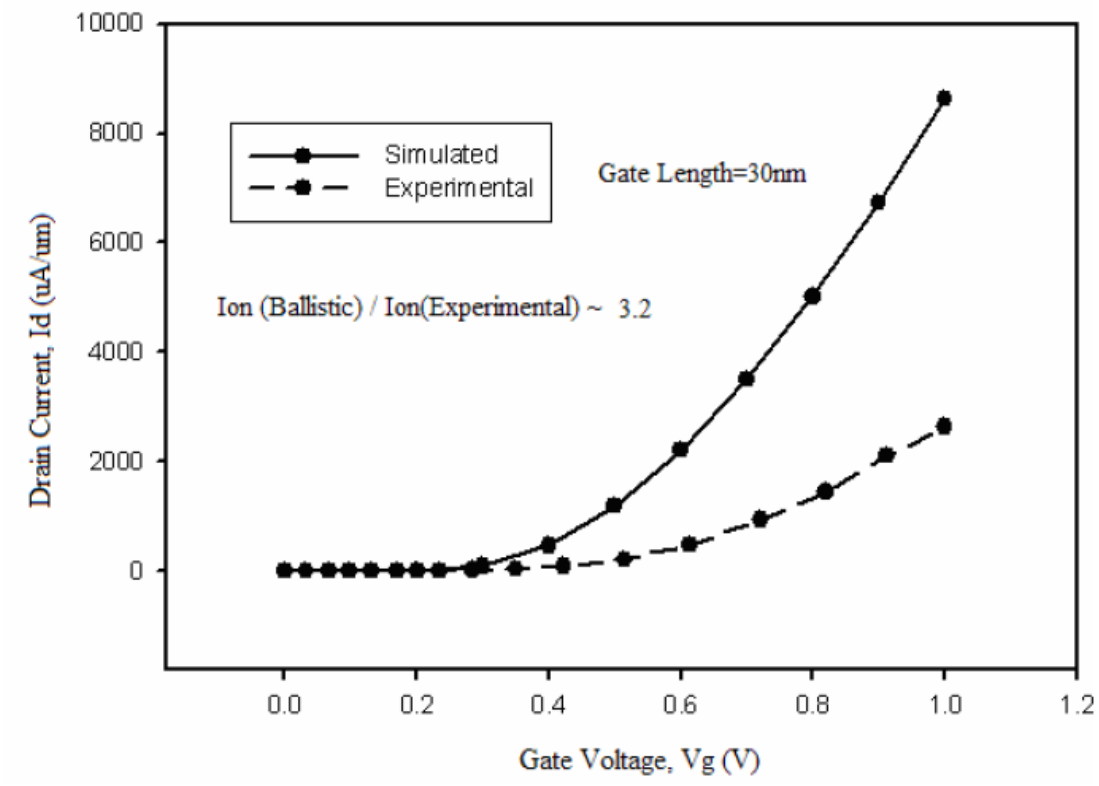


(b)

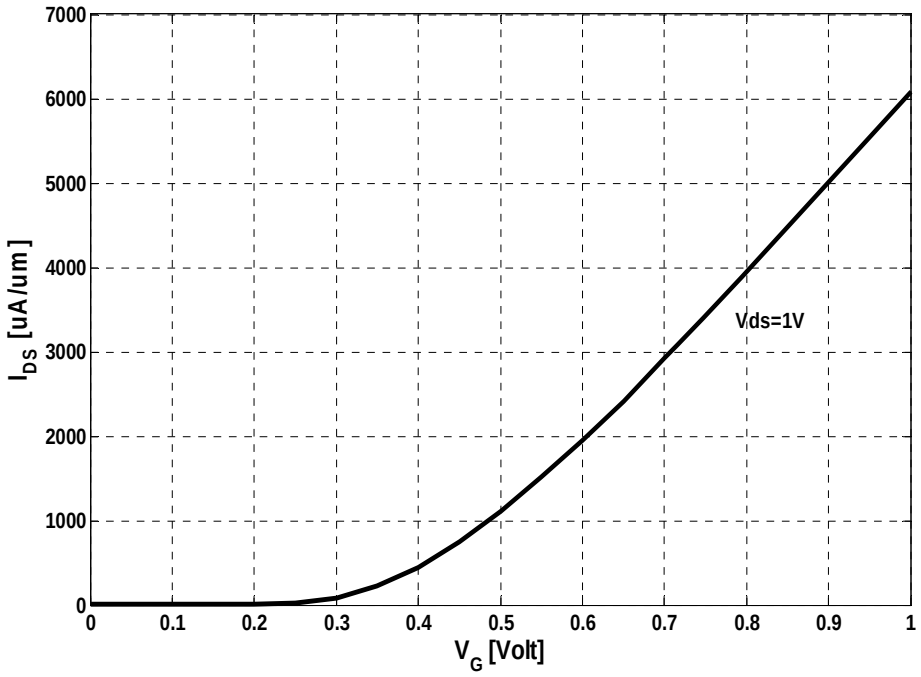
Figure 4.3 Transfer characteristics for (a) fabricated GAA SiNW FET [53] and (b) simulated SiNW FET.

The value of the subthreshold slope obtained from the compact model simulation is 67.75 mV/dec while that of the experimental device's SS is 71 mV/dec. The better SS found from the compact model simulation result can be attributed to the ideal wrap around gate structure assumed in the simulation. In addition, the value of I_{off} is calculated at a gate and drain voltages of 0 V and 1 V respectively and is calculated from the compact model to be 4.669 nA/nm and 3.1 nA/nm from the experimental result. As expected this value is attributed, again, to the ideal wrap around gate structure assumed for our simulated device.

The linear transfer characteristics, I_{ds} - V_{ds} graph found from the experimental result and our simulation are shown in Figure 4.4(a) and (b) respectively. From these graphs the values of On-state current and DIBL are calculated. The value of I_{on} is taken to be the drain current at the maximum gate and drain bias which are V_{gs}=1V and V_{ds}=1V.



(a)



(b)

Figure 4.4 The linear I_{ds} - V_{gs} curve of (a) the experimental [53] (b) simulated SiNW FET.

From these graphs, the value of I_{on} is calculated for the simulated device to be 6.081 mA/µm compared to that of the recorded experimental value which is 2.64 mA/µm. This discrepancy between the results of the experimental and the simulated device is due to the assumption of ballistic transport in the simulated device which over estimates the On-state current. The value of DIBL calculated from our simulation results is 34.39 mV/V while the DIBL value calculated from the fabricated device experimental results is 13 mV/V. From these results, we can see that there is a good agreement between the results of the simulated and the experimental device in DIBL value. All the results obtained in this section are summarized in Table 4.1.

Table 4.1 Comparison between the simulated and the experimental device results.

	Simulated SiNW FET	Experimental SiNW FET
Gate length	30nm	30nm
Nano wire diameter	10nm	10nm
Oxide thickness	2nm	2nm
ON current	6.081mA/µm	2.64mA/µm
OFF current	4.669nA/ µm	3.1nA/ µm
ON/OFF ratio	$\sim 10^6$	$\sim 10^6$
DIBL	34.39mV/V	13mV/V
Subthreshold Slope	67.75mV/dec	71mV/dec

4.1.3 Comparison with the Numerical Simulation Results

To further see the accuracy of the developed model, the simulation results of our model are compared with that of the numerical one. The simulation software for the numerical device modeling is based on the work done by Jing Wang et al. and his colleagues at Purdue, named NW. The tool (NW) is a 3D self-consistent, quantum, SiNW simulator based on the EMA [54]. For all simulations, MATLAB software has been used and ballistic transport is assumed.

4.1.3.1 The Device Structure

The device structure considered for the simulation is again a GAA (cylindrical) SiNW FET shown in Figure 4.5. For all simulations, the channel length is taken to be 10 nm and a gate oxide thickness of 1 nm is assumed, the oxide being SiO_2. In addition, the NW diameter is taken to be 5 nm. The gate material has been assumed to have an adjustable work function and has been set to a mid-gap value of 4.5 eV.

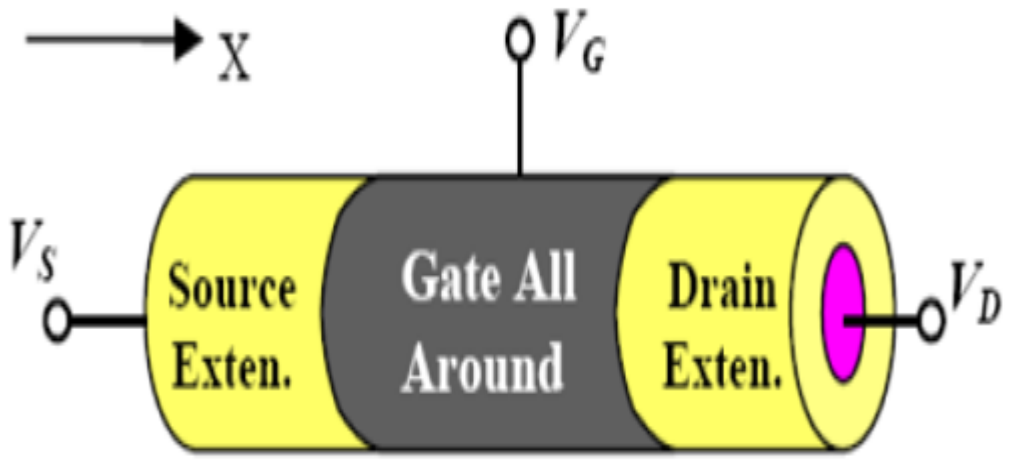
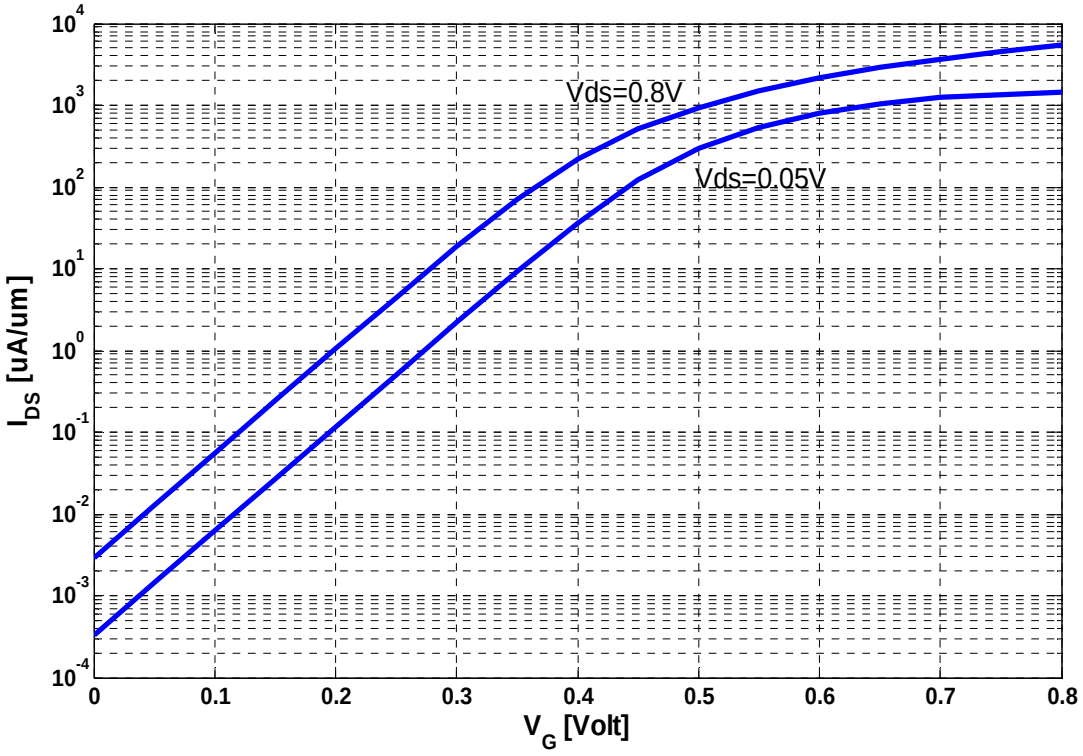


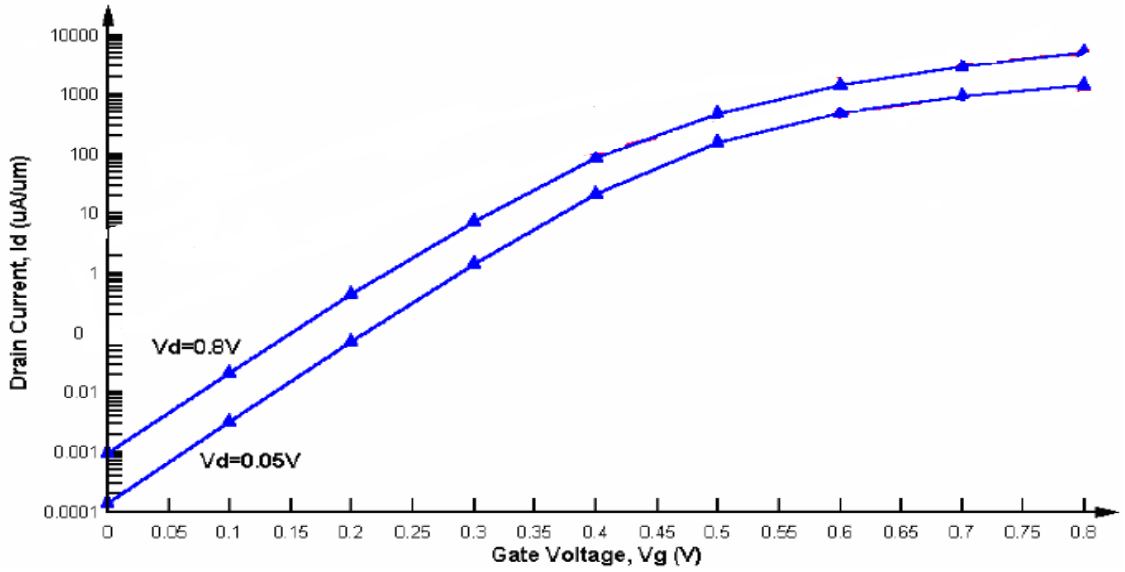
Figure 4.5 SiNW FET structure assumed for the numerical simulation [54].

4.1.3.2 Simulation Results and Discussion

The transfer characteristics, log I_{ds} - $V_{gs,}$ is shown in Figure 4.6(a) and (b) drawn from the compact modeling and numerical simulation respectively. The value of I_{off} is calculated to be 2.929 nA/ µm from the compact modeling simulation. From the numerical simulation results, the value of I_{off} is calculated to be 1 nA/µm, which is very small when compared to the compact modeling simulation result. This is probably due to the inclusion of two dimensional electrostatics effects in the compact modeling simulation. The other parameters extracted from these graphs are the values for SS and DIBL. The value for SS from the compact modeling simulation is calculated to be 70.09 mV/dec which is in good agreement with that of the numerical modeling result that is 75.38 mV/dec. Finally the DIBL is calculated to be 76.94 mV/V from the compact modeling simulation and 94.6 mV/V from the numerical result. These results suggest that there is a large discrepancy in the DIBL values between the two simulations. This is, also, probably due to the inclusion of two dimensional electrostatic effects in the modeling equations of the compact model.



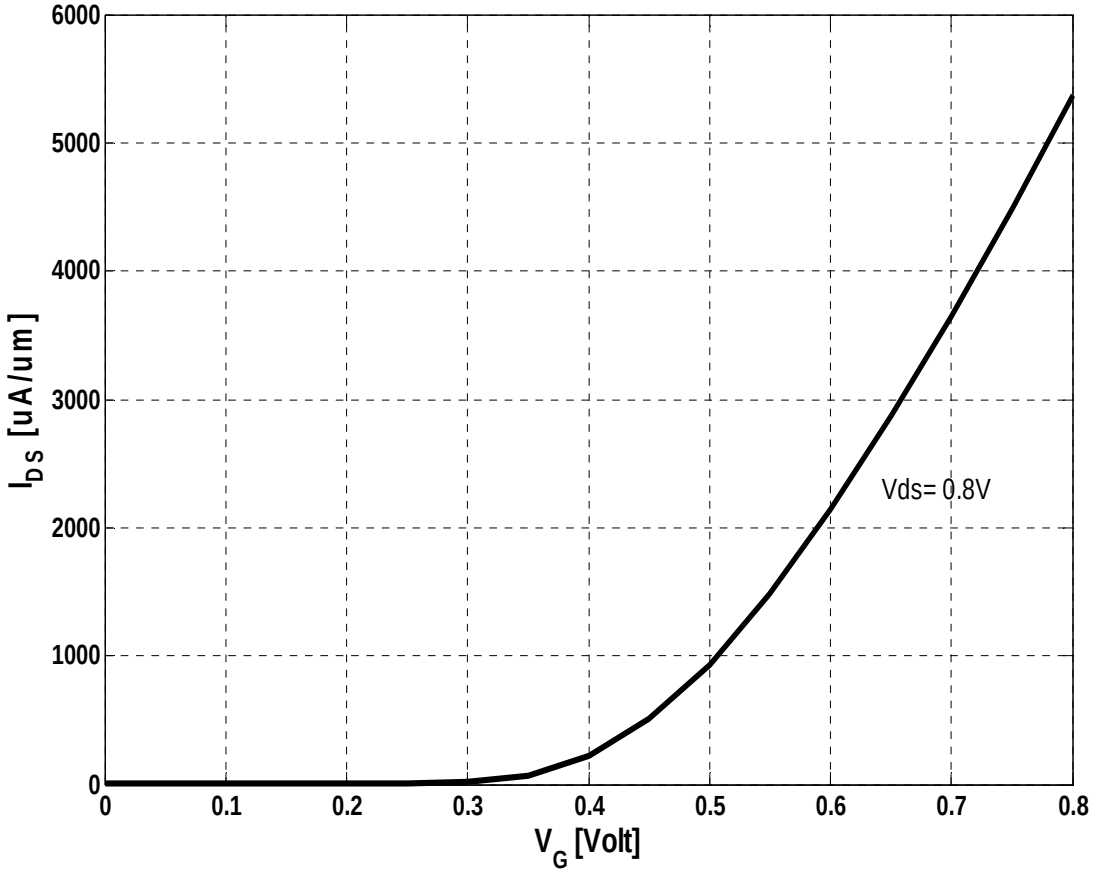
(a)



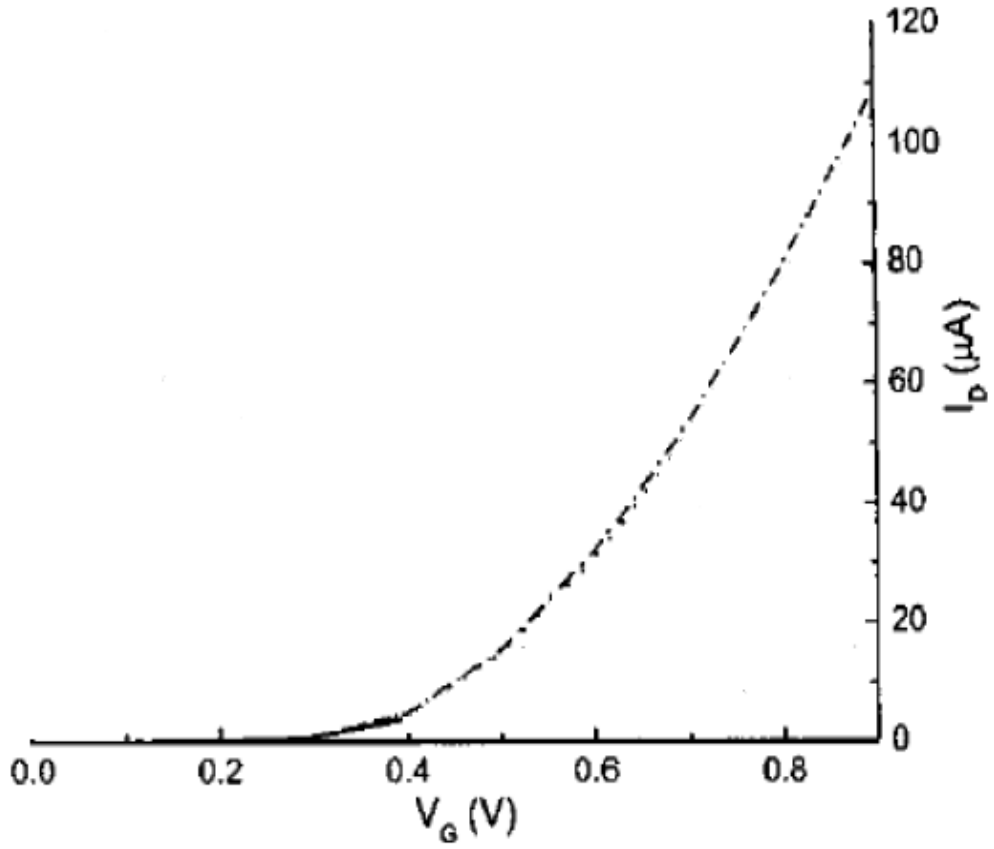
(b)

Figure 4.6 Simulated transfer characteristics SiNW FET (a) for the compact modeling simulation. (b) For the numerical simulation [49].

The linear transfer characteristics drawn from the compact modeling simulation and that of the numerical simulation are shown in Figure 4.7(a) and (b) respectively. From these graphs the on-state current is extracted. The value of I_{on} for both simulations is taken as the current at zero gate voltage and at the highest drain voltage, which in this case is 0.8 V. From the compact modeling simulation, the on-state current is calculated to be 4950 mA/µm. Also the on-state current from the numerical simulation is calculated to be 5024 mA/µm, which is a little bit higher than that from the compact model. This implies there is a very good agreement in the value of I_{on} between the two simulation results.



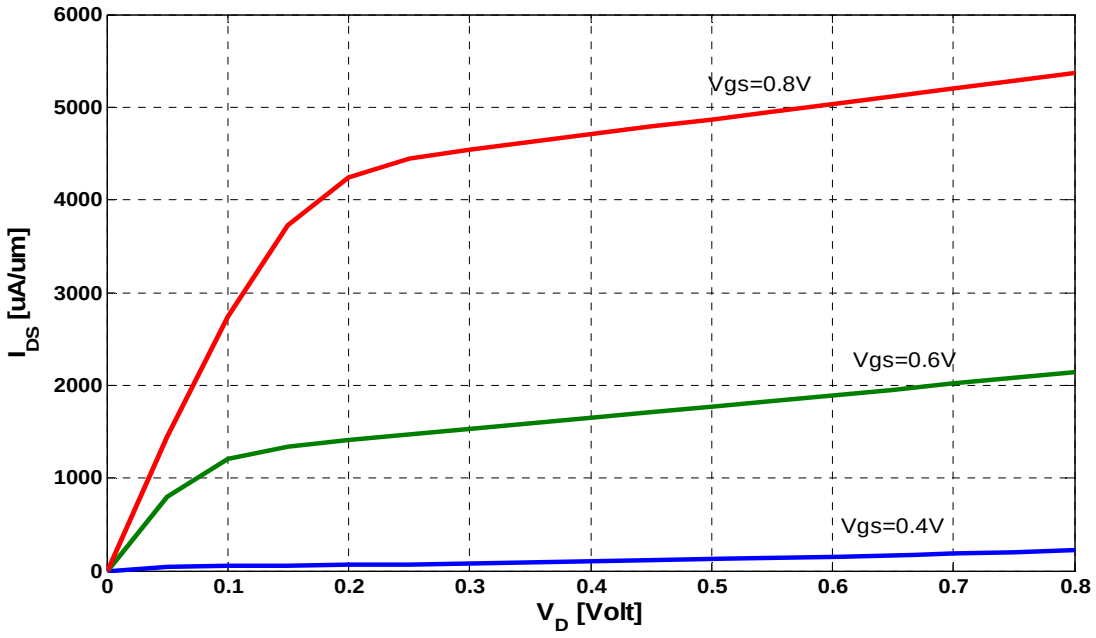
(a)



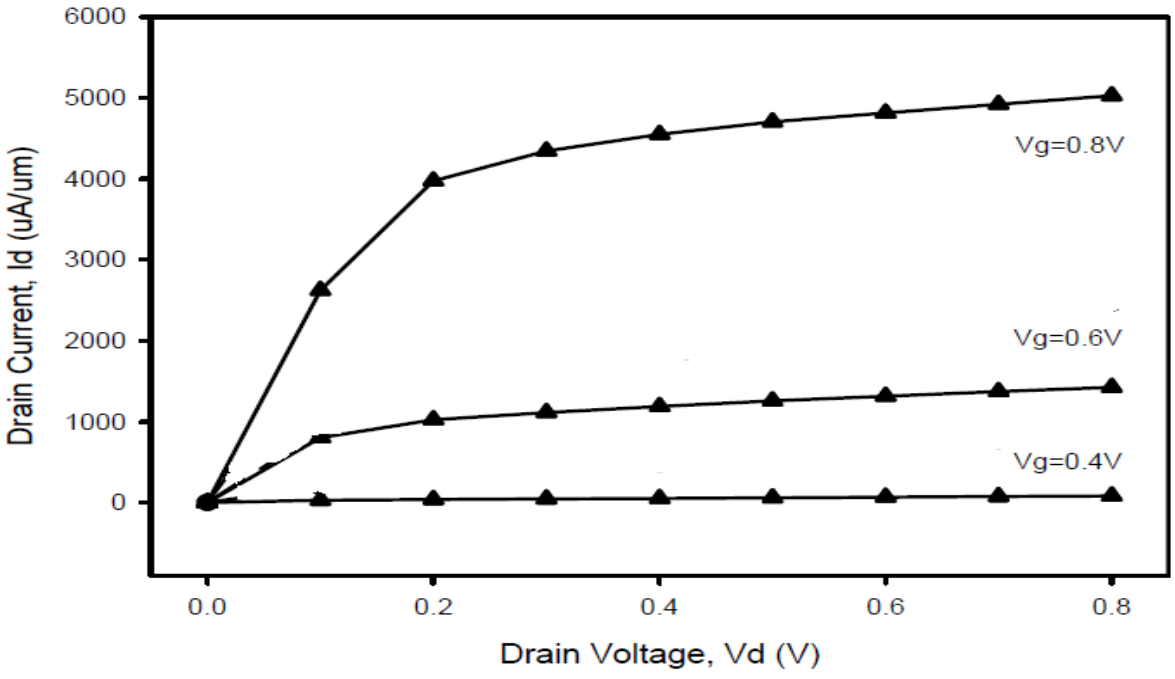
(b)

Figure 4.7 The linear transfer characteristics from (a) the compact modeling simulation and (b) from the numerical simulation [49].

Finally, the out put characteristics curves, I_{ds} - V_{ds}, drawn from the compact modeling and from that of the numerical simulation are shown in Figure 4.8(a) and (b). Transconductance is the most important dynamic parameter of MOS for analogue applications because it reflects the transfer efficiency from input to output. The output conductance is extracted from these graphs for a gate voltage of 0.8 V. The output resistance is found to be 147.17 kΩ from the compact modeling simulation result and 187.46 kΩ from the numerical simulation result. In both cases a very high output conductance is found and they are in good agreement. These results are summarized in Table 4.2.



(a)



(b)

Figure 4.8 Simulated $I_{ds} - V_{ds}$ curves for the SiNW FET from (a) compact modeling simulation. (b) Numerical modeling simulation.

Table 4.2 Comparison between the compact model and numerical model simulation results.

	Simulated SiNW FET (COMPACT MODEL)	Simulated SiNW FET (tool Nano Wire)
Nano wire diameter	5nm	5nm
Oxide thickness	1nm	1nm
ON current	5365µA/µm	5024 µA /µm
OFF current	2.929nA/ µm	1nA/ µm
ON/OFF ratio	$\sim 10^6$	$\sim 10^6$
DIBL	76.94mV/V	75.38mV/V
Subthreshold Slope	70.94mV/dec	94.6mV/dec

4.2 The Effect of Scaling of Physical Parameters on the Device Performance

The performance of SiNW FET is a direct function of its physical parameters. Therefore, scaling of these parameters greatly affects its performance. There are various important physical parameters of SiNW FETs. Among these, channel length, gate length, gate width, NW diameter and oxide thickness are the main parameters. In this section, we will investigate the effect of scaling of the NW diameter and the gate oxide thickness on the device performance.

4.2.1 Scaling of NW Diameter

For this simulation the SiNW FET structure of Figure 4.1 is used. For all simulations, the gate oxide thickness is kept at 1 nm and the NW diameter is varied from 2 nm to 6 nm. The voltage range taken for the gate and drain bias is 0 V-1 V.

It is known that a high performing transistor should have a reasonably low Off-state current and a large On-state current, so that its I_{on} / I_{off} ratio becomes fairly large. As we can see from Figure 4.9, the value of I_{off} decreases with decreasing NW diameter. This is due to the high suppression of SCEs because of the greatest control of gate over the channel. Therefore, as expected, gate has the greatest control of the channel for lower NW diameters.

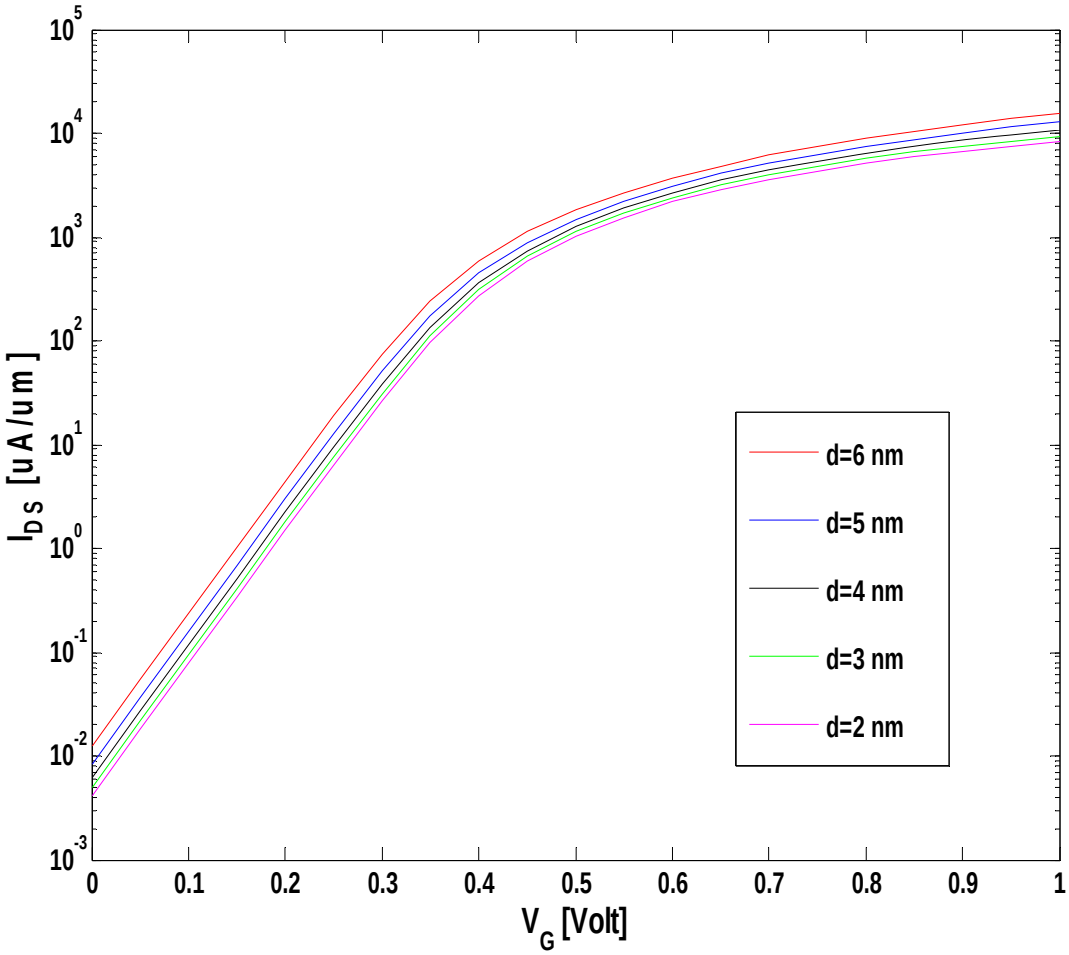


Figure 4.9 Log I_{ds} –V_{gs} graph with varying diameter from 2 nm to 6 nm in steps of 1nm.

Figure 4.10 shows the output, I_{ds}-$V_{D,}$ characteristics graph with varying NW diameters. The drain supply voltage is kept at 1 V for all simulations and the gate supply voltage is varied b/n 0V and 1V in the simulation. From this graph, we can see that the highest current occurs at the highest NW diameter taken in the simulation. One possible reason for the increase of current with the NW diameter can be the quantum confinement effect. As the NW diameter decreases there will be quantum mechanical confinement of states which decreases the On-state current. Figure 4.10 depicts I_{ds}-V_{ds} characteristics with varying NW diameter.

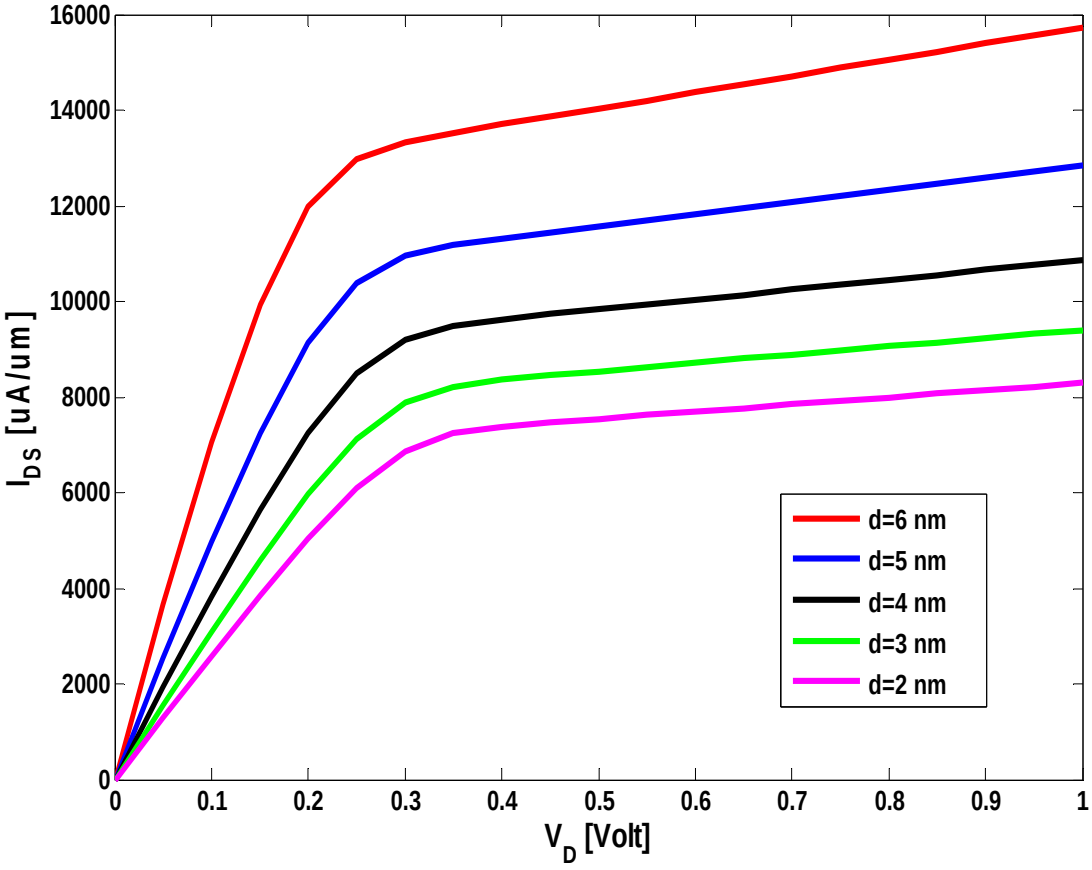


Figure 4.10 Ids-Vds characteristics graph for varying diameters from 2 nm to 6 nm in steps of 1nm.

4.2.2 Scaling of Gate Oxide Thickness

To see the effect of scaling of gate oxide thickness on the performance of SiNW FET, the oxide thickness is varied from 1 nm to 3 nm. In the simulation, the gate supply voltage is kept at 1V and the drain supply voltage is varied b/n 0V and 1V. As shown in Figure 4.11, the value I_{off} is found to be the same for all oxide thickness values taken. Figure 4.12 shows the increase of the value of I_{on} with the oxide thickness. Similar to the diameter scaling, this is due to the quantum confinement effect at the smaller oxide thicknesses. Note that for all simulations the NW diameter is kept at 5 nm.

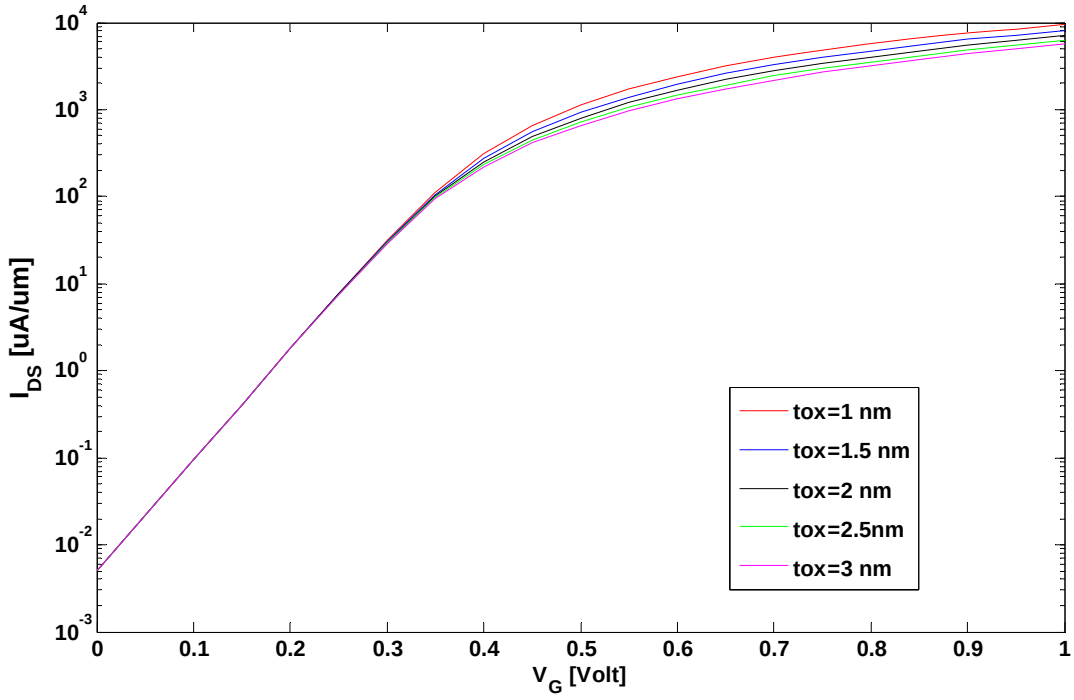


Figure 4.11 I_{ds}-V_{gs} graph for oxide thickness varied from 1 nm to 3 nm.

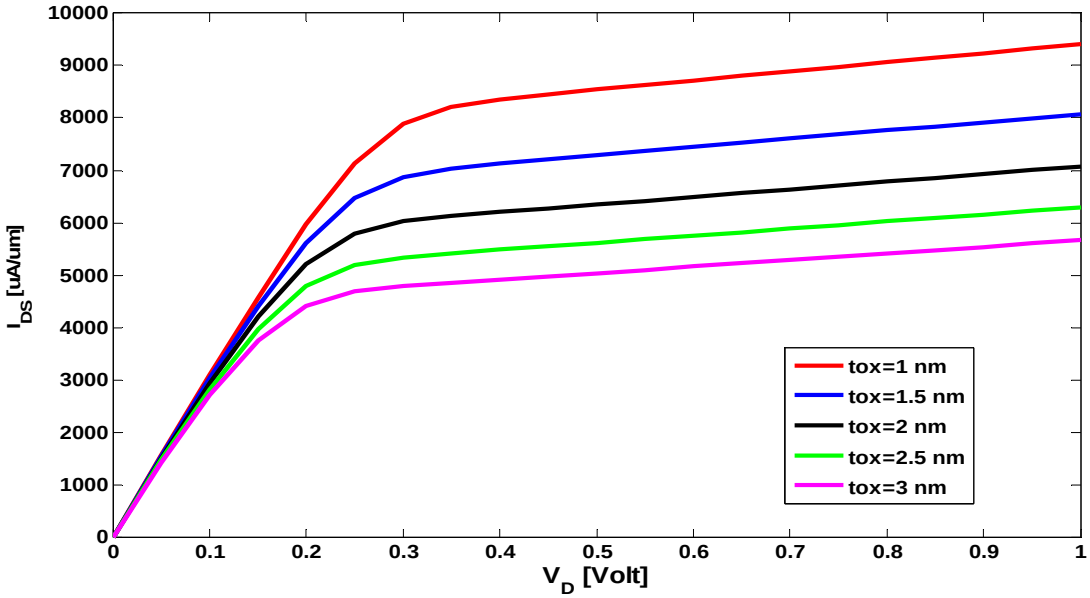


Figure 4.11 I_{ds}-V_{ds} characteristic graph for oxide thickness varying from 1 nm to 3 nm.

CHAPTER FIVE : CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this thesis, the modeling of SiNW FETs is done. The model development was divided into two sections. The first section is devoted to the modeling of SiNW FETs assuming ballistic transport. The model is based on Natori's theory of ballistic MOSFETs and is extended to include 2D electrostatic effects. In the second section, the model of SiNW FETs is developed assuming the presence of scattering in the device. This model is based on McKelvey's flux method. When scattering effects are assumed to be negligible, the scattering model reduces to the ballistic SiNW FET model developed in section one.

The developed model was tested by comparing its simulation results with that of the experimentally reported results. The comparison showed that the developed model agrees well with the experimentally obtained results. Also, the simulation results found from the developed model were compared with that of the numerical simulation results. The numerical simulation results were found from the NanoHub, using the software, NW. The comparison results give a good agreement which shows the accuracy of the developed model.

In order to see the effect of scaling of the physical parameters on the performance of SiNW FET, we have made simulations by varying these parameters. Specifically, the simulation was done by varying the diameter of the NW and the gate oxide thickness. Our result showed that the On-state current increased with the increase of the NW diameter from 1 nm to 6 nm. Similarly, the Off-state current decreased with the decrease of diameter from 6 nm to 1 nm. The decrease of I_{off} is attributed to the increasing of the gate control with decreasing diameter. The increase of I_{on} with the NW diameter is due to the increase of quantum confinement effects with the decreasing diameter. In order to see the effect of scaling of gate oxide thickness on the performance of the device, simulation was done. Similar to the diameter scaling case, there was an increase of On-state current with the gate oxide thickness and there was a decrease of Off-state current with decreasing of oxide thickness.

5.2 Future Work

In the development of a model for SiNW FET, the source/drain contacts are assumed to be degenerately doped semiconductors. However, recently SiNW FETs whose source/drain contacts are made of metals are being developed. Therefore one possible future work could be to assume metal source/drain contacts instead of semiconductors in the modeling of these transistors. Also, in the model derivation, the effects of source/drain resistance should be included.

The other possible future work could be extending the model developed in this thesis to include the effects of higher subbands. This is because in the model developed here, only the lowest (first) subband is assumed to be occupied by carriers. Therefore extending of the model could also be done in the future.

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APPENDIX

MATLAB code

For implementation of the developed model in to various graphs a MATLAB simulator is used. The complete MATLAB code for the simulation of the I-V characteristic graphs is given in the first part of the appendix. In the second and third part of the appendix, the code for NW diameter scaling and oxide thickness scaling are given respectively.

I. MATLAB code for the I-V characteristics

```
function I = main( t,d,epsr,T,VI,VF,NV)

% Physical constants
m0=0.91e-30;    hbar=1.05e-34;      q=1.6e-19;    eps0=8.85e-12;     kB=1.38e-23;
m=0.19*m0;                          % Transverse mass of electron
kT=kB*T/q;                          % Thermal voltage.
V=linspace(VI,VF,NV);               % Voltage (gate or drain) steps.
Cox=2*pi*epsr*eps0/log((2*t+d)/d);
CG=Cox;
C_SIG=CG/alphag;                    % C_SIG=sum of capacitors
U0=q/C_SIG;                         % Charging energy
N1D= 2*sqrt(2*m*kB*T/pi/(hbar)^2);% Effective 1D density of states

N0 = N1D*fermi(Ef/kT,1,-1/2);           % Electron concentration at the top of the barrier in neutral
device.
I0 = 2*(q*kB*T/pi/hbar);
nL(0)=zeros(NV,NV);                     % Mobile charge density.
I=zeros(NV,NV);                     % Current.
Ef_mat=zeros(NV,NV);                % Source Fermi level.
Esub_max=zeros(NV,NV);              % Energy at the top of the barrier.

for kVg=1:NV                                        % Bias loop begins.
   for kV=1:NV
      Vg=V(kVg);  Vd=V(kV);
      mu1=Ef;   mu2=mu1-Vd;                         % Source and drain fermi levels.
      UL=-(alphag*Vg)-(alphad*Vd);                  % Laplace potential.
      Uscf=fzero(@Uscf_zero,0,optimset('tolx',1e12),N1D,mu1,mu2,kT,UL,U0,N0);
nL(0)=0.5*N1D*(fermi((mu1-Uscf)/kT,1,-1/2)+fermi((mu2-Uscf)/kT,1,1/2))-N0;
                % Mobile charge induced by gate and drain
      nL(kV,kVg)=nL(0);
      eta1=(mu1-Uscf)/kT; eta2=(mu2-Uscf)/kT;
      % Vd changes along fixed column and Vg changes along fixed row.
      I(kV,kVg)=I0*(fermi(eta1,1,0)-fermi(eta2,1,0));
      Esub_max(kV,kVg)=Uscf; Ef_mat(kV,kVg)=mu1;
```

```
      Us(kV,kVg) = Uscf;
   end
end
  %transconductance, gm, and output conductance,gd, calculation.
gm=(I(NV,NV)-I(NV,NV-1))/(V(NV)-V(NV-1));
gd=(I(NV,NV)-I(NV-1,NV))/(V(NV)-V(NV-1));
%subthreshold slope,s, and DIBL calculation.
I1=log10(I(NV,:));
I2=log10(I(2,:));
Vg1=interp1(I1,V,log10(I(NV,1)),'spline');
Vg2=interp1(I1,V,log10(I(NV,1)/10),'spline');
Vg3=interp1(I2,V,log10(I(NV,1)),'spline');
S=(Vg1-Vg2)*1000;
DIBL=(Vg3-Vg1)/(V(NV)-V(2))*1000;

         % Plots the Id-Vg and Id-Vd characteristics
 figure(1);
 h1=semilogy(V,I([2,NV],:)./(10.0e-9));
 xlabel('V_G [Volt]');
ylabel('I_{DS} [uA/um]');
set(gca,'xlim',[V(1) V(NV)]);
grid on;
figure(2);
   h1=plot(V,I([NV],:)/10.0e-9);
   xlabel('V_G [Volt]');
ylabel('I_{DS} [uA/um]');
grid on;
figure(3);
h1 = plot(V,I(:,[9,13,NV])./10.0e-9);
xlabel('V_D [Volt]');
ylabel('I_{DS} [uA/um]');
set(gca,'xlim',[V(1) V(NV)]);
grid on;
```

II. MATLAB code for the NW diameter scaling graphs

```
function I = main( t,epsr,mt,T, VI,VF,NV)

% Physical constants
m0=0.91e-30;   hbar=1.05e-34;    q=1.6e-19;   eps0=8.85e-12;    kB=1.38e-23;
d1=2.0e-9; d2=3.0e-9; d3=4.0e-9; d4=5.0e-9; d5=6.0e-9;
m=mt*m0;                    % Transverse mass of electron
kT=kB*T/q;                  % Thermal voltage.
V=linspace(VI,VF,NV);           % Voltage (gate or drain) steps.
Cins1=2*pi*epsr*eps0/log((2*t+d1)/d1);
Cins2=2*pi*epsr*eps0/log((2*t+d2)/d2);
```

```
Cins3=2*pi*epsr*eps0/log((2*t+d3)/d3);
Cins4=2*pi*epsr*eps0/log((2*t+d4)/d4);
Cins5=2*pi*epsr*eps0/log((2*t+d5)/d5);
CG1=Cins1;
CG2=Cins2;
CG3=Cins3;
CG4=Cins4;
CG5=Cins5;
C_SIG1=CG1/alphag;                % C_SIG=sum of capacitors
C_SIG2=CG2/alphag;
C_SIG3=CG3/alphag;
C_SIG4=CG4/alphag;
C_SIG5=CG5/alphag;
U01=q/C_SIG1;                     % Charging energy
U02=q/C_SIG2;
U03=q/C_SIG3;
U04=q/C_SIG4;
U05=q/C_SIG5;
N1D= 2*sqrt(2*m*kB*T/pi/(hbar)^2);% Effective 1D density of states
N0 = N1D*fermi(Ef/kT,1,-1/2);          % Electron concentration at the top of the barrier in neutral
device.
I0 = 2*(q*kB*T/pi/hbar);
N=zeros(NV,NV);                   % Mobile charge density.
I1=zeros(NV,NV); % Current.
I2=zeros(NV,NV);
I3=zeros(NV,NV);
I4=zeros(NV,NV);
I5=zeros(NV,NV);
Ef_mat=zeros(NV,NV);              % Source Fermi level.
Esub_max=zeros(NV,NV);            % Energy at the top of the barrier.

for kVg=1:NV                                    % Bias loop begins.
   for kV=1:NV
      Vg=V(kVg);  Vd=V(kV);
      mu1=Ef;   mu2=mu1-Vd;                     % Source and drain fermi levels.
       UL=-(alphag*Vg)-(alphad*Vd);             % Laplace potential.
 Uscf1=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U01,N0);
 Uscf2=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U02,N0);
 Uscf3=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U03,N0);
 Uscf4=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U04,N0);
 Uscf5=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U05,N0);
 dN=0.5*N1D*(fermi((mu1-Uscf1)/kT,1,-1/2)+fermi((mu2-Uscf1)/kT,1,-1/2))-N0;        %   Mobile
charge induced by gate and drain

      N(kV,kVg)=dN;
      eta11=(mu1-Uscf1)/kT; eta21=(mu2-Uscf1)/kT;
```

```
        eta12=(mu1-Uscf2)/kT; eta22=(mu2-Uscf2)/kT;
        eta13=(mu1-Uscf3)/kT; eta23=(mu2-Uscf3)/kT;
        eta14=(mu1-Uscf4)/kT; eta24=(mu2-Uscf4)/kT;
        eta15=(mu1-Uscf5)/kT; eta25=(mu2-Uscf5)/kT;
        % Vd changes along fixed column and Vg changes along fixed row.
        I1(kV,kVg)=I0*(fermi(eta11,1,0)-fermi(eta21,1,0));
        I2(kV,kVg)=I0*(fermi(eta12,1,0)-fermi(eta22,1,0));
        I3(kV,kVg)=I0*(fermi(eta13,1,0)-fermi(eta23,1,0));
        I4(kV,kVg)=I0*(fermi(eta14,1,0)-fermi(eta24,1,0));
        I5(kV,kVg)=I0*(fermi(eta15,1,0)-fermi(eta25,1,0));

       Esub_max1(kV,kVg)=Uscf1; Ef_mat(kV,kVg)=mu1;

       Esub_max2(kV,kVg)=Uscf2;
       Esub_max3(kV,kVg)=Uscf3;
       Esub_max4(kV,kVg)=Uscf4;
       Esub_max5(kV,kVg)=Uscf5;

        Us1(kV,kVg) = Uscf1;
        Us2(kV,kVg) = Uscf2;
        Us3(kV,kVg) = Uscf3;
        Us4(kV,kVg) = Uscf4;
        Us5(kV,kVg) = Uscf5;
    end
end
   %transconductance, gm, and channel conductance,gd, calculation.
gm1=(I1(NV,NV)-I1(NV,NV-1))/(V(NV)-V(NV-1));
gm2=(I2(NV,NV)-I2(NV,NV-1))/(V(NV)-V(NV-1));
gm3=(I3(NV,NV)-I3(NV,NV-1))/(V(NV)-V(NV-1));
gm4=(I4(NV,NV)-I4(NV,NV-1))/(V(NV)-V(NV-1));
gm5=(I5(NV,NV)-I5(NV,NV-1))/(V(NV)-V(NV-1));

gd1=(I1(NV,NV)-I1(NV-1,NV))/(V(NV)-V(NV-1));
gd2=(I2(NV,NV)-I2(NV-1,NV))/(V(NV)-V(NV-1));
gd3=(I3(NV,NV)-I3(NV-1,NV))/(V(NV)-V(NV-1));
gd4=(I4(NV,NV)-I4(NV-1,NV))/(V(NV)-V(NV-1));
gd5=(I5(NV,NV)-I5(NV-1,NV))/(V(NV)-V(NV-1));
%subthreshold slope,s, and DIBL calculation.
I11=log10(I1(NV,:));
I12=log10(I2(NV,:));
I13=log10(I3(NV,:));
I14=log10(I4(NV,:));
I15=log10(I5(NV,:));
I21=log10(I1(2,:));
I22=log10(I2(2,:));
I23=log10(I3(2,:));
```

```
I24=log10(I4(2,:));
I25=log10(I5(2,:));

vg11=interp1(I11,V,log10(I1(NV,1)),'spline');
vg12=interp1(I12,V,log10(I2(NV,1)),'spline');
vg13=interp1(I13,V,log10(I3(NV,1)),'spline');
vg14=interp1(I14,V,log10(I4(NV,1)),'spline');
vg15=interp1(I15,V,log10(I5(NV,1)),'spline');

vg21=interp1(I11,V,log10(I1(NV,1)/10),'spline');
vg22=interp1(I12,V,log10(I2(NV,1)/10),'spline');
vg23=interp1(I13,V,log10(I3(NV,1)/10),'spline');
vg24=interp1(I14,V,log10(I4(NV,1)/10),'spline');
vg25=interp1(I15,V,log10(I5(NV,1)/10),'spline');

vg31=interp1(I21,V,log10(I1(NV,1)),'spline');
vg32=interp1(I22,V,log10(I2(NV,1)),'spline');
vg33=interp1(I23,V,log10(I3(NV,1)),'spline');
vg34=interp1(I24,V,log10(I4(NV,1)),'spline');
vg35=interp1(I25,V,log10(I5(NV,1)),'spline');

S1=(vg11-vg21)*1000;
S2=(vg12-vg22)*1000;
S3=(vg13-vg23)*1000;
S4=(vg14-vg24)*1000;
S5=(vg15-vg25)*1000;

DIBL1=(vg31-vg11)/(V(NV)-V(2))*1000;
DIBL2=(vg32-vg12)/(V(NV)-V(2))*1000;
DIBL3=(vg33-vg13)/(V(NV)-V(2))*1000;
DIBL4=(vg34-vg14)/(V(NV)-V(2))*1000;
DIBL5=(vg35-vg15)/(V(NV)-V(2))*1000;
 % Plots charactteristics and output graphs
 figure(1);
    h1=semilogy(V,I1([NV],:)./(2*1.0e-9),'r');
    hold on;
    h6=semilogy(V,I2([NV],:)./(3*1.0e-9),'b');
    h3=semilogy(V,I3([NV],:)./(4*1.0e-9),'k');
    h4=semilogy(V,I4([NV],:)./(5*1.0e-9),'g');
    h5=semilogy(V,I5([NV],:)./(6*1.0e-9),'m');
   xlabel('V_G [Volt]');
   ylabel('I_{DS} [uA/um]');
   set(gca,'xlim',[V(1) V(NV)]);
   grid on;
   figure(2);
    h1=plot(V,I1([NV],:),'r');
```

```
    hold on;
     h6=plot(V,I2([NV],:),'b');
     h3=plot(V,I3([NV],:),'k');
     h4=plot(V,I4([NV],:),'g');
     h5=plot(V,I5([NV],:),'m');
xlabel('V_G [Volt]');
ylabel('I_{DS} [uA]');
set(gca,'xlim',[V(1) V(NV)]);
grid on;
figure(3);
h1 = plot(V,I1(:,[NV])./(2*1.0e-9),'r');
hold on;
h6 = plot(V,I2(:,[NV])./(3*1.0e-9),'b');
h3 = plot(V,I3(:,[NV])./(4*1.0e-9),'k');
h4 = plot(V,I4(:,[NV])./(5*1.0e-9),'g');
h5 = plot(V,I5(:,[NV])./(6*1.0e-9),'m');
xlabel('V_D [Volt]');
ylabel('I_{DS} [uA/um]');
set(gca,'xlim',[V(1) V(NV)]);
grid on;
```

III. MATLAB code for the gate oxide scaling graph results

```
function I = main(d,epsr,mt,T, VI,VF,NV)

% Physical constants
m0=0.91e-30;    hbar=1.05e-34;     q=1.6e-19;    eps0=8.85e-12;     kB=1.38e-23;
t1=1.0e-9; t2=1.5e-9; t3=2.0e-9; t4=2.5e-9; t5=3.0e-9;
m=mt*m0;                        % Transverse mass of electron
kT=kB*T/q;                      % Thermal voltage.
V=linspace(VI,VF,NV);               % Voltage (gate or drain) steps.
Cins1=2*pi*epsr*eps0/log((2*t1+d)/d);
Cins2=2*pi*epsr*eps0/log((2*t2+d)/d);
Cins3=2*pi*epsr*eps0/log((2*t3+d)/d);
Cins4=2*pi*epsr*eps0/log((2*t4+d)/d);
Cins5=2*pi*epsr*eps0/log((2*t5+d)/d);
CG1=Cins1;
CG2=Cins2;
CG3=Cins3;
CG4=Cins4;
CG5=Cins5;
C_SIG1=CG1/alphag;                  % C_SIG=sum of capacitors
C_SIG2=CG2/alphag;
C_SIG3=CG3/alphag;
C_SIG4=CG4/alphag;
```

```
C_SIG5=CG5/alphag;
U01=q/C_SIG1;                    % Charging energy
U02=q/C_SIG2;
U03=q/C_SIG3;
U04=q/C_SIG4;
U05=q/C_SIG5;                  % Charging energy
N1D= 2*sqrt(2*m*kB*T/pi/(hbar)^2);% Effective 1D density of states

N0 = N1D*fermi(Ef/kT,1,-1/2);          % Electron concentration at the top of the barrier in neutral device.
I0 = 2*(q*kB*T/pi/hbar);
N=zeros(NV,NV);                % Mobile charge density.
I1=zeros(NV,NV); % Current.
I2=zeros(NV,NV);
I3=zeros(NV,NV);
I4=zeros(NV,NV);
I5=zeros(NV,NV);               % Current.
Ef_mat=zeros(NV,NV);             % Source Fermi level.
Esub_max=zeros(NV,NV);           % Energy at the top of the barrier.
for kVg=1:NV                                    % Bias loop begins.
   for kV=1:NV
      Vg=V(kVg);  Vd=V(kV);
      mu1=Ef;   mu2=mu1-Vd;                     % Source and drain fermi levels.
      UL=-(alphag*Vg)-(alphad*Vd);              % Laplace potential.
Uscf1=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U01,N0);
Uscf2=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U02,N0);
Uscf3=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U03,N0);
Uscf4=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U04,N0);
Uscf5=fzero(@Uscf_zero,0,optimset('tolx',1e-12),N1D,mu1,mu2,kT,UL,U05,N0);
dN=0.5*N1D*(fermi((mu1-Uscf1)/kT,1,-1/2)+fermi((mu2-Uscf1)/kT,1,-1/2))-N0;        % Mobile charge induced by gate and drain

      N(kV,kVg)=dN;
      eta11=(mu1-Uscf1)/kT; eta21=(mu2-Uscf1)/kT;
      eta12=(mu1-Uscf2)/kT; eta22=(mu2-Uscf2)/kT;
      eta13=(mu1-Uscf3)/kT; eta23=(mu2-Uscf3)/kT;
      eta14=(mu1-Uscf4)/kT; eta24=(mu2-Uscf4)/kT;
      eta15=(mu1-Uscf5)/kT; eta25=(mu2-Uscf5)/kT;
      % Vd changes along fixed column and Vg changes along fixed row.
      I1(kV,kVg)=I0*(fermi(eta11,1,0)-fermi(eta21,1,0));
      I2(kV,kVg)=I0*(fermi(eta12,1,0)-fermi(eta22,1,0));
      I3(kV,kVg)=I0*(fermi(eta13,1,0)-fermi(eta23,1,0));
      I4(kV,kVg)=I0*(fermi(eta14,1,0)-fermi(eta24,1,0));
      I5(kV,kVg)=I0*(fermi(eta15,1,0)-fermi(eta25,1,0));
      Esub_max1(kV,kVg)=Uscf1; Ef_mat(kV,kVg)=mu1;
```

```
      Esub_max2(kV,kVg)=Uscf2;
      Esub_max3(kV,kVg)=Uscf3;
      Esub_max4(kV,kVg)=Uscf4;
      Esub_max5(kV,kVg)=Uscf5;

       Us1(kV,kVg) = Uscf1;
       Us2(kV,kVg) = Uscf2;
       Us3(kV,kVg) = Uscf3;
       Us4(kV,kVg) = Uscf4;
       Us5(kV,kVg) = Uscf5;

   end
end
  %transconductance, gm, and channel conductance,gd, calculation.
gm=(I1(NV,NV)-I1(NV,NV-1))/(V(NV)-V(NV-1));
gd=(I1(NV,NV)-I1(NV-1,NV))/(V(NV)-V(NV-1));
%subthreshold slope,s, and DIBL calculation.
Ie1=log10(I1(NV,:));
Ie2=log10(I1(2,:));
vv1=interp1(Ie1,V,log10(I1(NV,1)),'spline');
vv2=interp1(Ie1,V,log10(2*I1(NV,1)),'spline');
vv3=interp1(Ie2,V,log10(I1(NV,1)),'spline');
S=(vv2-vv1)/log10(2)*1000;
DIBL=(vv3-vv1)/(V(NV)-V(2))*1000;
        % Plots characteristics and output graphs
        figure(1);
  h1=semilogy(V,I1([NV],:)./(5*1.0e-9),'r');
   hold on;
   h2=semilogy(V,I2([NV],:)./(5*1.0e-9),'b');
   h3=semilogy(V,I3([NV],:)./(5*1.0e-9),'k');
   h4=semilogy(V,I4([NV],:)./(5*1.0e-9),'g');
   h5=semilogy(V,I5([NV],:)./(5*1.0e-9),'m');
   xlabel('V_G [Volt]');
   ylabel('I_{DS} [uA/um]');
   set(gca,'xlim',[V(1) V(NV)]);
  grid on;
   figure(2);
   h1=plot(V,I1([NV],:),'r');
   hold on;
   h2=plot(V,I2([NV],:),'b');
   h3=plot(V,I3([NV],:),'k');
   h4=plot(V,I4([NV],:),'g');
   h5=plot(V,I5([NV],:),'m');
   xlabel('V_G [Volt]');
ylabel('I_{DS} [uA/um]');
set(gca,'xlim',[V(1) V(NV)]);
```

```
grid on;
figure(3);
h1 = plot(V,I1(:,[NV])./(5*1.0e-9),'r');
hold on;
h2 = plot(V,I2(:,[NV])./(5*1.0e-9),'b');
h3 = plot(V,I3(:,[NV])./(5*1.0e-9),'k');
h4 = plot(V,I4(:,[NV])./(5*1.0e-9),'g');
h5 = plot(V,I5(:,[NV])./(5*1.0e-9),'m');
xlabel('V_D [Volt]');
ylabel('I_{DS} [uA/um]');
set(gca,'xlim',[V(1) V(NV)]);
grid on;
```