Design and Performance Analysis of Schottky Terahertz Transceiver for 6G Wireless Communication

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Declaration

I, the undersigned, declare that the thesis comprises my own work in compliance with internationally accepted practices; I have fully acknowledged and referred all materials used in this thesis work.

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This is to certify that the thesis prepared by **Surafel Berhanu Abegaz**, entitled *Design and Performance Analysis of Schottky Terahertz Transceiver for 6G Wireless Communication* and submitted in partial fulfillment of the requirements for the degree of Master of Science (Communication Engineering) complies with the regulations of the University and meets the accepted standards with respect to originality and quality.

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Dedicated to all who labor for humanity.

— Surafel

ABSTRACT

Wireless technology is in a rapid chase of higher data rates to satisfy the growing demands of services and devices which will all interconnect. One of the envisioned technologies to fulfill this is Terahertz wireless communication owing to wide bandwidth and possible bitrates into the Tbps. Challenges however exist with Terahertz source generation. One such candidate based on Schottky diode carrier upconversion may be a low cost solution, nonetheless phase noise presents a bottleneck in such an upconversion scheme for Phase Shift Keying (PSK) and Quadrature Amplitude Modulation (QAM).

In this study, high bitrate communication was investigated with respect to phase noise and Local Oscillator (LO) (Terahertz (THz)) obtained by frequency multiplication. Terahertz transceivers with both Zero-Intermediate Frequency (IF) and double conversion architectures were designed. The transceivers were evaluated with simulation using PSK and QAM modulation schemes and examined for the optimal frequency range. Due to the excellent properties of graphene as well as future relevance Graphene Field Effect Transistor (GFET) and Schottky Barrier Diode (SBD) were the primary device technologies.

High bitrate communication was possible at 209GHz with double conversion architecture. Five Gbps was obtained with Binary Phase Shift Keying (BPSK), 10Gbps with Quadrature Phase Shift Keying (QPSK), 15Gbps with 8 Phase Shift Keying (8PSK), 20Gbps with 16-ary Quadrature Amplitude Modulation (16QAM) and 30Gbps with 64-ary Quadrature Amplitude Modulation (64QAM) and had Error Vector Magnitude (EVM) of 40.9%, 49.1%, 12.9%, 28.7% and 13.1% respectively. A 73µm GFET was employed as the Radio Frequency (RF) transistor technology. The 185.9GHz LO was designed with Schottky diode multiplication and had peak phase noise of -101dBc/Hz. The frequency multiplication process was found to be limited to the lower THz range of less than 375GHz, for satisfactory communication performance. Active frequency multipliers degrade the phase noise for high order PSK. However a x2 subharmonic mixer can be used, if the LO power is limiting the conversion efficiency. Single stage Schottky multipliers with multiple harmonics and filtering was found to produce high power but also high phase noise as result of the Butterworth filter. As a result the single stage multipliers are suitable for Pulse Amplitude Modulation (PAM) only. A frequency threshold for the SBD THz LO beyond which spectrally efficient modulation is not optimal is contributed in this research. In addition the GFET was demonstrated in its viability, by its successful use in all THz analog circuits in the In Phase - Quadrature (IQ) (de-) modulator.

Demonstrated by the high bit rates achieved in this work, Schottky multiplied THz carriers and graphene Field Effect Transistor (FET)s make a cost effective route for

6G wireless as well as Local Area Network (LAN) and Personal Area Network (PAN) within the lower THz range.

KEYWORDS

THz, Schottky, Graphene, 6G, High Bitrate Communication

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ACRONYMS

ADS Advanced Design System
AM Amplitude Modulation
ASK Amplitude Shift Keying
AWGN Additive White Gaussian Noise
BER Bit Error Rate
BJT Bipolar Junction Transistor
BPSK Binary Phase Shift Keying
CL Conversion Loss
CMOS Complementary Metal Oxide Semiconductor
CVD Chemical Vapor Deposition
DC Direct Current
DSP Digital Signal Processing
EVM Error Vector Magnitude
FET Field Effect Transistor
FM Frequency Modulation
FOM Figure of Merit
FSO Free Space Optics
Gbps Gigabits per second
GFET Graphene Field Effect Transistor
GO Graphene Oxide
HEMT High Electron Mobility Transistor
IF Intermediate Frequency
IP3 Third Order Intercept
IQ In Phase - Quadrature
ISI Inter-Symbol Interference
LASER Light Amplification by Stimulated Emitted Radiation
LAN Local Area Network
LNA Low Noise Amplifier
LO Local Oscillator

MESFET Metal Semiconductor Field Effect Transistor

mHEMT metamorphic High Electron Mobility Transistor

mmWave Millimeter Wave

MOS Metal Oxide Semiconductor

OOK On Off Keying

PA Power Amplifier

PAN Personal Area Network

PAM Pulse Amplitude Modulation

pHEMT pseudomorphic High Electron Mobility Transistor

PM Phase Modulation

PSK Phase Shift Keying

QAM Quadrature Amplitude Modulation

QCL Quantum Cascade Laser

QPSK Quadrature Phase Shift Keying

RADAR Radio Detection and Ranging

RGO Reduced Graphene Oxide

RF Radio Frequency

RX Receiver

SBD Schottky Barrier Diode

SNR Signal to Noise Ratio

SPICE Simulation Program with Integrated Circuit Emphasis

sub-mmWave Sub Millimeter Wave

Tbps Terabits per second

THz Terahertz

TX Transmitter

UHF Ultra High Frequency

UWB Ultra Wideband

VCO Voltage Controlled Oscilattor

2D Two Dimensional

8PSK 8 Phase Shift Keying

16APSK 16 Amplitude Phase Shift Keying

16PSK 16 Phase Shift Keying

16QAM 16-ary Quadrature Amplitude Modulation

64QAM 64-ary Quadrature Amplitude Modulation

1

INTRODUCTION

With the rapid growth in data traffic globally and the emergence of 5G Cellular Communication, we can expect to see a range of high bitrate demanding services like Virtual Reality and Machine to Machine communication. Communication at Terabits per second (Tbps) has been accomplished with fibre optics[1]. It is evident that fibre optics will be the supporting wired communications in the near future at all premises. For wireless communication the situation is different. Available Radio Frequency (RF) and microwave spectrum is already crowded up to several tens of GHz. The push is to use wideband communication such as Ultra Wideband (UWB) (which can overlap licensed microwave spectrums with little interference) or higher frequency ranges extending in to millimeter wave, sub-millimeter waves or even Free Space Optics (FSO)[2]. The demand to communicate at higher frequencies is expected to remain after 5G.

Among the prospective technologies for 6G and beyond is Terahertz wireless communication, lying within the infrared transition frequencies of microwaves and optics. This frequency band, between 0.1 - 10THz, presents unique challenges and opportunities. By nature of the large bandwidth, bitrates into Gigabits per second (Gbps) have been reported. It presents itself a viable candidate for local and personal area networks. Since high attentuation is experienced by Terahertz (THz) radiation in the presence of water vapor, such communication is limited to moderate distances[3].

Up to the turn of the 21st century, THz sources were few and expensive[4]. Limited by lack of suitable oscillators, development lagged. However, it now appears that femtosecond Light Amplification by Stimulated Emitted Radiation (LASER) based systems that induce THz radiation on photoconductive antennas provide one solution. Or as an alternative LASER excited nonlinear crystals for generating mixer products in the Terahertz. However prices of such LASER from online store catalogs such as on alibaba.com remains prohibitively expensive in excess of $\$5,000.00$. These LASER are generally Quantum Cascade Laser (QCL). QCLs require layering of different semiconductor materials but have high processing costs. Ultrafast photodiodes have also been used for photo mixing to generate THz[3]. Another method is nonetheless sought which has a cost advantage. A mature technology which is well developed and cost effective is upconversion of microwave sources using the nonlinear characteristics of Schottky frequency multipliers.

An efficient frequency multiplier is a varactor diode having a capacitance that varies with voltage to the inverse square root for an abrupt uniformly doped junction[5]. At THz a suitable such diode is a Schottky junction capable of fast switching speeds[6]. Frequency multiplier produce m-order sums and differences of multi-

ples of the input angle, after which filtering is employed to get the corresponding desired product. This prospect leads the way to generating the carrier frequency. However the challenges that arise with this technique is that the phase error in the input will double, and multiply at the output of consecutive frequency multipliers.

Employing frequency multiplicaton using Schottky diodes THz communication is possible but is hampered by the phase noise. This phase noise by nature can be reduced by design but within limits. And so arbitrary higher frequencies trade off with phase fidelity. Modern digital communication systems use both combinations of digital amplitude and phase modulation schemes such as Quadrature Amplitude Modulation (QAM) as this would be chosen for spectral efficiency[6]. It is also known that THz waves have high attenuation rates. Combined with the phase noise present in such frequency multiplication schemes, acheiving modulation gains is difficult.

A high oscillator frequency has a drawback in that the multiplication process incurs a substantial power loss due to the limited conversion efficiency of the Schottky devices[7]. The low oscillator power aggravates the higher phase noise.

Transistor technology for Millimeter Wave (mmWave) and Sub Millimeter Wave (sub-mmWave) are an area of active development. Indium Phosphide transistors have been reported with 0.67THz cut off frequencies, though not yet readily available in a commercial setting[8]. Indium Gallium Arsenide transistors have likewise been developed[9]. The relatively recent discovery of graphene with remarkable electronic properties has stirred up research into using it for RF devices amongst others. Graphene is a single layer carbon nanosheet. Graphite is formed from several graphene layers. Numerous methods have been identified for extracting mono and few layer graphene such as solution exfoliation, liquid phase exfoliation and Chemical Vapor Deposition (CVD)[10]. High quality graphene is a targeted and active research area. Graphene Field Effect Transistor (GFET) with a theoretical record high electron mobility and cost reduction in comparison to other THz High Electron Mobility Transistor (HEMT)s, make graphene a strong candidate for cost effective RF transistor technology[11].

In this work, spectrally efficient THz communication is investigated using frequency multiplication of microwave oscillators. The promising GFET is used as the THz transistor technology.

1.1 STATEMENT OF THE PROBLEM

To attain the THz frequencies for high bit rate communication in 6G wireless communication Schottky based sources present a low cost option over photonic approaches.

Terahertz sources, using Schottky diodes, have been implemented widely in systems with On Off Keying (OOK) modulation. Due to compounding phase noise

extension to digital phase modulations has not been addressed sufficiently and must be analysed and understood to what extent it can be utilized for enhanced data rates.

1.2 OBJECTIVE

General Objective

The general objective is to do a performance analysis of a Schottky based Transceiver at THz in liu of the phase noise inherent in such a scheme.

Specific Objectives

The specific objectives of this thesis are:

- Design a Schottky Terahertz Tranceiver
  - Optimize the design with respect to digital phase modulation
- Evaluate the performance of the transceiver in a Additive White Gaussian Noise (AWGN) channel
- Summarize the findings for different PSK and QAM modulation schemes.

1.3 SCOPE AND LIMITATIONS

In this research, only Zero-Intermediate Frequency (IF) or Direct conversion architecture as well as double conversion architecture is used for the transceiver. In addition to this practical issues such as synchronization and channel estimation have been neglected.

Regarding THz transistor technology this work is limited to GFET.

Regardless of the constraints and limitations chosen, the validity of the findings is not limited.

1.4 CONTRIBUTIONS OF THE RESEARCH

There are a plethora of research outcomes in the area of THz communication, however, none of them addresses how far we can extend frequency multiplications usefully within the limits of phase noise. Also the design considerations for the LO of a THz communication transceiver is addressed. Graphene technology has been used as a material for direct detection and modulation/demodulation of the THz waves. The GFET as the primary device technology for all THz RF/analog processing in a traditional In Phase - Quadrature (IQ) scheme is contributed in this work. High bitrate communication is demonstrated with Schottky diode frequency multiplication and GFET technology.

1.5 LITERATURE REVIEW

Terahertz communication is seen as the technology for 6G wireless standard with both photonic and electronics based transceivers. Of the transceivers documented in literature, Elayan et al in 2018 [12] provided a comparison of THz transceivers reported. The photonic approaches provided higher bit rates than those with electronic implementations. It was noted that Graphene device technologies may provide the best solution for THz devices. However in 2016, Song et al. outlined emerging sources at THz pertinent to communication[13]. It is noted that the Schottky barrier is gaining in popularity; however, there are also high expectations for Resonant Tunnel Diodes (that operate on a negative IV differential). It can be seen from these that both electronics and photonics approaches are being developed and promising to meet the THz gap.

Several transceivers have been reported that corroborate the applicabilty and benefits of the THz band. In 2015 Kanno A. et al implemented a photonic based transceiver with a 1Gbps data source and OOK modulation at a 300GHz carrier ferquency[14]. That same year, a group of researchers at San Jose State University, demonstrated an OOK 210GHz transceiver using Complementary Metal Oxide Semiconductor (CMOS) technology with a bit error rate of 10^{-12}[15]. Using Schottky frequency multiplication, Guo et al. in 2015 attained a Terahertz communication link at 340GHz and achieved a bitrate of over 30Gbps[16]. Gallium Arsenide Schottky barrier diodes were employed. Additionally link budget analysis was conducted to obtain comparison of several modulation schemes.

With Schottky frequency conversion, progress is being made. Liu et al. in 2015[17] reported a 160GHz source with 35mW power. The same in 2017[18] increased the frequency to 360GHz - at about a third of the power available from the 2015 paper. Siles et al. in 2015 also performed relatively efficient Schottky multiplication to mmWave (105-120GHz) and sub-mmWave (170-200GHz) with efficiencies of 30% and 25% respectively[7].

Modulation schemes employed have been mostly OOK modulation. Nagatsuma et al. in 2016, reviewed the advances that had occurred in THz communication. A table comparing the best performance results were documented and it can be seen that Schottky Barrier technologies were employed in either Amplitude Shift Keying (ASK) or OOK[19]. In 2016 Yao[20] put the modulation schemes in perspective for THz wireless communication. OOK was pointed out to be inefficient spectrally, though much simpler to implement. This fact is not new to the Terahertz band but higher order modulation schemes are necessary for equitable utilization. Hence Yao in 2016, studied 16QAM, 16 Phase Shift Keying (16PSK) and 16 Amplitude Phase Shift Keying (16APSK) in an AWGN. In 2014, Boes et al.[21] reported 8 Phase Shift Keying (8PSK) modulation at 240GHz and noted that the system was not suitable for amplitude modulation. Recently Dan et al.[22] in 2020 reported a proof of concept 16-ary Quadrature Amplitude Modulation (16QAM) modulation at 300GHz, using the same 35nm InGaAs transistor technology.

To enable communication with Schottky diodes at THz frequencies low phase noise microwave oscillators are needed. Lee H. and Mohammadi S. attained a low phase noise oscillator with -106dBc/Hz at 400kHz offset, using a CMOS Voltage Controlled Oscilattor (VCO).[23]. A low phase noise HEMT oscillator was reported by Lai et al. in 2014 including a comparison of a negative resistance- and Colpitts-based oscillators using the same transistor[24]. The negative resistance oscillator had superior performance but operated at a lower frequency than the Colpitts oscillator at a 1MHz frequency offset. A digitally synthesised oscillator that had a phase noise of -140dBc/Hz at 1KHz offset[25] has also been attained by Lesage J. and Penn J in 2017.

Graphene as a semiconductor has a zero band gap making it distinct from most semiconductors with non-zero bandgap. As a result the transfer characteristic of GFET is different. Fregonese et al. in 2013 developed a model useful for simulation[11]. Rodriguez et al. in 2014 used this model to obtain simplified relations for hands on analog design purposes[26].

To resolve the THz gap, Schottky based oscillators play an important role. However, to attain better utilization of spectrum using Schottky based oscillators, digital phase modulation has to be employed in cohort to Pulse Amplitude Modulation (PAM). This enables higher bit rates than with OOK, ASK or Phase Shift Keying (PSK) alone. An examination of the performance is necessary to see the extent communication is viable with digital Phase Modulation (PM) in the midst of phase noise and limited power.

In this work, the optimal range for the the THz LO using SBD multipliers and spectrally efficient modulation is examined by both the phase noise and output power at multiple THz frequencies. Previous work focused on either output power as the performance criteria or a single frequency was used. Much work on THz transceivers has been accomplished with InGaAs and InP transistors hence the GFET is employed in this work to contrast.

1.6 METHODOLOGY

In order to execute the research, a methodology was prepared and can be seen in Figure 1.1. Beginning a selection of a microwave transistor with low noise figure and high operating frequency was made from online electronics databases. The chosen microwave transistor was then used to design the microwave oscillator and subsequently multiplied with the SBD to THz until the phase noise and output power became unsatisfactory. A mixer was then designed with the GFET and followed by Power Amplifier (PA), Low Noise Amplifier (LNA), IF and baseband amplifier design. Using these active circuits and filters the Zero-IF modulator and demodulator was simulated along with the necessary signal processing. Following the diode mixer and x2 GFET subharmonic mixer were designed. The diode mixer was then employed in addition to the amplifiers and active fundamental mixer to construct a double conversion architecture and performance evaluated for several modulation schemes.

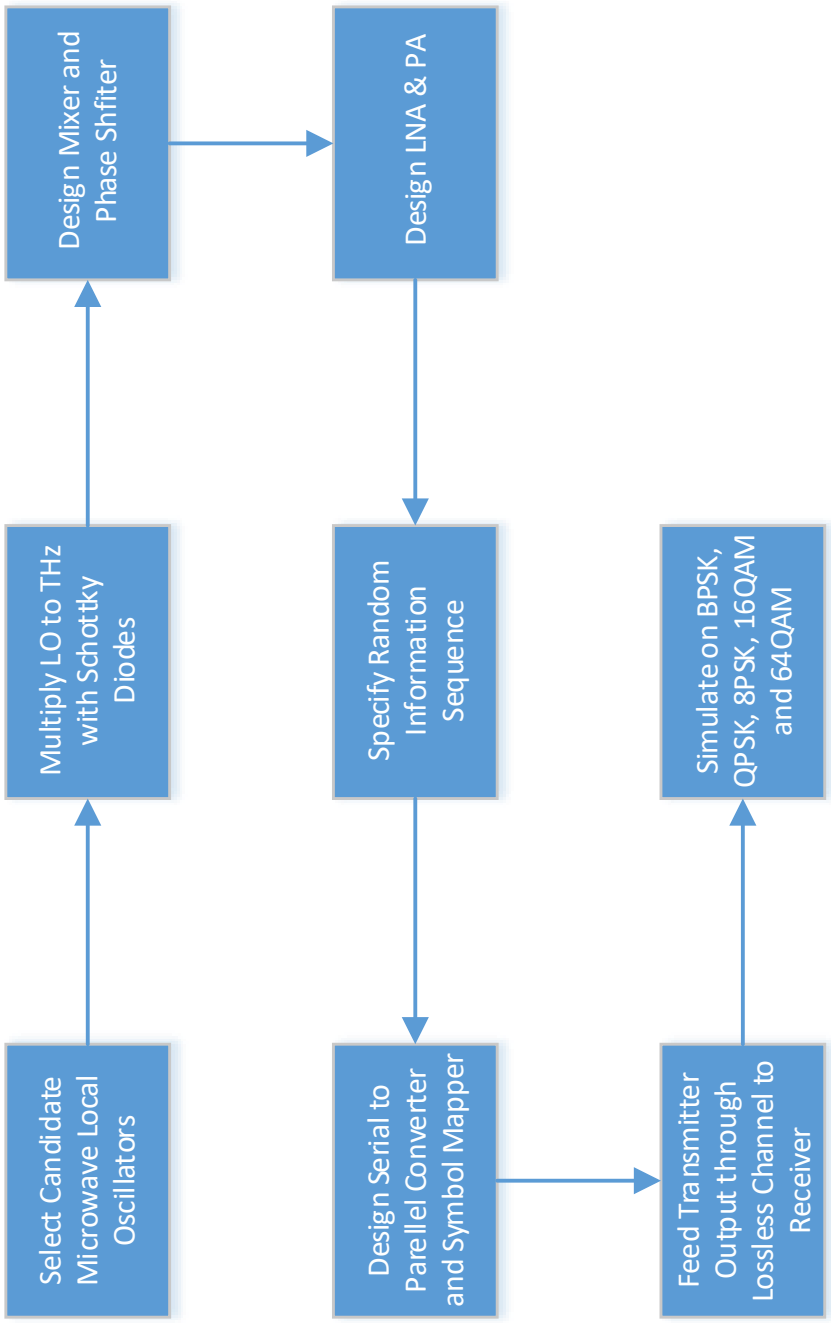


Figure 1.1: Procedure Followed Presented as Flow Chart

2

NONLINEAR CIRCUITS AND PHASE NOISE

In essence all devices are nonlinear; however, depending on the operating condition a circuit can be approximated as linear with the attending simplicity of analysis. In contrast, when a circuit is intentionally operating where nonlinear effects are used, this is generally classified as nonlinear circuit. Mathematically the difference between a linear circuit and a nonlinear circuit, is the same as the difference between a linear equation and nonlinear equation. The standard definition of linear being the applicability of superposition equation (see eq 2.1). Nonlinear equation or circuit in the general class is infinitely varied (eq 2.2). In these equations x is the independant variable and y the dependant variable.

$$y = a_0 + a_1 x \tag{2.1}$$

$$y = \sum_{k=0}^{K} a_k x^k \qquad K > 1 \tag{2.2}$$

2.1 OSCILLATOR

An oscillator is a quasilinear circuit and unstable at startup but stabilizes at steady state to a fixed frequency. Two broad classes exist for oscillators: negative resistance based and feedback based. Both operate similarly by providing a reflection coefficient $\Gamma > 1$ and loop gain of $G_{loop} > 1$, respectively. At startup there is amplitude growth but eventually a point is reached by the oscillator at steady state where the $\Gamma = 1$ and loop gain $G_{loop} = 1$ at a particular frequency[27].

In a communication system, for carrier synchronization a VCO is used where the oscillation frequency and phase is tuned to replicate the transmit oscillator. This can be done by tuning capacitive feedback in a Colpitts topology or by tuning inductive feedback in a Hartley topology. In this thesis, a Colpitts oscillator the preferred topology, has been employed. It is preferred by reason of the convenience of varactor diode applicability[28].

2.1.1 *Colpitts Oscillator Design*

Referring to Figure 2.1, the oscillator consists of an (inverting) amplifier with gain A and a feedback network with a gain of β. By designing the feedback to satisfy the Barkhausen criteria at a specific frequency we obtain an oscillator (see eq 2.3)[28].

The oscillation frequency is given in eq 2.4, and the feedback factor is obtained

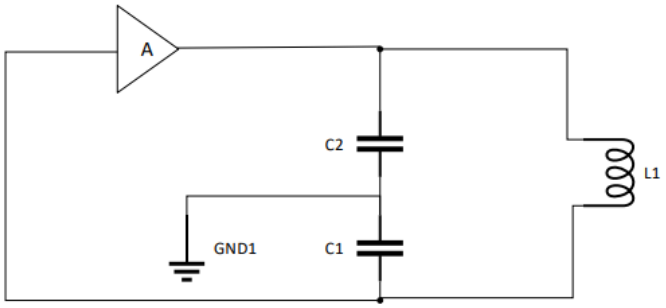


Figure 2.1: Colpitts Oscillator with Inverting Amplifier [28]

in eq 2.6. C_1 and C_2 are the capacitances in Figure 2.1, whilst C_T is the combined equivalent capacitance. L_1 is the inductance in Figure 2.1.

$$A\beta = 1 \tag{2.3}$$

$$f_o = \frac{1}{2\pi\sqrt{L_1 C_T}} \tag{2.4}$$

$$C_T = \frac{C_1 C_2}{C_1 + C_2} \tag{2.5}$$

$$\beta = \frac{C_2}{C_1} \tag{2.6}$$

2.1.2 *Phase Noise*

Rather than amplitude noise the main source of non ideality in an oscillator is phase noise. An oscillator can be said to amplify noise and selectively filter the desired frequency while applying positive feedback. Naturally from this description, the filter with a finite quality factor will not completely attenuate frequencies beside the center frequency. Therefore, a spread is present in the output spectrum of the oscillator in a similar form to that of the filter selectivity. Another viewpoint is that the noise rich in phase variation will satisfy the oscillator Barkhausen criteria regardless of phase shift and the oscillator results in a time varying phase. The time varying phase will appear as a spread of frequencies around the center frequency by the same reason as the equivalence of Frequency Modulation (FM) and PM. An approximate mathematical model was given by Leeson[27]. Phase noise can be measured with a spectrum analyzer or alternatively simulated with software such as Advanced Design System (ADS).

Phase noise is significant as it is an inherent non-ideality in an oscillator. When an oscillator is used in PM, the phase contains information and the oscillator phase noise contributes a loss of precision to this information and possible complete loss.

2.2 FREQUENCY MULTIPLIERS

A frequency multiplier uses the nonlinear characteristics of passive and active devices to generate harmonics of the input function. Frequency multipliers can be used in cohort with frequency dividers to create an overall fractional multiplication. For THz generation, integral multipliers are more common[3].

The decision which type of device to use for frequency multiplication is application specific. With diodes it is possible to use either a varistor or varactor mode. Varistors being variable resistors have more noise, lower conversion efficiency and higher bandwidth than varactors. Varactors have low noise, high efficiency and narrow bandwidth. Varactors is the term used for a semiconductor capacitor relying on the varying depletion region capacitance. This approach adds less noise as there is a low series resistance where the bulk semiconductor is the main source of resistive losses and thermal noise. For low phase noise applications, thermal noise should be minimized, thus leading to varactor multiplication as the preferred technique for THz generation. Schottky Barrier Diode (SBD) with high electron mobility and low loss, are the class of diodes used at THz frequency by nature of their fast switching capability[29].

Active devices such as Field Effect Transistor (FET)s can be used as frequency multipliers. These have simultaneously higher efficiency and higher bandwidth than varactor diodes. Nonetheless there is more noise power which is depending on the requirements undesirable. An ideal frequency multiplier degrades the Carrier to Noise Ratio (CNR) where N is the multiplication order, according to eq 2.7[29].

$$\Delta \mathrm{CNR} = 20 \log(\mathrm{N}) \tag{2.7}$$

Varactor Frequency Multiplier Design

The design of a x2 Schottky frequency multiplier using the classic procedure by Burckhardt will be summarized[29]. In order to begin design, the reverse biased diode capacitance plays an important role. A good figure of merit for a diode is the dynamic cut off frequency given by eq 2.8. S_{max} and S_{min} are the elastances (inverse capacitances) at the two operating extremes of the (reverse biased) diode and Rs is the series resistance. This cut off frequency, F_{cd}, should be at least 50 times the frequency to be multiplied for Burckhardt's procedure to be accurate[29].

$$F_{cd} = \frac{S_{max} - S_{min}}{2\pi \mathrm{Rs}} \tag{2.8}$$

An idler is employed to allow only one frequency to excite the diode. An idler can be characterized as an open-circuit or short circuit termination on the varactor

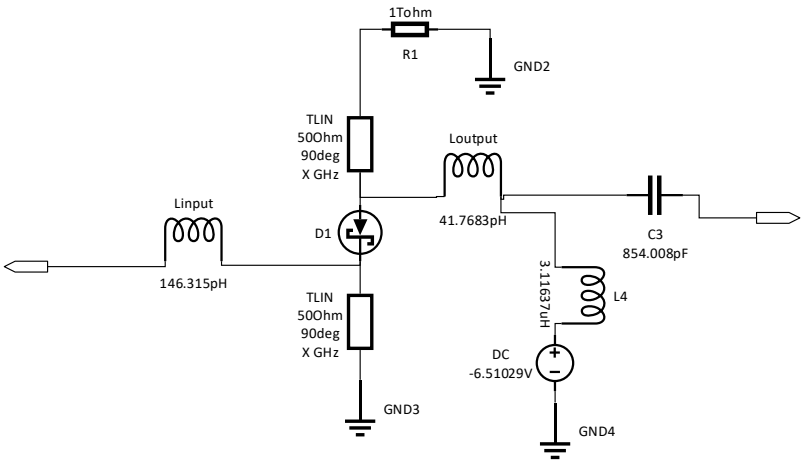


Figure 2.2: x2 Frequency Multiplier - 23.23 GHz to 46.46 GHz

diode at the fundamental or harmonics. These idlers permit frequency multiplication to be easily done without subsequent filtering of undesired harmonics. The idler is implemented by the two stubs at 23.23GHz (see X in Figure 2.2). In effect the diode input (cathode) is grounded by the short circuit stub, preventing any input excitation beyond the fundamental frequency. The open circuit stub serves as a ground to the fundamental with little difference to any higher harmonics. Varactor multipliers without idlers have several harmonics exciting and contributing in the multiplication. However, multipliers without idlers need open circuit stubs at the output of the multiplier. That is subsequent to C3 in Figure 2.2, to remove the undesired harmonics. Since several harmonics are present in the output matching network, highly broadband inductors are necessary and these cannot be implemented with simple distributed narrowband stubs or pattern type elements, making fabrication very difficult. With the idler in place the input and output matching can be designed based on the minimum capacitance of the diode and eqs 2.9 and 2.10 give the matching inductor values. L_{input} and L_{output} are inductances in Figure 2.2. In addition a Direct Current (DC) bias is necessary as shown. Highest efficiency for the DC bias is found close to the breakdown voltage. Once the topology is setup with these values, an optimization can be done with unconstrained nonlinear minimization algorithms. One such algorithm group is the random search method, where randomnly picked values can be used for the variables until a minimum is reached[30]. For this particular application the variables are the inductor, capacitor and DC voltage values and the values chosen for modification minimize a cost function based on highest conversion efficiency. These algorithms as implemented in ADS can be used to obtain optimum component values for efficiency and DC biasing.

$$L_{input} = \frac{1}{(2\pi f)^2 \frac{1}{0.5 * S_{max}}} \tag{2.9}$$

$$L_{output} = \frac{L_{input}}{4} \tag{2.10}$$

In the procedure for Burckhardt, there is also input and output resistive matching. These were found to only reduce conversion power efficiency more than matching loss reduction and thus were ignored.

2.3 MIXERS

A mixer is an essential nonlinear circuit used in carrier based communication circuits. The function being frequency translation, by multiplying the carrier frequency with the input IF or RF signal in the time domain. Ideal fundamental mixers, are generally desired to produce only second order products. However, practical mixers produce higher order mixer products. It is found that mixers performance is limited by these higher products. Characteristics such as gain compression and Third Order Intercept (IP3) are used to model them[29].

Like frequency multiplier, mixers can be designed with passive or active semiconductor devices. The passive devices, SBD being the most common can achieve mixing with a single diode. For better performance balanced two to four diode mixers are prevalent. These mixers presume the local oscillator power is high enough to forward bias the diode. This is not usually so at THz and thus active devices with better sensitivity are used[29].

The principle design of a mixer involves matching the LO, RF and IF at their respective frequencies to the nonlinear device(s). There are a myriad of mixer circuits. An exhaustive discussion can be found in standard RF books[29][6][31]. A fundamental mixer produces the desired output centered at that of the local oscillator frequency. However, a subharmonic mixer is intended to generate an output at higher harmonics of the local oscillator thus providing good isolation of the LO from the output.

3

THZ DEVICE TECHNOLOGIES

In electronics generally device materials and design varies with the intended frequency of operation. Thus at THz, transistors have to have high enough electron mobilities to support the high frequency signals[31]. Hence InP HEMTs, InGaAs HEMTs and GFETs, are found to meet the requirement.

In general for high frequency circuits parasitic capacitances present in FET devices limit the cut off frequency. Therefore, to improve the performance for THz transistors, the gate device dimensions have to be reduced. In particular the gate length can be reduced as it factors into the magnitude of the capacitances. The gate width can also be reduced, to this aim, however this limits the maximum drain source current and is thus done sparingly. The electron mobility of the semiconductor is the other important parameter. As the device shrinks in gate length high mobility accounts for a higher current due to a higher conductivity[31].

3.1 BASICS OF HIGH ELECTRON MOBILITY TRANSISTORS

Before HEMTs were available the primary microwave transistor was GaAs Metal Semiconductor Field Effect Transistor (MESFET) (see Figure 3.1). The operating principle of this transistor is typical of FETs where the primary advantage is the higher electron mobility of GaAs over Silicon Bipolar Junction Transistor (BJT)s. By varying the gate voltage, the channel can be varied from effectively open circuit to very low resistances and this is also characteristic of HEMT. However, it is to be noted that doping in general at high doping concentrations lowers the electron mobility. To circumvent this problem, HEMTs were proposed. A HEMT has a structure

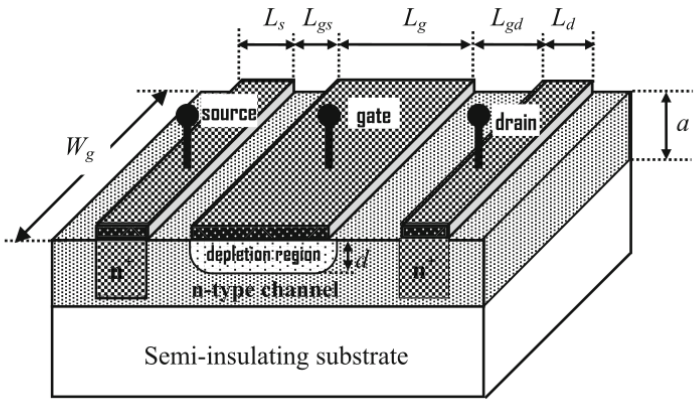


Figure 3.1: Structure of a GaAs MESFET[31]

such as shown in Figure 3.2. A HEMT is charaterized by the presence of a higher band gap material in this case AlGaAs over an undoped high mobility semicon-

ductor, in this case GaAs. As a result of the doping in the n-type AlGaAs and the higher energy level, electrons diffuse from the AlGaAs to the GaAs; thereby forming a thin layer of electrons within the GaAs and confined to a potential well in the GaAs substrate known as a Two Dimensional (2D) electron gas. It is to be noted in Figure 3.2 that there is a spacer layer of undoped AlGaAs. This thin layer is there to reduce the effect on the electron gas as a result of any donor ions in the n-type AlGaAs layer. The figure portrays a lattice matched HEMT. There are

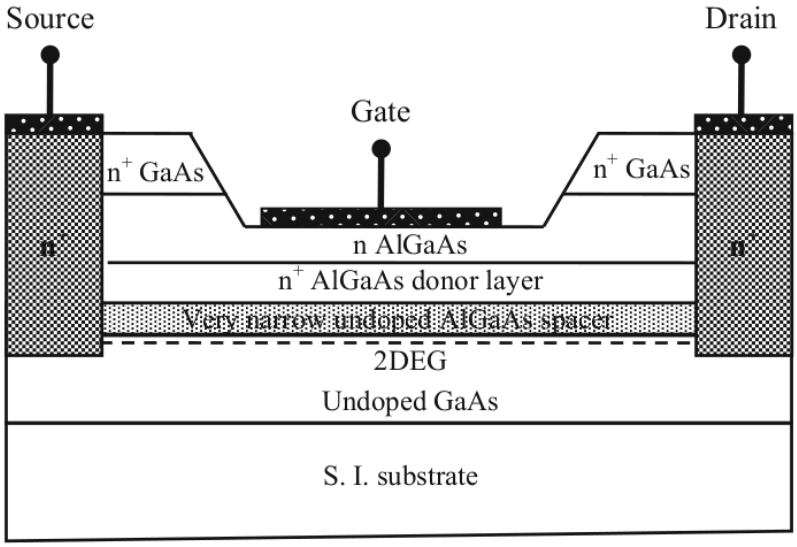


Figure 3.2: Structure of a AlGaAs/GaAs HEMT[31]

also pseudomorphic and metamorphic HEMTs. Each classification deals with the lattice strain at the high band gap semiconductor and the undoped semiconductor material[31]. Lattice strain is a way of describing and quantifying the crystal lattice constant mismatch at different semiconductors. Pseudomorphic depicts a case where the mismatch is relatively small. The higher band gap material due to the strain changes the lattice shape by the Possion effect and thus is deformed to make a match. Metamorphic on the other hand indicates a gradually changing lattice constant, from the surface of the substrate to that of the higher band gap material[32].

Materka Model

The Materka model is widely used for HEMTs[27], and the equation as used in ADS is given in equations 3.1 - 3.3. α and λ are constants. V_{gs}, V_{ds} and V_{to} are the gate source, drain source and gate turn off voltages respectively. I_{ds} and I_{dss} are the drain source current and saturation current, respectively. λ is known as channel length modulation constant and is related to the Early effect.

$$TI = |\alpha V_{ds}| \tag{3.1}$$

$$F = \frac{TI}{V_{gs} - V_{to}} \tag{3.2}$$

$$I_{ds} = I_{dss}(\frac{V_{gs}}{V_{to}} - 1)^2 tanh(F)(1 + \lambda V_{ds}) \tag{3.3}$$

3.2 GRAPHENE FIELD EFFECT TRANSISTORS

Graphene, a semiconductor with zero band gap, has attained great attention from the day it was first discovered. Having the highest electron mobility known[10], it is promising for RF active device applications. GFETs take the form of Metal Oxide Semiconductor (MOS) with much active research[11]. As a result of the zero band gap, graphene can switch from electron conduction to hole conduction (that is from n-type to p-type) solely with gate bias[33]. Several methods are yet being explored for graphene synthesis in particular with the top down approach. The top down approach is more cost effective however has more crystal defects than that of the bottom up approach such as CVD[10]. The most popular top down approaches being solution exfoliation and liquid phase exfoliation. The first involves oxidation and expansion exfoliation of graphite flakes to form Graphene Oxide (GO). The GO is then chemically reduced to form Reduced Graphene Oxide (RGO), that is graphene with some defects[10]. Liquid phase exfoliation can be be done using expanded graphite and high power sonication to fully exfoliate the graphite worm structures[10].

Graphene Field Effect Transistor Device Equations

The GFET device model equations are listed inr the following equations[11]. C_{top} in eq 3.4 is the gate capacitance, where A is the channel area and d the gate thickness. V_{GSi} and V_{DSi} is the internal gate source voltage and internal drain source voltage respectively. e is the charge of an electron. N_f is the acceptor minus donor doping concentration. v_f is the fermi velocity. Q_{netAV} is the average channel charge. ω is the surface phonon charge divided by Plancks reduced constant. n_{puddle} is a quantity dealing with crystal inhomogeneity induced charge. I_D is the drain source current. C_{GS} and C_{GD} is the gate source capacitance and gate drain capacitance, respectively. The remaining variables are derived quantities with no particular physical significance.

$$C_{top} = \frac{\epsilon A}{d} \tag{3.4}$$

$$s = sign((C_{top}(V_{GS_i} - V(x)) + eN_f) \tag{3.5}$$

$$\beta = \frac{e^3}{\pi \hbar v_f} \tag{3.6}$$

$$Q_{netAV} = \beta s(\frac{-C_{top} + \sqrt{C_{top}^2 + 4\beta|C_{top}(V_{GSi} - \frac{V_{DSi}}{2}) + eN_f|}}{2\beta})^2 \tag{3.7}$$

$$J_{denom} = L + \mu\frac{(\pi\frac{|Q_{netAV}|}{e} + n_{puddle})^{0.5}}{\omega}|V_{DSi}| \tag{3.8}$$

$$z2 = C_{top}(V_{GSi} - V_{DSi}) + eN_f \tag{3.9}$$

$$z1 = C_{top}V_{GSi} + eN_f \tag{3.10}$$

$$J_{num1} = -\frac{1}{12e\beta^2 C_{top}}[6\beta C_{top}^2 z_{1,2} - 6\beta^2 z_{1,2}^2 + C_{top}(C_{top}^2 - 4\beta z_{1,2})^{3/2}] \tag{3.11}$$

$$J_{num2} = -\frac{1}{12e\beta^2 C_{top}}[6\beta C_{top}^2 z_{1,2} + 6\beta^2 z_{1,2}^2 - C_{top}(C_{top}^2 + 4\beta z_{1,2})^{3/2}] \tag{3.12}$$

$$J_{z_2} = J_{num1} \qquad z2 < 0 \tag{3.13}$$

$$J_{z_2} = J_{num2} \qquad z2 > 0 \tag{3.14}$$

$$J_{z_1} = J_{num1} \qquad z1 < 0 \tag{3.15}$$

$$J_{z_1} = J_{num2} \qquad z1 > 0 \tag{3.16}$$

$$J_{num} = J_{z_2} - J_{z_1} \tag{3.17}$$

$$I_D = e\mu W\frac{J_{num} + n_{puddle}V_{DSi}}{J_{denom}} \tag{3.18}$$

$$v_{satAV} = \frac{\omega}{\sqrt{\pi(\frac{|Q_{netAV}|}{2} + n_{puddle})}} \tag{3.19}$$

$$E_{AV} = \frac{1}{\frac{(|Q_{netAV}|+en_{puddle})\mu W}{I_D}|\frac{\mu}{v_{satAV}}} \tag{3.20}$$

$$I_{num1} = -\frac{1}{12e\beta^2 C_{top}}[6\beta C_{top}^2 z_{1,2} - 6\beta^2 z_{1,2}^2 + C_{top}(C_{top}^2 - 4\beta z_{1,2})^{3/2}] \tag{3.21}$$

$$I_{num2} = -\frac{1}{12e\beta^2 C_{top}}[-6\beta C_{top}^2 z_{1,2} - 6\beta^2 z_{1,2}^2 + C_{top}(C_{top}^2 + 4\beta z_{1,2})^{3/2}] \tag{3.22}$$

$$I_{z_2} = I_{num1} \qquad z2 < 0 \tag{3.23}$$

$$I_{z_2} = I_{num2} \qquad z2 > 0 \tag{3.24}$$

$$I_{z_1} = I_{num1} \qquad z1 < 0 \tag{3.25}$$

$$I_{z_1} = I_{num2} \qquad z1 > 0 \tag{3.26}$$

$$I_{num} = I_{z_2} - I_{z_1} \tag{3.27}$$

$$Q_{ch} = eW\frac{I_{num} + n_{puddle}V_{DSi}}{E_{AV}} \tag{3.28}$$

$$C_{GS} = -\frac{\delta Q_{ch}}{dV_{GS}} \tag{3.29}$$

$$C_{DS} = -\frac{\delta Q_{ch}}{dV_{DS}} \tag{3.30}$$

4

TRANSCEIVER ARCHITECTURES

When designing a receiver or transmitter it is necessary to decide on an architecture. This decision entails a large part on the type of modulation scheme, bandwidth and complexity. There are several topologies where an all digital system is seen as the ideal[34]. However at THz frequencies sampling at Nyquist rate with sufficient quantization granularity is very difficult and expensive. Currently, the most used architecture at THz is the Zero-IF and the double conversion superheterodyne[22][21]. The Zero-IF architecture is known for its simplicity and compactness due to no IF stage filters. In addition, to the simplicity there is no image problem. The image problem is where an undesired transmit channel separated by two times the IF center frequency (from the desired band), makes its way into the receiver. Once the image frequency has been mixed with the desired band there is no way to remove it. This is a situation which has to be avoided. The double conversion architecture which is the most used in communication[27], is more complex than the Zero-IF. However the double conversion can be designed to have no image problem and can avoid the DC offset problem in the Zero-IF topology.

4.1 SINGLE CONVERSION SUPERHETERODYNE

A single conversion superheterodyne consists of only one IF and therefore only one mixer. In general a single conversion can have any low frequency center but more commonly a center frequency of DC is chosen resulting in Zero-IF[6]. There are several challenges with the single conversion architecture. The IF at a frequency other than DC is prone to the image problem as the image can make its way into the received signal. The way to avoid this is to either use highly selective band select filters or even better convert the IF to a larger frequency than the maximum baseband frequency by 35% or more[35]. The first approach makes the filter order large and the resulting circuit bulky. The second approach makes use of large frequency separation of the image from the desired band. This ensures that the image falls in the stop band of the band select filter. At an IF of DC there is no image problem, however there is a DC offset issue. With Zero-IF the LO can make it's way into the transmit band and mix at the receiver to form a DC value. A DC offset shifts the symbols and biases to one symbol or symbol group. Figure 4.1 shows the topology which can either be a Zero-IF or any other low IF.

4.2 DOUBLE CONVERSION SUPERHETERODYNE

Double conversion as the name implies has two IF stages (see Figure 4.2). Higher IF filter selectivity to bandwidth can be achieved more easily in stages. A draw back of the single conversion architecture is that narrow filter selectivity at higher frequencies is not readily possible. This is where double conversion alleviates the

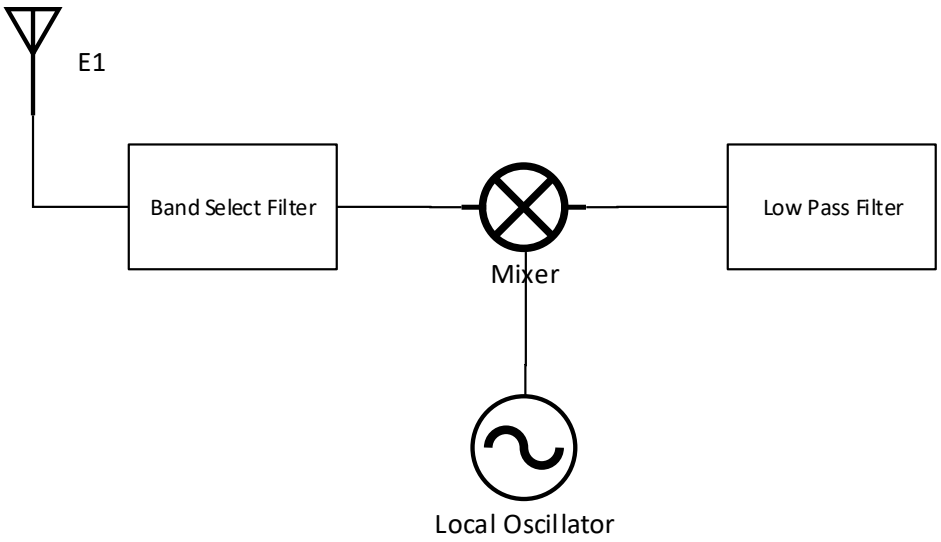


Figure 4.1: Single Conversion Architecture

problem by using a second lower IF. Due to the versatility it forms a popular group of the superheterodyne in communication circuits[27]. Figure 4.2, shows a double conversion architecture which can be represenative of a BPSK modulation.

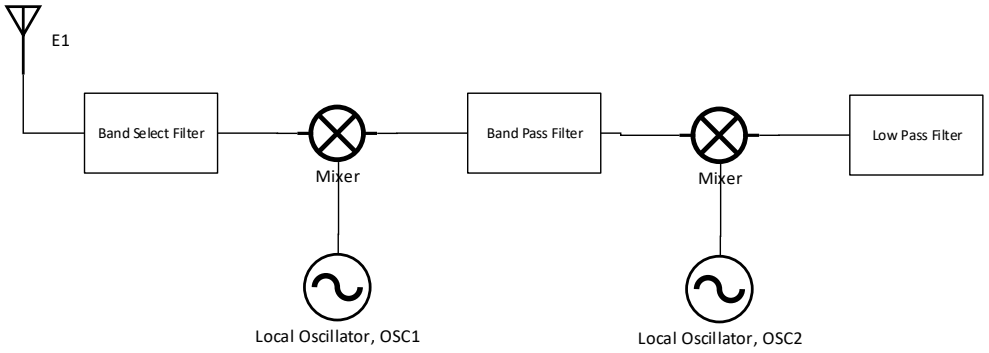


Figure 4.2: Double Conversion Architecture

4.3 ERROR PERFORMANCE

When assessing a transceiver in particular the receiver, the Signal to Noise Ratio (SNR) is an important figure. It has a direct effect on correct demodulation. As a means to reflect the distortion present in a transceiver the Bit Error Rate (BER) or Error Vector Magnitude (EVM) can be used as both are dependant on the SNR.

The BER shows how many of the symbols, were incorrectly decoded. Whereas EVM shows the average magnitude of the error vector from the ideal constellation point magnitude.

5

EXPERIMENTAL SETUP

In order to assess the performance of SBD THz oscillator frequencies and communication transceiver performance a design procedure was conducted of a complete transceiver and the metrics evaluated by simulation. For the design and simulation Keysight ADS was chosen as it is well established and well featured[27]. In this chapter, what can be found is the design procedures comprising the individual components that are combined to form the entire transceiver. Harmonic balance simulation was employed for the RF circuits and ADS Ptolemy RF/Digital Signal Processing (DSP) co-simulator for the complete transceivers. Since phase noise can be reduced by designing lower noise figure circuits and overall performance improved significant emphasis was endued to low noise circuits.

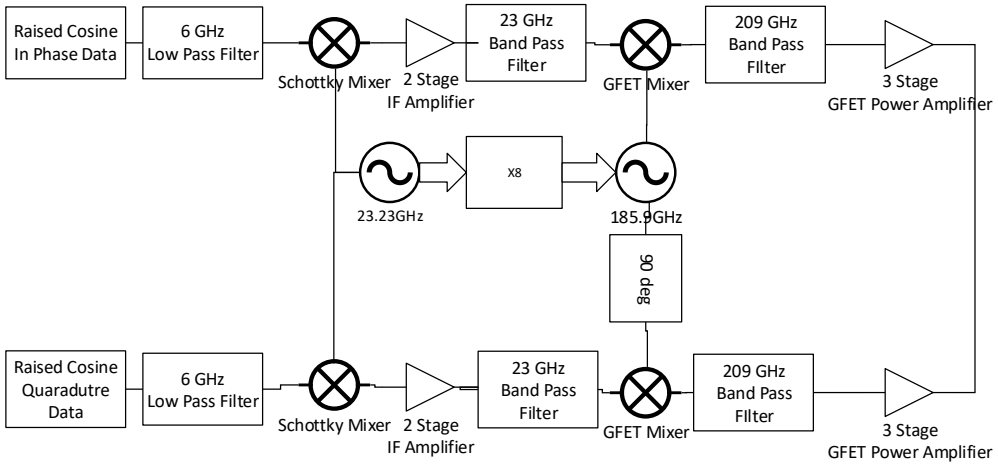
5.1 VALIDATION OF SETUP

Due to the novelity of THz communication, there are limited number of papers operating under similar frequency range and application area. Therefore the circuits and setup were validated by comparison with similar component level designs by Chen et al. in 2015 for the THz oscillator, Andersson et al. in 2012 for the GFET PA and Zhang et al. in 2016 for the GFET mixer[36][37][38]. The GFET device model used in the active circuits was also verified with results in Rodriguez et al in 2014[26] using the device parameters reported. To assess the error performance of the complete transceivers the system level figures were compared with the novel papers by Boes et al. in 2014, Dan et al. in 2020 and Kalfass et al in 2017[21][22][39].

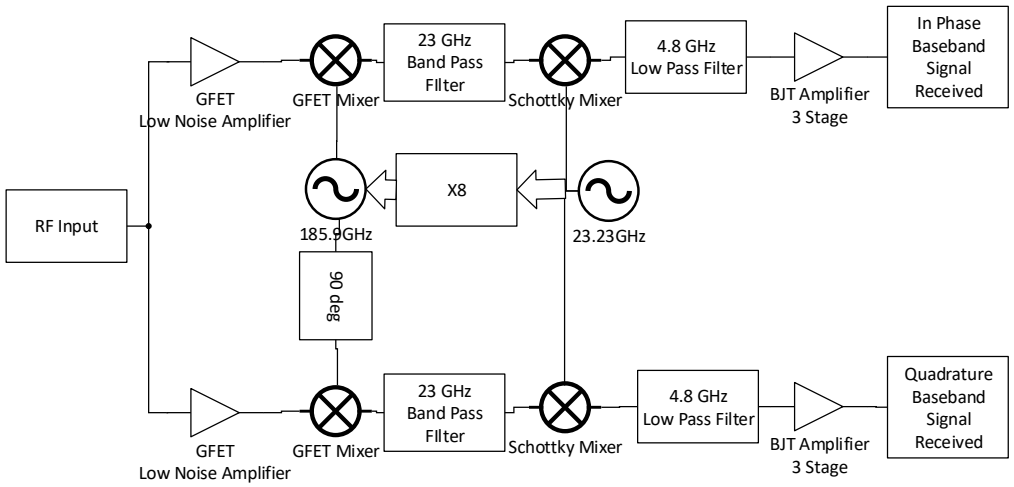
The double conversion transmitter and receiver can be seen in Figure 5.1. In the following subsections the individual component design will be discussed. The DSP used will conclude the chapter.

5.2 LOW PHASE NOISE MICROWAVE OSCILLATOR

Since the noise figure of the transistor selected will have a significant impact on the phase noise, a selection was made from commercial transistors with the highest Figure of Merit (FOM). The FOM in this decision was the product of cut off frequency and the inverse of noise figure. As a result of the high electron mobility of GaAs the noise profile is low at high frequencies and simplified the search in terms of device material. The microwave transistor selected was a GaAs HEMT with part number CE3520K3. The transistor selected was used to set the parameters according to Materka model for the HEMT. This was done by entering the turn off voltage of $-0.75V$, the drain source saturation current of $40mA$ and the calculated α from a bias condition into the model parameters. To compute α a gate source voltage of $-0.1V$, drain source voltage of $0.3V$, drain source current of $30mA$, turn



(a)



(b)

Figure 5.1: Double Conversion Transmitter (a) and Receiver (b)

off voltage of $-0.75V$, drain source saturation current of $40mA$ and channel length modulation of 0 were entered into the Materka model equation and solved for α. The equations for the Materka model can be found in Section 3.1. To keep the device safely within the maximum power limit $30mA$ was chosen and a DC bias voltage of $4V$ as this is the breakdown voltage. Using the plots in the datasheet a gate source voltage of $-0.1V$ is necassary to bias the current at $30mA$. However, as a result of the insufficient gain for oscillation a $30mA$ current source was used to provide higher gain. The $-0.1V$ gate source voltage can be calculated by using voltage divider for the gate volage and the source voltage obtained by the product of $30mA$ and the source resistance. The resistors were chosen to maintain the $-0.1V$ gate source voltage and obtain the $30mA$ biasing condition. The $23.23GHz$ Colpitts oscillator feedback network was then designed using the procedure in Chapter 2 for the GaAs pseudomorphic High Electron Mobility Transistor (pHEMT) and shown in Figure 5.2. It is to be noted that the precise amplifier gain used in the oscillator design procedure was found by simulation. $23.23GHz$ was chosen as the CE3520K3 device operates up to $26GHz$, but has slightly lower noise figures going down from this maximum frequency.

Initially the microwave oscillator was directly connected to a multiplier without a buffer. However this meant that the multipliers needed extensive trial and error tuning because the reactive loading of the varactor affects the feedback network of the oscillator. In order to prevent the oscillator from shifting in frequency a buffer was designed as shown in Fig 5.3. This buffer, a source follower, provides a high input impedance and low output impedance and prevents the oscillator from being affected by the multiplier. Varactor multipliers with idlers can only be used with the presence of the buffer as they are sensitive to the input frequency. The buffer was loaded with a source resistance whose resistance was chosen by trial and error so as to maintain highest transfer gain (necessarily less than unity) while still reducing nonlinear components. To accentuate the oscillator frequency a tank circuit resonating at $23.23GHz$ was connected to the source.

5.3 THZ OSCILLATORS

The overall $185.9GHz$ was obtained by multiplying the $23.23GHz$ with three x2 frequency multiplier stages (see Figure 5.4). The multipliers used to generate the $185.9GHz$ had idlers. As a result of the narrowband idler design, the input and output circuits involved a single frequency with the benefit that it allows for fabrication of the lumped components by distributed or pattern type elements.

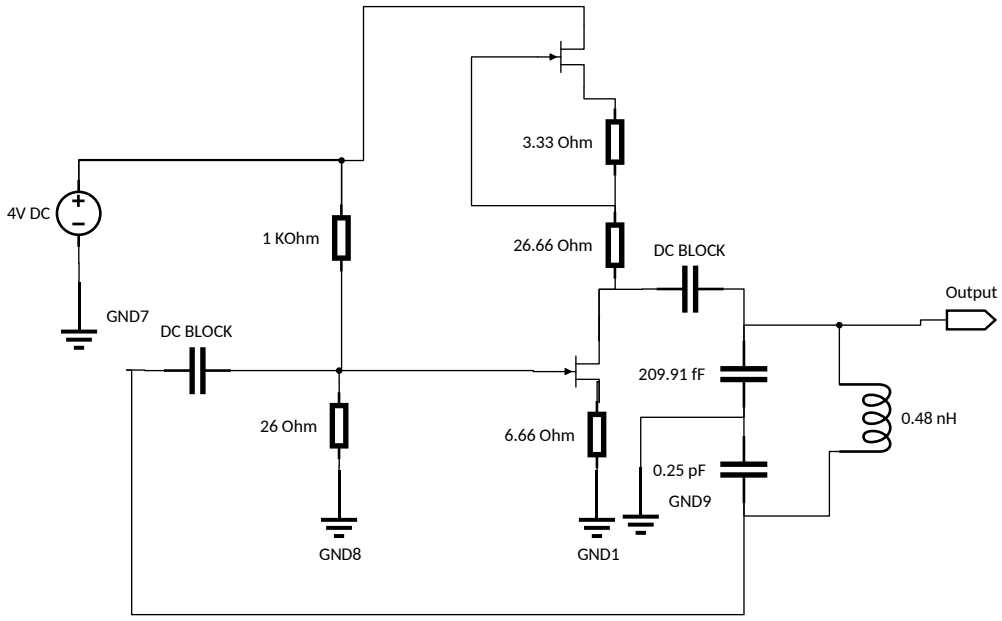


Figure 5.2: GaAs pHEMT Microwave Oscillator

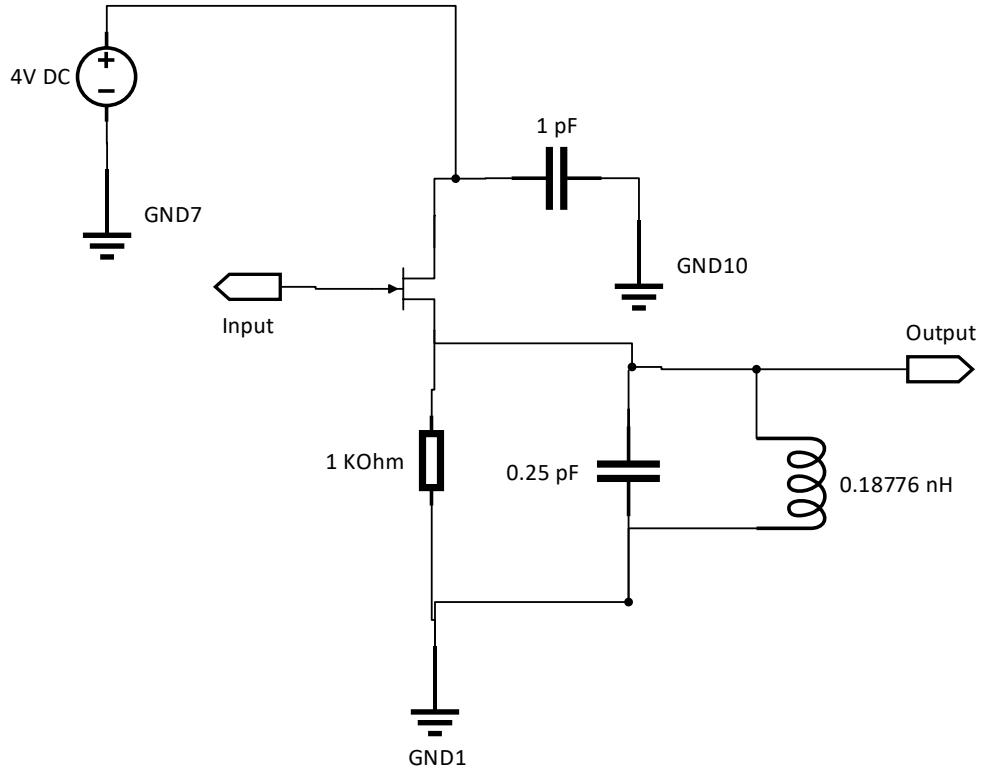


Figure 5.3: GaAs pHEMT High Impedance Buffer

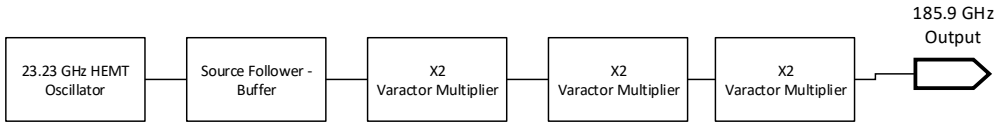


Figure 5.4: 185.9GHz Local Oscillator

5.4 FREQUENCY MULTIPLIERS

The MA4E1317 GaAs Schottky diode from M/A-COM was selected as it featured low junction capacitance and a low series resistance. As a result it was the diode used for all multipliers. Both multipliers with idlers and no idlers were designed to compare the performance. For the 185.9GHz oscillator used in the transceivers a summarized design procedure of the multiplier stages is given in Section 2.2 page 9.

5.5 GRAPHENE FIELD EFFECT TRANSISTOR DEVICE MODEL

For the GFET the compact model presented by Fregonese et al. in 2013 was used [11]. Verilog-A compatible equations from Fregonese et al. in 2013 were implemented for simulation (see Section 3.2 for the equations)[11]. The GFET was chosen to have a 73µm gate channel length and a 73µm gate width, for fabrication convenience. However, because the channel length is relatively large for a THz device the gate polyethylene dielectric was made sufficiently thick (1mm) to reduce the parasitic capacitance. An electron mobility of $7000\frac{cm^2}{Vs}$ was chosen since it was a typical value reported for high quality graphene[11]. Metal contact resistances are present at the drain and source, 50ohm and 0.3ohm, respectively. The metal contact resistances were typical values taken from literature[11]. Doping density was set to zero parts per million, since it deteriorates the carrier mobility for a reason akin to that of the MESFET discussed in Chapter 3.

5.6 AMPLIFIERS

5.6.1 *LNA*

LNA was designed with the GFET and had a noise figure of 0.284dB (see Figure 5.5). A current source loaded GFET was not mentioned in literature but it was a natural loading condition for attaining high gain. By finding the input (GFET gate) reflection coefficient using simulation at 209GHz the input capacitance could be computed and along with it the matching gate inductor for the LNA. The matching inductor was then slightly tuned by trial and error for some performance benefit. DC voltage biasing was chosen by ramping up in steps of 1V until the voltage gain no longer increased.

5.6.2 *PA*

A Class A amplifier was designed for the PA with attending high linearity and is shown in Figure 5.6. When using high order modulation linearity becomes a particularly important issue for a PA and hence regardless of the lower gain and power efficiency it was an appropriate choice. The PA topology was taken from Andersson et al[37] in 2012 and only the DC bias voltages was changed from default component values in the simulator. The DC bias voltages was obtained by trial and error and a step size of 0.2V.

5.6.3 *IF and Baseband Amplifiers*

The IF and baseband amplifiers can also be seen in Figures 5.7 and 5.8 and are also both Class A amplifiers. The former was essentially the amplifier used in the oscillator but with a higher drain resistance to maximize gain and no current source. The BJT baseband amplifier had significant gain and works in the Ultra High Frequency (UHF) band setting a baseband bandwidth limit of 6GHz. The 2SC3357 BJT had a typical gain value of 160. The biasing network was chosen such that the maximum forward gain can be used regardless of it's variability. The base bias current was chosen to be at 0.43mA. If the base current was increased more due to the high gain the transistor would be operating at or above the maximum power rating.

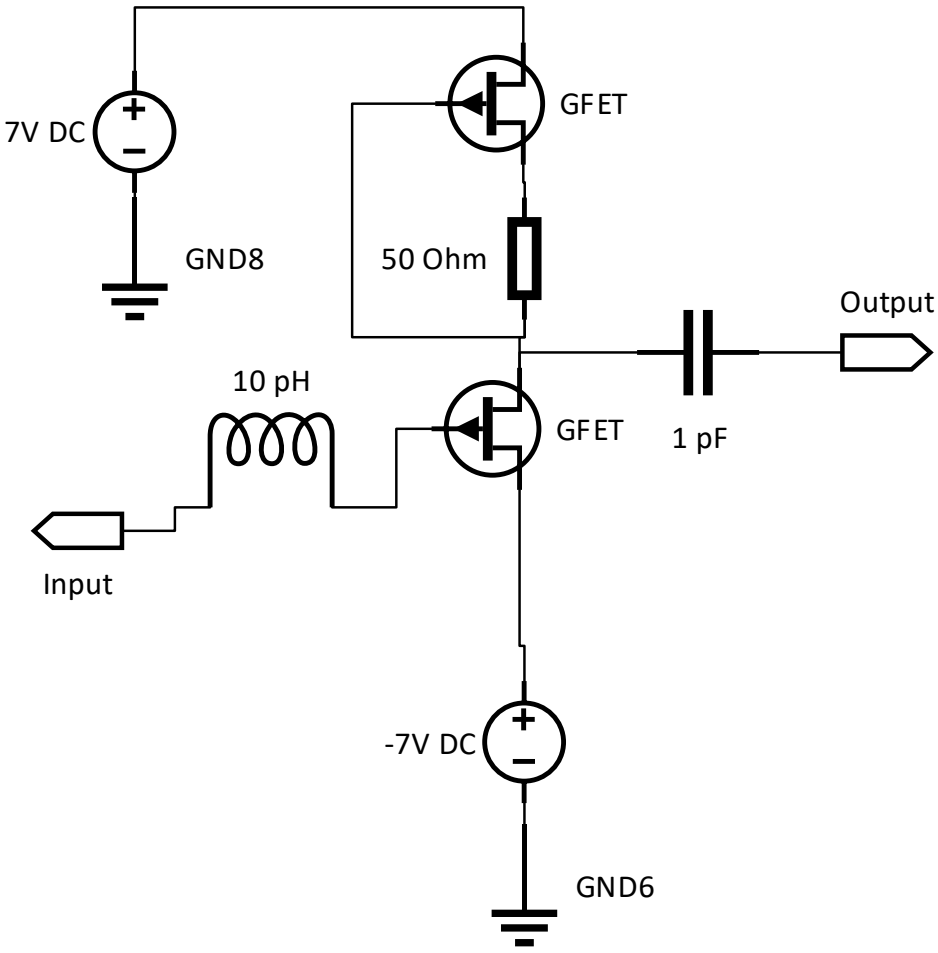


Figure 5.5: GFET Low Noise Amplifier

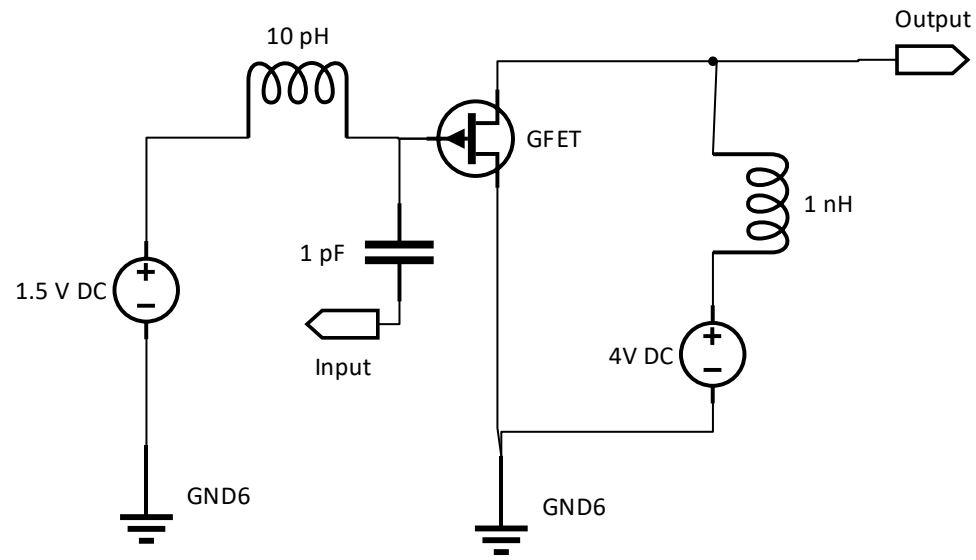


Figure 5.6: Class A GFET Power Amplifier

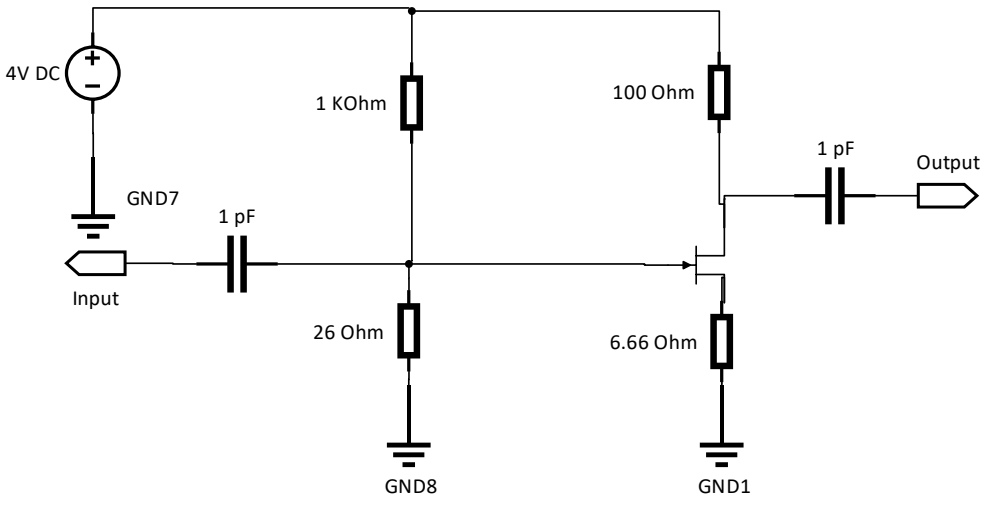


Figure 5.7: 23GHz IF Amplifier

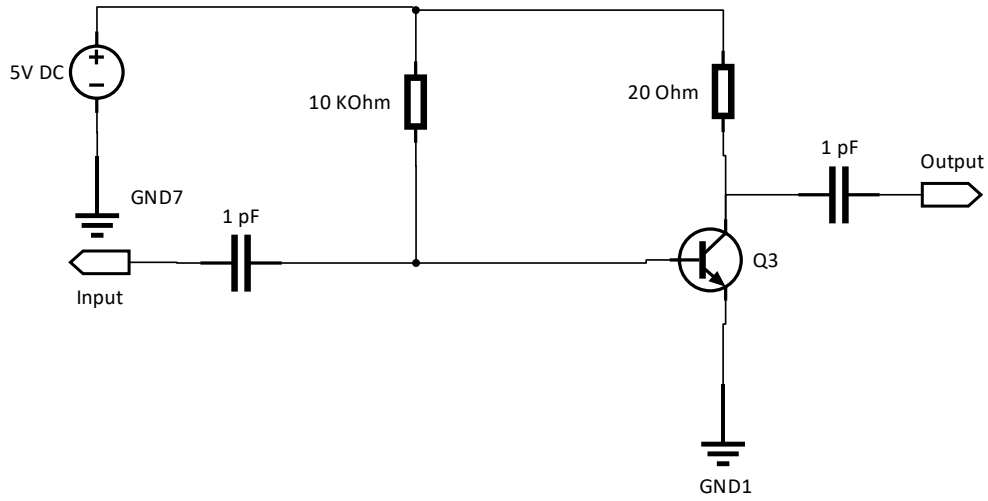


Figure 5.8: Baseband IF Amplifier

5.7 MIXERS

Two mixers were designed: a diode and an FET mixer. The diode mixer was selected for the microwave mixer as diode mixers have: low conversion loss, less component complexity and the oscillator power at that frequency is high enough to forward bias the diode. At THz the oscillator power produced was insufficient to forward bias a diode. However, FET mixers are capable of mixing with low oscillator powers. In the direct conversion architecture only the GFET fundamental mixer was used. For the double conversion architecture both the diode mixer and GFET fundamental mixer were employed. The Schottky diode mixer has 150dB LO to RF/IF rejection. The Schottky diode was based on a microwave diode with part number HSMS-286x and the modeled Simulation Program with Integrated Circuit Emphasis (SPICE) parameters were given in the datasheet. The diode mixer was matched at the output by the parallel combination of the 60hm diode resistance found in the datasheet and the capacitance was tuned for best conversion efficiency. However for the high LO rejection to be attained a 180 deg phase shift was employed to cancel the oscillator present at the output of the diode mixer. The diode mixer and GFET fundamental mixer can be seen in Figure 5.9 and 5.10, respectively. The x2 subharmonic mixer designed is also shown in Figure 5.11. The matching inductors for the GFET mixers were obtained by first calculating a gate capacitance reactance from the reflection coefficient and then using the complex conjugate to obtain the inductor impedance and hence inductance at 209GHz and further tuned. The fundamental GFET mixer had a drain bias at 1.5V to keep a positive voltage on the transistor since the input raised cosine signal had a maximum peak voltage of 1.5V. The gate biasing was chosen empirically by tuning and the 4nH inductor was also likewise found to decrease Conversion Loss (CL). The x2 subharmonic mixer was designed likewise to the fundamental GFET mixer. However since it was not

used in the transceivers the drain bias was tuned to reduce the CL for performance comparitive purposes.

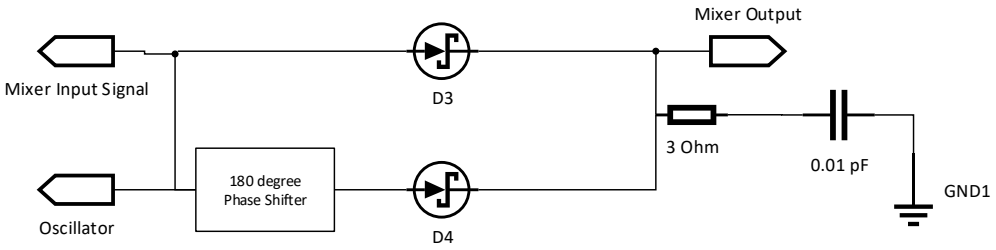


Figure 5.9: Schottky Diode Mixer

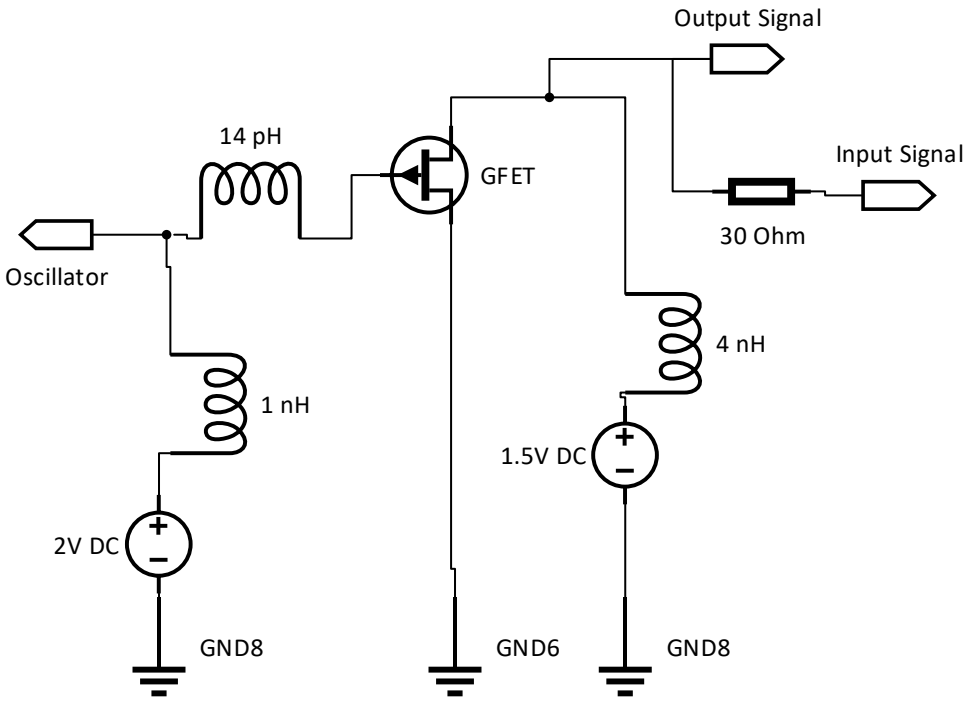


Figure 5.10: GFET Fundamental Mixer

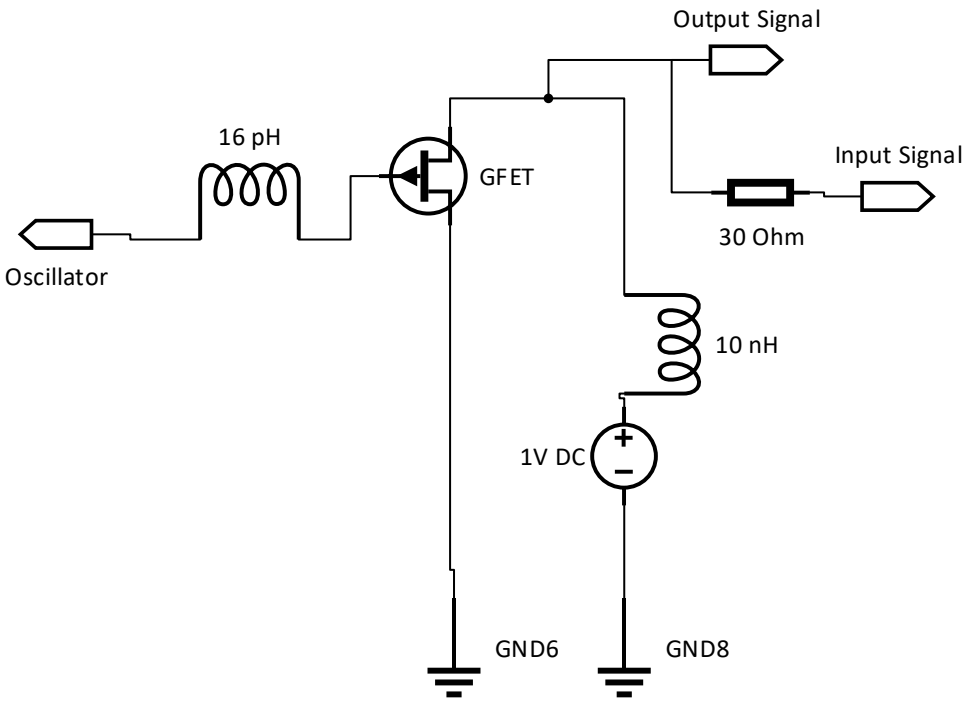


Figure 5.11: x2 Subharmonic GFET Mixer

5.8 MODULATOR

In order to put together the modulator the topologies in Chapter 4 were used as a template. The architectures were chosen for minimizing system size. Individual components in the generic architecture were replaced with those designed in a piecewise manner. By analysing the data output as each component was added decisions were made on the number of amplifier stages. Filters were also added as needed. As a result of high conversion loss a three stage PA was used in the double conversion architecture, (see Figure 5.1 (a)). The three stage PA also permits for communication at larger ranges. The 23GHZ IF amplifier introduced not only added gain to the diode mixer output but also made the lower and upper side-bands to have more level power. Similarly in the Zero-IF a three stage PA was used (see Figure 5.12).

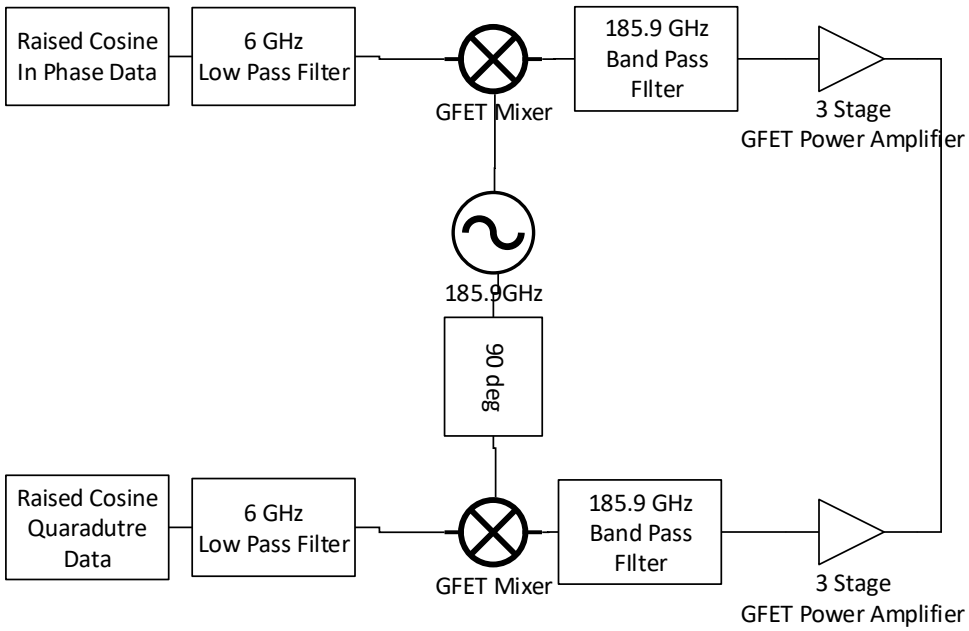


Figure 5.12: Single Conversion IQ Modulator

5.9 DEMODULATOR

The demodulator for the Zero-IF architecture and double conversion architecture is shown in Figures 5.13 and 5.1(b), respectively. An LNA was used in the double conversion to boost low received power however in the Zero-IF it was omitted because there was no improvement in the overall system performance. Like the modulator, the demodulator was built in a piecewise fashion, simulating as each designed component added. A three stage BJT was used for both architectures as the magnitude of the mixer output is low.

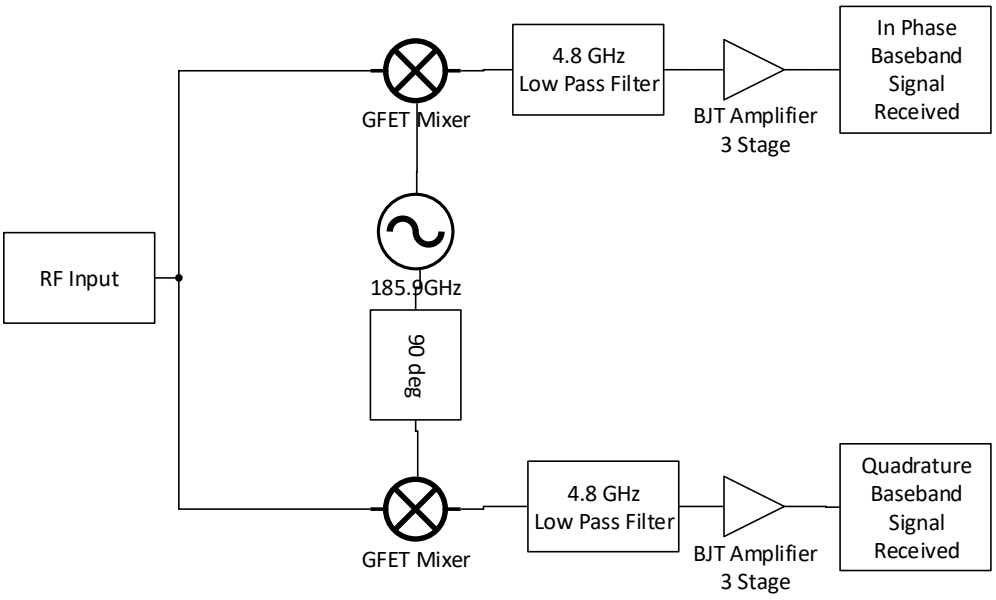


Figure 5.13: Single Conversion IQ Demodulator

5.10 TRANSCEIVERS

Since bandwidth is a scarce resource Raised Cosine pulse shaping was used to limit the signal bandwidth and also reduce Inter-Symbol Interference (ISI). The baud rate of all the transceivers is 5Gbps because performance was found to be best at this rate. Regardless of Transmitter (TX)/Receiver (RX) system the received baseband bandwidth is filtered to 4.8GHz. The digital signal processing such as the equally probable random data source, symbol (de-) mapper, conversion between complex and rectangular representations, error control coding, BER computation and Error Vector Magnitude (EVM) computation was performed conveniently using the ADS Ptolemy library implementations. Due to the complexity of the 185.9GHz source and long simulation time for Ptolemy real time simulation, the oscillators were characterized and replaced with built-in components. Phase noise was omitted for the 23GHz since no phase information is stored in the first upconversion stage of the transmitter. The 185.9GHz oscillator was characterized with the power and phase noise obtained when connected to the gate of the fundamental GFET mixer and replaced with a built-in oscillator with phase noise block. Error coding and correction employed included Trellis convolutional coding, Reed Solomon block coding, Turbo coding and Viterbi decoding.

6 RESULTS AND DISCUSSION

In this chapter, the performance of the components designed will be reported and benchmarked with published designs. The chapter begins with the oscillators and concludes with the overall transceiver metrics. Any model assumptions made will be included with in each subsection.

6.1 THZ OSCILLATORS

The THz oscillators which were designed as part of this research are discussed and compared in this section with that published in literature. As outlined in Section 2.1 the important type of noise degradation for an oscillator is phase noise. The source of phase noise was also defined in Section 2.1. For the purpose of this section salient points of phase noise will be reviewed. Phase noise manifests itself as a spread of frequencies around the desired carrier. The spread is due to the shifting carrier frequency angle. A phase noise plot indicates the magnitude of these frequencies[27]. Spectrum analyzers are capable of measuring and showing the phase noise by displaying the spectrum averaged over a time interval[27]. ADS alteratively was used as a replacement for the spectrum analyzer as it can mimick the process. To assess the performance of the designed oscillators phase noise and output power plots are shown in Figure 6.1 and 6.2. The performance of the oscillators was also evaulated with MATLAB by plotting a BPSK constellation plot with their respective phase noise data. From these constellation plots a phase noise level of less than -90dBc/Hz was observed to be best. The phase noises of some oscillators was unnacceptable as the delineation between the bit values 1 and 0 was not present or in other words a complete circle was formed of data points on the BPSK constellation plot. The multiple stage THz oscillators generally show as expected decreasing power and increasing phase noise and are shown in Figure 6.1. However, as can be seen in Figure 6.1(b) the 101GHz oscillator had lower performance than the 185.9GHz oscillator. This demonstrates that design plays an important role in obtaining suitable performance. One of the design factors for the 101GHz oscillator's lower performance was the use of a 25.29GHz microwave frequency in comparison to the 23.23GHz of the 185.9GHz oscillator. For the lower noise figure 23.23GHz was chosen. The 185.9GHz shown in Figure 5.4 had a lower phase noise of -128dBc/Hz when connected to the GFET mixer. In comparison the phase noise was -101dBc/Hz when free standing (see Figure 6.3). This lower phase noise of -128dBc/Hz was the result of good impedance matching. For the transceivers the -128dBc/Hz phase noise data was used for the specification of the built-in oscillator component. This is because it is the phase noise at which the GFET mixer (with local oscillator at gate) is operating. Since the phase noise of the built-in component does not shift, it was set to reflect the performance as seen by the mixer. Unlike the multiple stage oscillators the single stage THz oscillators shown in Figure 6.2

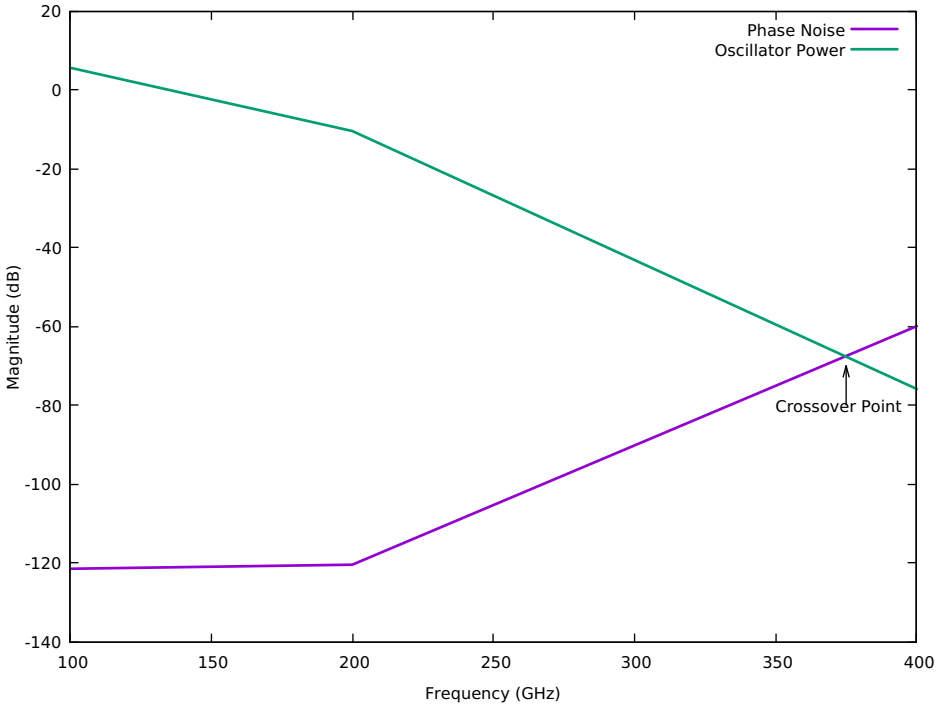
Table 6.1: THz Oscillators

Author	Frequency	Power	Phase noise
Chen et al. (2015)	172-196GHz	12.5dBm	Unavailable
Waliwander et al. (2016)	180 - 200GHz	19dBm	Unavailable
Kalfass et al. (2017)	240GHz	Unavailable	−110dBc/Hz
Dan et al. (2020)	300GHz	Unavailable	−90dBc/Hz
This Work	185.9GHz	3.255dBm	−128.3dBc/Hz
This Work	185.9GHz	1.434dBm	−112dBc/Hz
This Work	200GHz	19.54dBm	−120.5dBc/Hz
This Work	371.7GHz	−30dBm	−94.214dBc/Hz

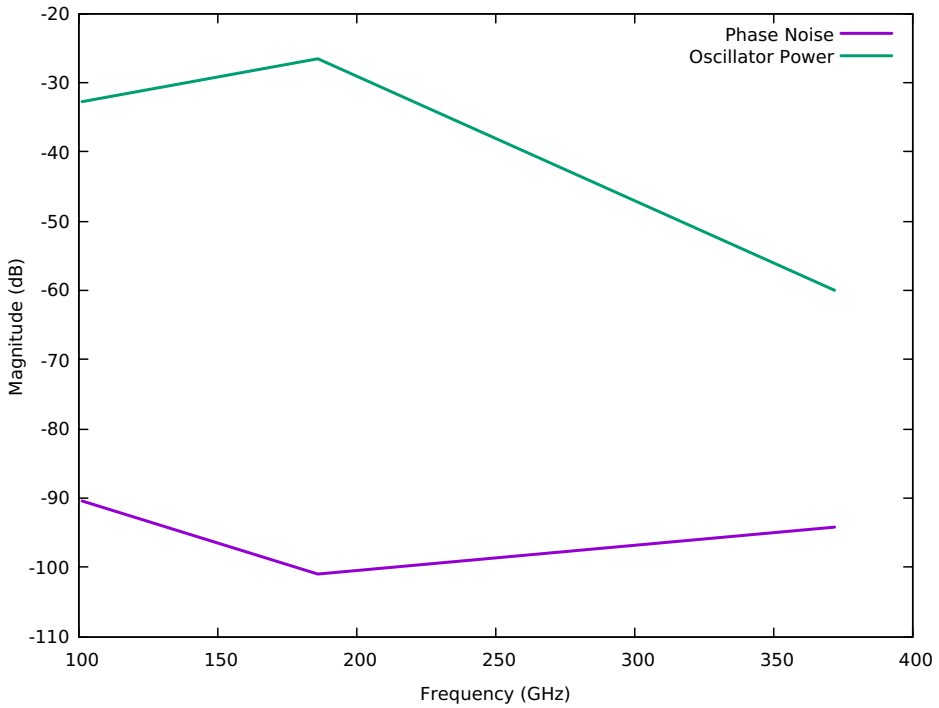
had high power and high noise, simultaneously. The high phase noise of the single stage THz oscillators was found to be due to the Butterworth filter used to select the desired frequency. When the Butterworth filter was removed and the phase noise plotted at the output of the multiplier the phase noise level was much reduced. However the output of the single stage multiplier as is, was not of use because there were several strong THz frequency components. The performance difference as a result of the Butterworth filter can be attributed to the reflected frequencies in the stop band of the filter returning to the diode and re-exciting it to produce harmonics and add to the overall phase noise.

Table 6.1 shows a comparision of the multiple stage THz oscillators obtained in this work and in literature. The values are listed in dBm rather than the dB in the figures. The 185.9GHz oscillators obtained by the SBD and the x2 subharmonic GFET are listed in this order respectively.

Chen et al. in 2015 had reported a high power 172-196GHz source with 12.5dBm power[36]. They produced the oscillator by a combination of active and passive multiplication[36]. The 185.9GHz oscillator shown in Figure 5.4 had an output power of 3.255dBm. The first two multiplier stage had generated a 92.93GHz oscillator with 0.28V amplitude; however, the last multiplication stage incurred the highest conversion loss reducing the output voltage to 47mV. This reduction is expected as the quality factor of the diode decreases with increasing frequency[29]. The x2 subharmonic GFET mixer design shown in Figure 5.11 and the corresponding frequency multiplication that occured generated a 1.434dBm 185.9GHz signal. The x2 subharmonic mixers outputs less power than that with the Schottky multiplier. Higher powers are usually attained using active multipliers. However, this was not the case with the GFET x2 subharmonic mixer. The primary load of an oscillator is a mixer and FET mixers can operate well with lower oscillator output powers thus diminishing the effect of a few decibels on system performance. Figure 6.8 shows that the x2 subharmonic GFET mixer with the designed oscillator had a CL performance of 38dB close to that of the lowest CL of 34dB reported



(a)



(b)

Figure 6.1: Multiple Stage THz LO Phase Noise and Power Plot a) Without Idlers b) With Idlers

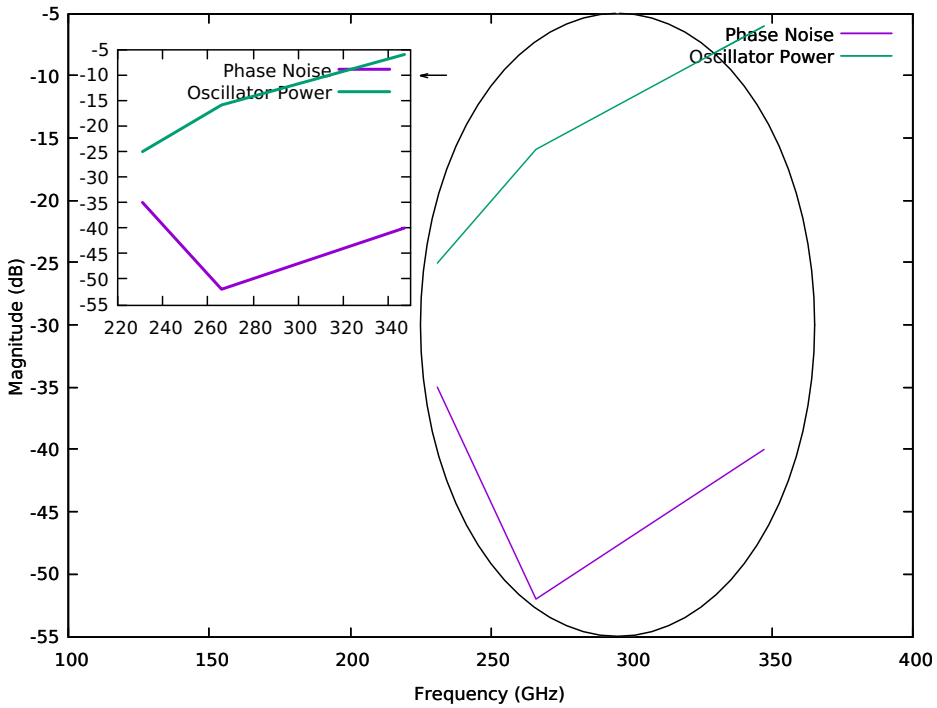


Figure 6.2: Single Stage THz LO Phase Noise and Power Plot

with GFET mixers to-date at 190GHz. Waliwander et al. in 2016 achieved an 180 - 200GHz Schottky multiplication with LO output power of 19dBm verified by simulation[40] and was comparable to the 19.54dBm 200GHz oscillator designed in this work without idlers. This shows that in this frequency range of around 200GHz adequate and high power oscillators are readily possible with Schottky varactors. By allowing for no idler in the multiplication stages for the 200GHz oscillator the power level was higher. Nonetheless this comes at the expense of implementing the broadband inductors and capacitors which can be difficult at THz frequencies.

Figure 6.1(a) has a crossover point for phase noise and power. Beyond this crossover point communication would be difficult with phase modulation. Figure 6.1(b) shows the performance of a 371.7GHz oscillator obtained by an additional multiplication by two stage of the 185.9GHz as shown in Figure 5.4. The performance of the 371.7GHz which is 3.3GHz away from the crossover point has satisfactory phase noise for BPSK but could not be used for phase modulation of higher order. This can be demonstrated by a constellation plot. Nonetheless the -30dBm output power at 371.7GHz source is too low for a mixer to operate well thus eliminating also the BPSK option. However, Liu et al. in 2017 have reported a 10.8dBm source at 360GHz using multiple diodes for each x2 stage[18]. The oscillator reported by Liu et al. in 2017 however can be expected to increase the phase noise . The equivalent series resistance of the four diodes employed by Liu et al. in 2017 per multiplier stage will increase the thermal noise power and hence phase noise. Considering that the quality factor of a circuit limits the bandwidth. The higher the center frequency the more bandwidth achievable for the same percent bandwidth as a

result of quality factor. However this frequency scaling scheme becomes less than ideal to use beyond 375GHz both in terms of power and phase noise. Design and device improvements may allow for better noise and power specifications. It is unlikely to extend further than 400GHz because an ideal multiplier of order N increases phase noise by $20 \log N$. For good performance a low phase noise of less than -90dBc/Hz is preferred. Dan et al. in 2020 used a 300GHz oscillator with -90dBc/Hz for THz communication, whereas Kalfass et al. in 2017 used a 240GHz oscillator generated by x2 Subharmonic mixing of 120GHz[22][39]. Kalfass et al in 2017 attained -110dBc/Hz at at 100KHz offset which is 2dBc higher than that of the 185GHz oscillator generated by the x2 GFET Subharmonic mixer in this work as shown in Figure 5.11[39]. It is clear that the phase noise is higher for active device multipliers but at -112dBc/Hz good transceiver performance can be attained. The high phase noise single stage THz oscillators could find use in only amplitude modulation schemes and may be sufficient for particular applications. The multiple stage THz sources are suitable for high spectrally efficient modulation schemes but is limited in frequency range. The 185GHZ oscillator phase noise can be seen in Figure 6.3.

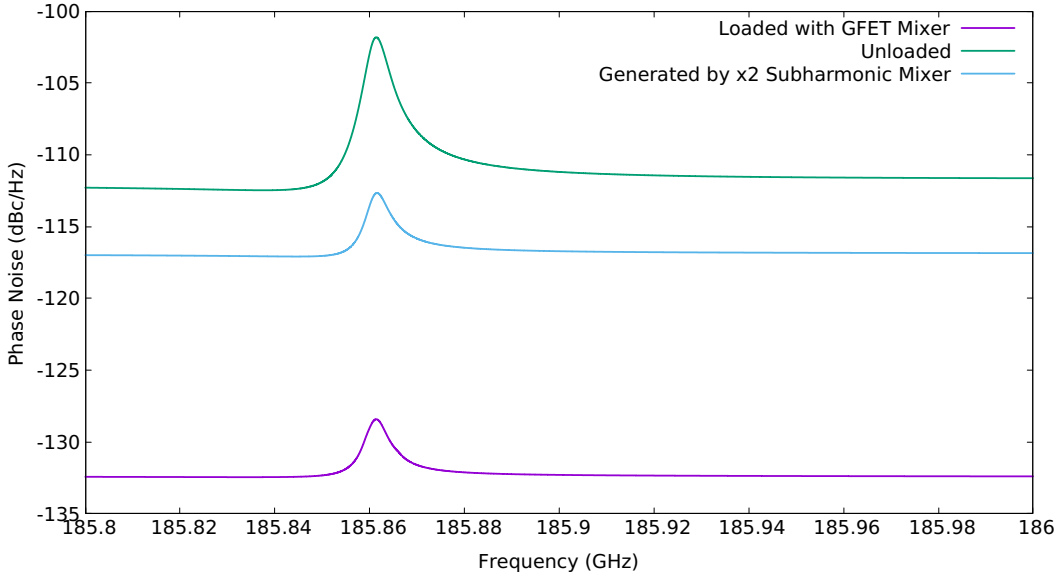


Figure 6.3: Local Oscillator with Mixer Performance

6.2 GRAPHENE FIELD EFFECT TRANSISTOR MODEL VERIFICATION

To verify the implemented Verilog-A GFET model was correct to the model equations published: the length, width, electron mobility and gate capacitance of the GFET was set according to that of the GFET in Rodriguez et al in 2014[26] and listed in Table 6.2. Following this the transistor was simulated for drain current against drain source voltage. The output characteristic can be seen in Figure 6.4 compared with measured data of Rodriguez et al. in 2014[26]. The C_{gs} and C_{ds} capacitances can be seen in Figure 6.5 and Figure 6.6, respectively.The three intrinsic parameters characterising the GFET device design comprises the current voltage characteristics and the parasitic capacitances (C_{gs} and C_{ds}). It can be seen from these plots that the GFET device model shows the same characteristic values with that in Rodriguez et al. in 2014 and can be concluded that it is operating according to the model. Rodriguez et al. in 2014 had also provided a simplified model for analog design; however, the values used in this comparison is the data points evaluated with the Fregonese model and reported by Rodriguez et al. in 2014. Fregonese et al. in 2013 did not have plots for C_{gs} and C_{ds} hence the values plotted by Rodriguez et al in 2014 using the Fregonese model were employed[26][11]. It is also to be noted that the model by Rodriguez et al. in 2014 cannot predict accurately the current voltage characteristic for negative gate source voltage neither the biasing dependant C_{gs} and C_{ds}. The x2 GFET subharmonic mixer in Figure 5.11 had both positive and negative gate source voltage as a result of the oscillator and the model by Rodriguez et al. in 2014 was insufficient for simulation[26].

Table 6.2: GFET Parameters Used for Verification

Parameter	Value
Channel Length	$440nm$
Channel Width	$1\mu m$
Carrier Mobility	$7000\frac{cm^2}{Vs}$
Gate Capacitance	$3.6mF/m^2$
Doping density	$0ppm$

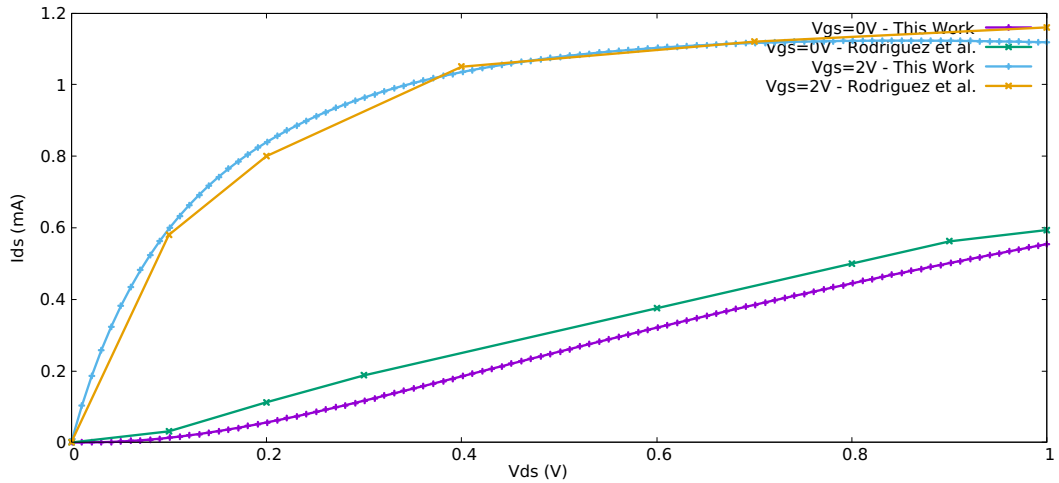
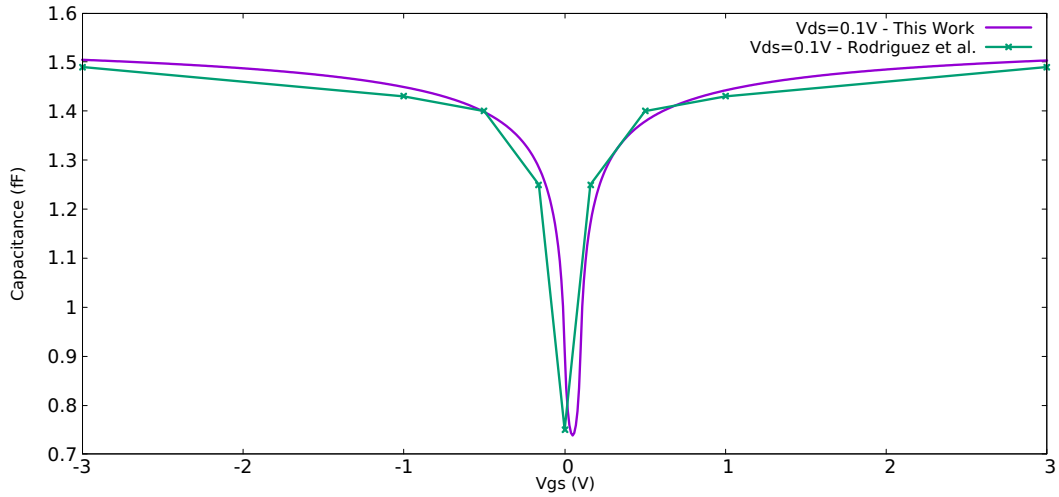
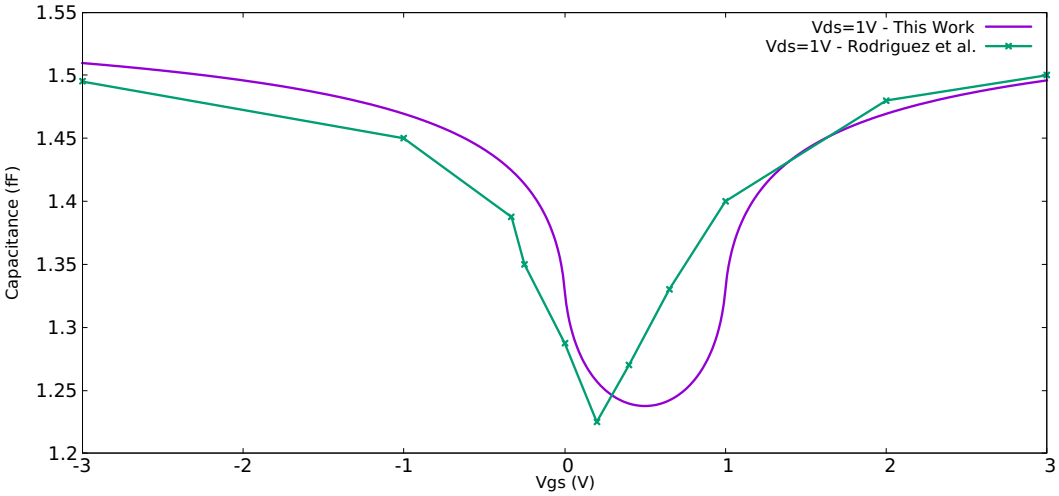


Figure 6.4: 440nm GFET Output Characteristics



(a)



(b)

Figure 6.5: 440nm GFET Gate Source Capacitance a) Vds of 0.1V b) Vds of 1V

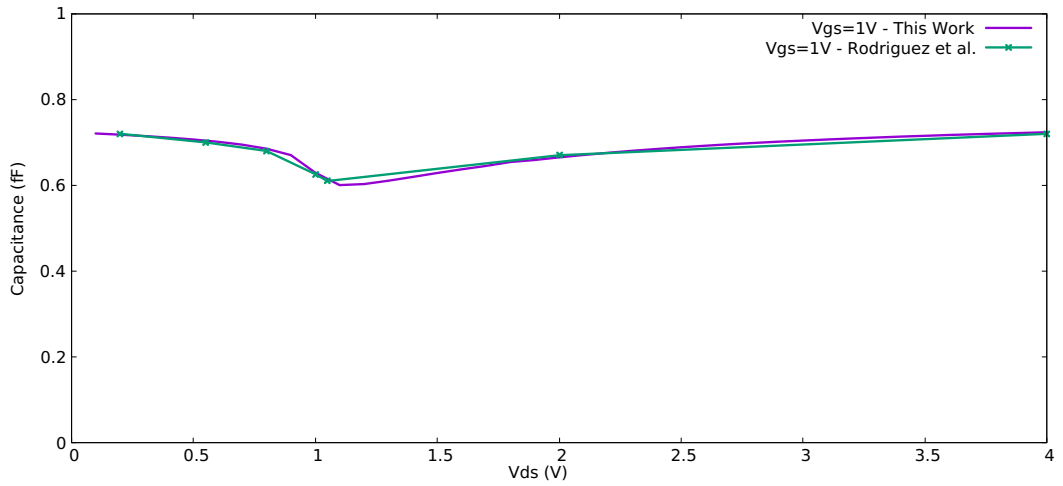


Figure 6.6: 440nm GFET Gate Drain Capacitance

6.3 AMPLIFIERS

The single stage PA and LNA shown in Figures 5.6 and 5.5 had transducer voltage gains of 6dB and 9.24dB, respectively as shown in Table 6.3. The LNA had a minimum noise figure of 0.284dB. The power amplifier was based on the topology of Andersson et al. in 2012 which had reported 10dB gain at 1GHz. In this work 6dB gain was attained at 200GHz[37]. Andersson et al. in 2012 reported the transistor had an electron mobility of $2000\frac{cm^2}{Vs}$ while in this work $7000\frac{cm^2}{Vs}$ was used[37]. In graphene terms both are lower than the theoretically possible $100,000\frac{cm^2}{Vs}$[41]. The LNA had higher gain than the PA and was a common source current source loaded topology frequently found in MOS circuits[5]. Since no GFET amplifiers were found in literature operating at 200GHz, comparison was limited. Nevertheless GFETs are being investigated at mmWave frequencies and are promising as large area devices[41].

Table 6.3: GFET Amplifiers

Author	Frequency	Gain	Amplifier Type
Andersson et al. (2012)	1GHz	10dB	PA
This work	200GHz	6dB	PA
This work	200GHz	9.24dB	LNA

6.4 MIXER

When comparing mixers as shown in Table 6.4 the CL is a significant metric. The lower the CL the better. For a given higher CL more amplification is necessary to make up for the CL. More amplifier stages results in a circuit that is more bulky and less capable in the presence of noise. Zhang et al. 2016 reported the lowest published figure so far using GFET mixers in the 190-210GHz frequency range[38]. As discussed in Section 2.3 on mixers, the third order nonlinearity plays an important role in describing mixer non-idealities. 1dB gain compression point is one figure of merit where the higher it is the better. It represents a varying CL with power level resulting in distortion. Likewise, with the IP3 the higher it is the better. IP3 represents a theoretical point beyond which the mixer is useless since the third order power surpasses the fundamental. Another important design parameter is LO to RF rejection which represents the magnitude of the oscillator leaking into the output spectrum. With a Zero-IF transceiver architecture low LO to RF rejection can significantly hinder proper operation.

Table 6.4: GFET Mixers

Author	Frequency	Conversion Loss	Oscillator Power
Zhang et al. (2016)	190-210GHz	34dB	10dBm
Vazquez et al. (2015)	220-330GHz	65dB	Unavailable
This work	185.9-216GHz	50dB	3.255dBm
This work	182.9-188.9GHz	38dB	10dBm

The Schottky diode mixer shown in Figure 5.9 had a 150dB LO to RF rejection and a CL of 21dB at 23.23GHz. The most important figure was the LO rejection figure for the double conversion architecture. The GFET mixer operated as a x2 subharmonic mixer and had a CL of 38dB at 92.93GHz LO power of 10dBm. This high LO power at 92.93GHz is readily available and was exceeded in the multiplier stage prior to the final 185.9GHz output stage at 18.94dBm. The CL of the x2 subharmonic mixer shown in Figure 5.11 was also much less than that of the 50dB CL of the fundamental GFET mixer used in the transceivers implemented in this work. Nonetheless there was still a strong 185GHz frequency component and thus the x2 subharmonic mixer cannot be used straight in a Zero-IF architecture. In addition the x2 subharmonic GFET mixer had much higher phase noise than the phase noise of the fundamental mixer. This demonstrates a trade off in power and phase noise (see Figure 6.3 for the phase noise plot). The gain compression plot of the fundamental GFET mixer can be seen in Figures 6.7 with a 1dB compression point at −6dBm input power. The IP3 was also plotted and can be extrapolated to 10dBm (see Figure 6.9). These figures are satisfactory as the spectral components of the raised cosine baseband signal over the 5GHz bandwidth does not exceed 1.93dBm. Generally the spectral components were over −10dBm for gain compression dis-

tortion to be minimal. The fundamental power of the x2 subharmonic mixer was plotted for verification with that of Zhang et al in 2016 (see Figure 6.8)[38]. Zhang et al. in 2016 had reported 34dB conversion loss with a 95-105GHz local oscillator at 10dBm power[38]. The GFET dimensions used by Zhang et al. were a double channel setup with 2x40µm gate width and 0.5µm gate length. In this work 73µm gate width and length was used and obtained comparable results with Zhang et el. in 2016[38]. The phase noise as plotted in Figure 6.3 counters the benefit of the higher output power with the x2 subharmonic GFET mixer. The fundamental GFET mixer however still attained a lower CL than that of Vazquez et al. in 2015 where 65dB CL was reported at 220 - 330GHz[42].

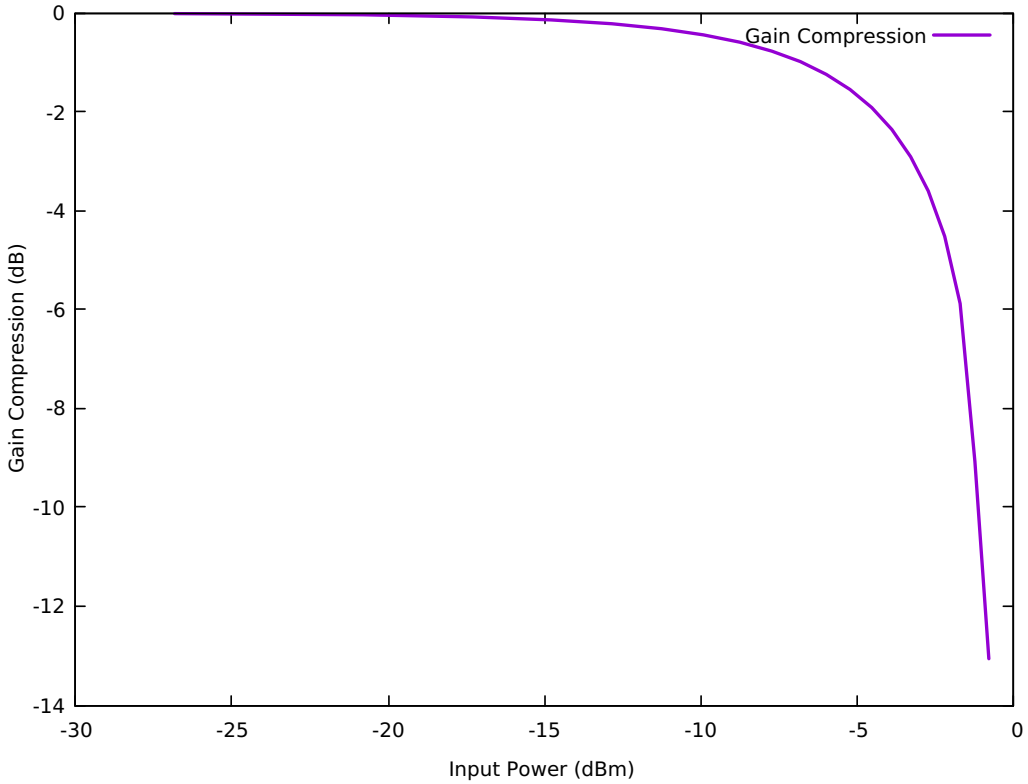


Figure 6.7: Fundamental GFET mixer Gain Compression

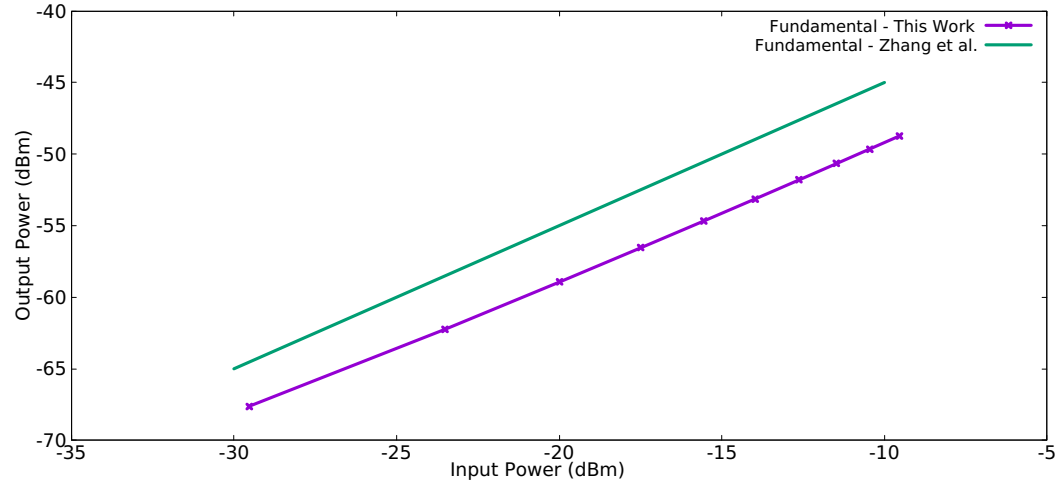


Figure 6.8: x2 GFET subharmonic mixer Fundamental Power

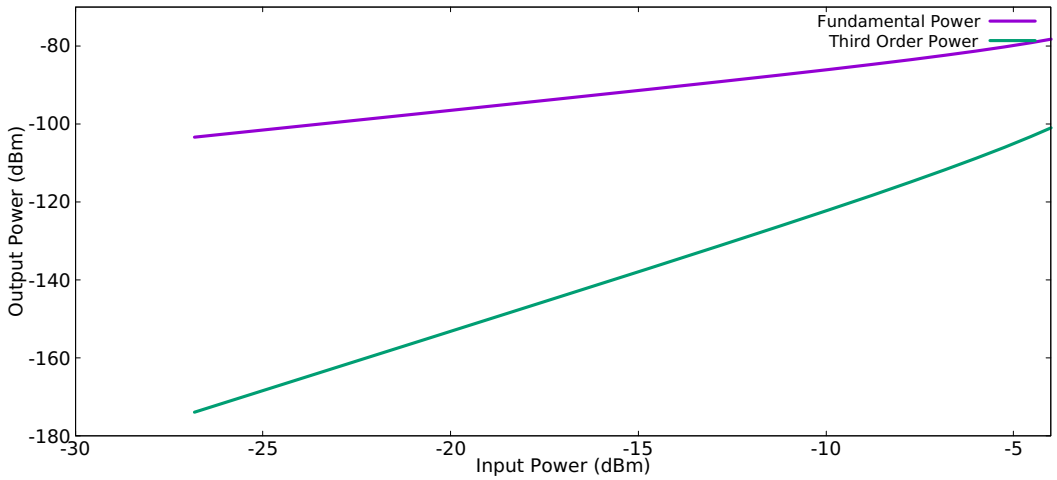


Figure 6.9: IP3 of Fundamental GFET mixer

6.5 NOISE PERFORMANCE

The performance of the components comprising the transceiver have been examined and shown to be state of the art. To assess the complete transceiver, it is also appropriate to show the systems ability to communicate bits. In the following two subsections the BER and EVM figures will be discussed.

6.5.1 *Bit Error Rate*

The BER is an immediate quantity affecting communication quality. Several error coding schemes are possible; however, it was found that a combination of Turbo and trellis convolutional coding had best performance and the Reed Solomon coding initially used was supplanted. For the double conversion BPSK system minimum BER is 0.0 with a combination of Turbo coding (code rate $\frac{1}{2}$) and a trellis convolutional coding (code rate $\frac{1}{2}$). Using only Turbo coding the BPSK BER is 0.03. These figures show that with only half the full throughput of 5Gbps BPSK uncompressed digital speech (64Kbps) can be communicated supporting 39062 conversations. While for 16QAM with the same error coding as the BPSK a minimum BER of 0.0 is achieved with combination of Turbo and trellis coding and $9 * 10^{-3}$ with only Turbo coding. Error control coding was used to reduce these quantaties substantially and was necessary as the transceivers caused distortion. The capacity at 16QAM was a high 20Gbps and showed error free high throughput data communication was possible with a code rate of $\frac{1}{4}$.

6.5.2 *Error Vector Magnitude*

The EVM demostrates the spread about the ideal constellation point and indicates how much noise is present in the system. The EVM obtained for the separate modulation schemes is presented here. A theortically ideal value of EVM is 0.0%. The Zero-IF architecture was modeled with built-in components and had a DC offset problem. The 8PSK modulated system was unusable due to the DC offset. Nonetheless the Zero-IF with 8PSK can be seen to reach a lower 19.7% at the absence of the LO leak or DC offset. Therefore, the Zero-IF transceiver is not useful for communication without better cancellation of the LO leakage in the GFET mixer. For double conversion: 5Gbps BPSK had an EVM of 40.9%, 10Gbps QPSK had an EVM of 49.1%, 15Gbps 8PSK had an EVM of 12.9%, 20Gbps 16QAM had an EVM of 28.7% and 30Gbps 64QAM for double conversion had an EVM of 13.1%. The double conversion architecture achieved it's best performance with a combination of amplitude and phase modulation.

6.6 TRANSCEIVERS

The designed transmitter had a good IQ power balance as both in phase and quadrature had the same RF voltage to three significant digits. This comparison was made using the same baseband source power. The IQ power balance is important for high order modulation such as QAM where the precise amplitudes define a constellation point. The transmitter had a 79 degree phase shift between the IQ components in the RF spectrum when fed with the same baseband input source. In an ideal transmitter 90 degree phase shift is expected however, practically values near this are satifactory. The THz oscillator is loaded with two loads in a IQ modulator therefore the output power reduces thus increasing the mixer conversion loss. A higher oscillator power of $6-10\text{dBm}$ could improve the performance of the mixer substantially.

At the receiver the LNA was loaded with a low mixer impedance for noise purposes and only 6dB gain was achieved for low received powers. The GFET fundamental mixer achieved the lowest CL of 32dB in the receiver. This was most likely due to low gain compression and the CL is comparable to that of the Zhang et al[38]. However, due to the low power a three stage BJT baseband amplifier was necessary to increase the received signal to greater than 1V.

To compare the performance of the THz transceiver in this work with a microwave implementation, the designed components were setup with the LO frequencies of the 23GHz transmitter of Rahayu et al in 2003[43]. The 23GHz transmitter power obtained with the transciever in this work can be seen in Figure 6.10. The RF power obtained by Rahayu et al. in 2003[43] was 25.4dBm while 8.395dBm was obtained in this work. The label Maximum Spurious in Figure 6.10 is for the maximum spurious mixer product generated and was -94.661dBm while Rahayu et al. in 2003 obtained -98dBm[43]. In this work it should be noted that while a three stage PA was employed in the THz transmitters but only a two stage PA was used in this simulation comparison.

Table 6.5: THz Transceivers

Author	Frequency	Modulation	EVM
Boes et al. (2014)	240GHz	8PSK	21.6%
Dan et al. (2020)	300GHz	16QAM	15.2%
This work	209GHz	BPSK	40.9%
This work	209GHz	16QAM	28.7%

The THz transceivers were compared to those of Boes et al. in 2014 and Dan et al. in 2020 as can be seen Table 6.5[21][22]. Both Boes et al. in 2014 and Dan et al. in 2020 used 35nm InGaAs metamorphic High Electron Mobility Transistor (mHEMT)

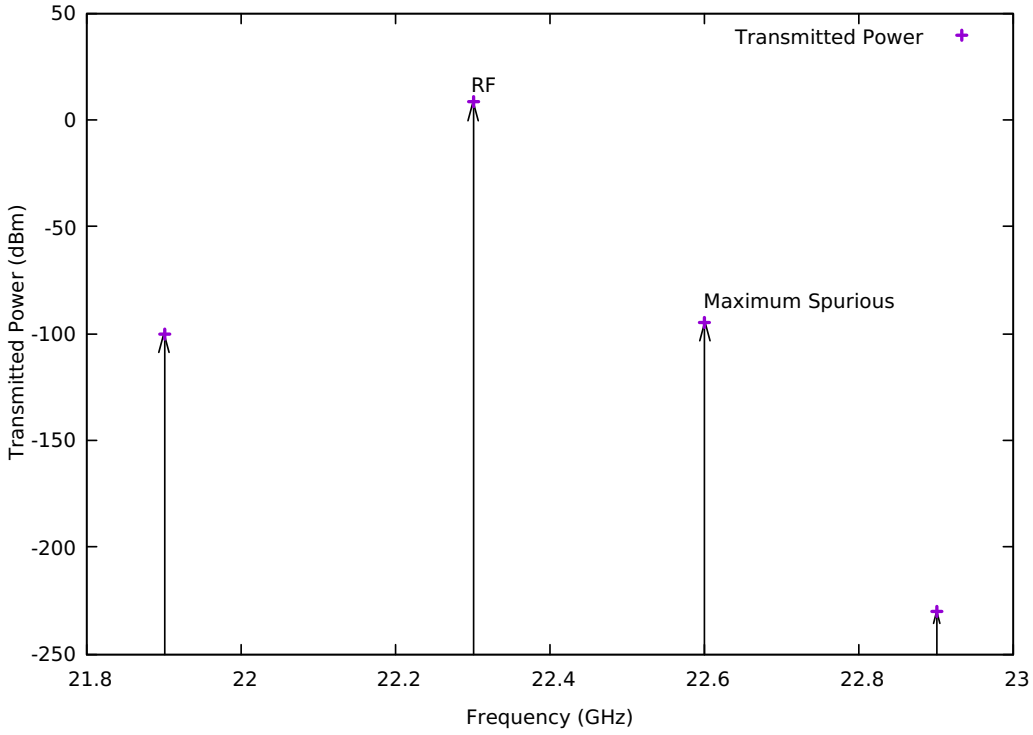


Figure 6.10: 23GHz Transmitter Performance

Table 6.6: THz Transmit Power

Author	Frequency	Bandwidth	Total Power
Kalfass et al. (2017)	240GHz	64GHz	−4.5dBm
This work	209GHz	10GHz	−24.676dBm

device technology. For the 240GHz Zero-IF transceiver by Boes et al. in 2014 a EVM of 21.6% was reported using 8PSK. In this work, 19.7% was obtained with Zero-IF under the condition of high local oscillator IF/RF rejection. However, when accounting for the actually obtained rejection the DC offset made the output bits to be biased to one symbol or symbol group. Thus the Zero-IF with the fundamental mixer could not perform well without better oscillator cancellation. In addition the x2 subharmonic GFET mixer also had a strong 185.9GHz signal. Therefore to obtain what Boes et al. in 2014 found using a x2 subharmonic mixer, LO cancellation is necessary for the GFET mixer design. This can simply be accomplished with a bandreject filter at that specific frequency. Nevertheless since x2 subharmonic GFET increases the phase noise the overall benefit is reduced. With double conversion the EVM is lower than that of Boes et al. in 2014 at 12.9%. Dan et al. in 2020 compared both 300GHz Zero-IF and double conversion architectures. A DC offset on the Zero-IF transceiver was reported and that the double conversion superheterodyne had superior performance[22]. Dan et al. also reported 15.2% EVM on 16QAM whilst 28.7% was obtained in this work. In addition BPSK with double conversion architecture attained a 40.9% EVM. Although this is high, error correction makes the scheme very usable at high redundancies. The transmitted signal power reported by Kalfass et al. in 2017 had $-4.5\mathrm{dBm}$ with RF bandwidth of 64GHz while 10GHz RF bandwidth was employed in this work and the transmitted signal signal power was $-31.386\mathrm{dBm}$ for 16QAM and $-24.676\mathrm{dBm}$ for BPSK[39]. Kalfass et al. achieved 850m coverage at 240GHz. To normalize the transmit power for comparison the transmit power per GHz bandwidth is $-0.07\mathrm{dBm/GHz}$. While in this work it is $-2.4676\mathrm{dBm/GHz}$ for BPSK[39]. Thus the transceivers designed in this work can certainly be expected to operate at 10-20m range for wireless Local Area Network (LAN) and femtocells. Overall the range can be extended by adding PA stages nonetheless at the cost of circuit size. The 16QAM and 64QAM transceivers can support high speed communication at very low error rate with substantial error coding redundancy and still provide high throughput. The highest reported all electronic transeceiver throughput was by Hamada et al in 2019 using InP transistors[44]. A bit rate of 120Gb/s was achieved at 300GHz with a 30GHz bandwidth and a range at 9.8m[44]. Considering the large bandwidths used such systems are not economical in terms of spectrum allocation and commercially could pose a problem. In addition InP is an expensive substrate[32].

7

CONCLUSION

THz communication viability is only possible with affordable THz sources of satisfactory performance. Observing the current state of art much was unanswered and hence the term THz gap was not only in frequency but indeed there was a gap in knowledge to be filled especially considering the unique benefits of THz frequencies.

In the area of communication THz frequencies could provide for superior performance in wireless communication but also for Radio Detection and Ranging (RADAR) imaging. With this high expectation comes the challenge. The sources based on SBD are cost effective but was not fully explored either for communication or RADAR where phase information is a pivotal factor. Consequently, the research began with oscillator design and an intention to go to the highest THz while maintaining good performance. Initially 400GHz seemed like a good point to communicate at. What was encountered even in first multiplier stages is the power reduction which got worse with every stage and unusable by 400GHz. Multiplier design employed used a single diode per stage however literature cited with high power usually employed multiple diodes per stage. Multiple diodes seemed like an ideal way until the higher phase noise was considered leading to the choice to proceed with a single diode. Reflection on the results obtained says this was a good decision as a double conversion approach by nature uses two frequencies both of which may be substantial and allow for combined high frequencies. These substantial frequencies allow for overall frequency scaling with an oscillator in the lower THz range where sufficient power and low phase noise is conveniently obtained. For example the first mixer stage of this design in this work may be redesigned and replaced with 115GHz oscillator for an overall 300GHz system, which may very well be the optimal frequency in the quest for higher frequencies with SBD.

Mixer design was the second stage of the design procedure after oscillator design. The transistor technology and modelling formed a part of the mixer design stage as a FET approach was theoretically more viable. Graphene seemed a good candidate as well as InGaAs as the device material. To focus the scope graphene was finally decided on as it would lead to future prospect and to the relevance of the research. Concurrently while the device model was implemented it was realized the 200GHz oscillator posed some challenges to the interest of fabrication. Unfortunately time and worldwide circumstances meant parts were not available but for the sake of designing for manufacturability, the narrowband 185.9GHz oscillator was designed. Choosing GFET device dimensions was particularly designed for easy fabrication. Nonetheless high quality CVD graphene would be costly to grow on the order of 73µm dimensions and an oxide on the order of 1mm thickness. However, methods such as liquid phase exfoliations are cost effective but produce

graphene in micrometers and would still need more than one graphene flake to make a 73µm dimension. The necessity of multiple graphene flakes with imperfect contact may have some effect on transistor performance which can only be determined by a prototype.

A good test for the viability of the designed GFET was determined in the amplifier design. A bad device design would lead to unsatisfactory gain. However, the amplifier was in fact providing gain though unimpressive was quite good for THz. In fact the gain of the LNA was close to that of a microwave GFET amplifier. With all the major components in place transceiver simulation was pursued which was fraught with simulation difficulties, until finally understood how to use ADS for this purpose. An initial attempt was made to model all the components using built-in components for fast RF/DSP simulation. A difficulty with using built-in components is characterizing the GFET active circuits faithfully and what resulted was slightly too optimistic results. As a solution to this problem the exact circuits were used by providing good isolation between IQ paths and replacing only the complex oscillator with a built-in oscillator components with the respective power and phase noise values.

The initial transceiver designed was with the Zero-IF architecture and resulting from the DC offset problem was replaced with a double conversion architecture. The individual components were all performing well. However, the fundamental GFET mixer was the source of problem with Zero-IF and perhaps could have been worked on more. Nonetheless double conversion is robust and still preferred. Having simulated the BPSK transceiver the performance was promising since the signal waveforms at transmit baseband and recieve baseband had significant similarity. There was still a high error rate which could be reduced to a low figure with only a code rate of $\frac{1}{2}$ with Turbo coding. The BER could further be eliminated with a concatenated trellis convolutional code with the same code rate. Concatenated error coding are common in wireless standards for example with DVB-S2 and thus is demonstrated to be practical. Achieving a zero BER with a code rate of $\frac{1}{4}$ was a satisfying achievement considering the high effective bitrate. Initially digital PM was the primary target. What was encountered was that PM combined with Amplitude Modulation (AM) enhanced performance and a lower error rate was obtained. The high bitrates obtained with 16QAM and 64QAM were welcomed considering only 5GHz baseband bandwidth was used. Five GHz bandwidth is less than that published by any. Bandwidth is critical to any practical project for fiscal reasons. Hence making the design in this work with low bandwidth relavent. In addition the possible transmission distance of the transceivers reinforced the practicality.

A lossless channel was used in this work but to evaluate range and channel imperfections further work ought to be pursued. Further work could include suitable THz antennas, channel modelling and synchronization. Schottky THz transceivers with GFET technology have been demostrated as a viable candidate for LAN, Personal Area Network (PAN) and 6G wireless communication.

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A

LIST OF SYMBOLS

Tables A.1 and A.2 show the symbols used in this thesis.

Table A.1: Symbols

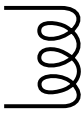
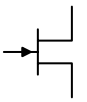
Identity	Symbol
Resistor	
Capacitor	
Inductor	
DC Source	
AC Source	

Table A.2: Symbols Continued

Mixer	
GaAs HEMT	
GFET	
Schottky Diode	
Ground	
Input/Output Pin	
Generic Block