Study and Evaluation of Multilayer PCB Manufacturing Inaccuracies on Malfunctioning of Circuits

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Declaration

I, the undersigned, declare that this thesis work is my original work, has not been presented for a degree in this or any other universities, and all sources of materials used for the thesis work have been fully acknowledged.

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This thesis has been submitted for examination with my approval as a university advisor.

Prof. Mohammed Abdo	_____	_____
Name	Signature	Date

Dedication

This thesis is dedicated to my father!!!

Acknowledgment

First of all, I would like to give my highest gratitude and appreciation to my advisor Prof. Mohammed Abdo for his continuous follow ups, support and guidance during my thesis work. This thesis wouldn't have been successful if his efforts and contributions were not there. Next, I am also thankful to Dr. Getachew Alemu for delivering continuous follow ups and constructive comments during the seminars.

Lastly, I would like to express my admirations and heartfelt gratitude to the school of Electrical and Computer Engineering for facilitating all the required things to carry on my thesis and providing all the necessary materials required for my study. I am also thankful to the staff members of school of ECE, particularly to the Microelectronics Engineering team for providing me the required softwares and guidance.

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List of Acronyms

PCB	Printed Circuit Board
CSPs	Chip Scale Packages
LDI	Laser Direct Imaging
AOI	Automatic Optical Inspection
ICs	Integrated Circuits
Df	Dissipation factor
Dk	Dielectric constant
DMD	Digital Micro-Mirror Device
UV	Ultra Violet
LFD	Lithography Friendly Design
RET	Resolution Enhancement Technique
OPC	Optical Proximity Correction
PV	Process variation
PTH	Plated Through Holes

Abstract

The PCB is a mechanical base used for interconnection of electronic components. In PCB manufacturing industry, the quality and reliability of circuits is highly dependent upon the accuracy of the manufacturing processes. Because of the different factors affecting the processes to function imperfectly, manufacturing processes inaccuracies like photolithography inaccuracy, etching inaccuracy, drilling inaccuracies and inaccuracies in other processes may be encountered. These inaccuracies cause severe problems that may result in degradation of circuit performance and malfunctioning of circuits.

In this research the levels of effects of the manufacturing inaccuracies on the malfunctioning of PCB circuits is investigated and analyzed. The effects of each process inaccuracies on circuits as well as how the processes are related with the affecting parameters are addressed in this thesis.

A four-layer multilayer board is considered and the software selected to study the effects of manufacturing inaccuracies is OrCAD PCB designer. The major PCB manufacturing processes considered are Photolithography, Etching, and Drilling. Schematic development, PSpice simulation and layout design are made for selected circuits to study the effects of inaccuracies.

According to the results obtained, drum speed, resolution and ratio of track to track spacing are the affecting parameters in Photo plotting while depth of focus, dose and mask bias variations are the factors affecting photolithography.

In addition, inaccurate etching results in either larger or smaller width of traces, leaves unwanted conductive materials, creates unnecessary holes or open circuits and short circuits. In the case of drilling, when there is wrongly or inappropriately drilled, the top and bottom layers may not be connected and creates open circuit.

In the over etching case simulation, 64 % of the output voltage reduction occurred for a 69% increase in resistance. This simply considering only one simple scenario the effect will be even worsened when similar individual effects are added to it. For capacitive effects, the output becomes unstable and oscillating.

Keywords: PCB, Inaccuracies, photolithography, etching, drilling, OrCAD

Chapter One

Introduction

1.1 Background

A printed circuit board (PCB) is a device used for mounting electronic components and providing electrical interconnections to the circuits that are found in electronic or electrical devices and systems.

PCB is constructed from an insulating material placed as the core and conducting material i.e. copper coated on the surfaces. This copper plating is etched away to form the actual copper pads and connection traces on the board surfaces as part of the board manufacturing process.

There are three major types of printed circuit board constructions namely, single-sided, double-sided and multi-layered. Single-sided boards are with copper pads and traces on one side of the board and the components are on one side of the substrate. When the number of components becomes too many for a single-sided board, a double-sided board may be used in which there are copper pads and traces on the top and bottom sides of the board. Electrical connections between the circuits on each side are made by drilling holes through the substrate in appropriate locations and plating the inside of the holes with a conducting material. The third type, a multi-layered board, has a substrate made up of layers of printed circuits separated by layers of insulation. It is designed with copper pads and traces on top and bottom of board with a variable number of internal copper layers with traces and connections. The components on the surface connect through plated holes drilled down to the appropriate circuit layer [1].

A multilayer board consists of a number of layers of dielectric material that has been impregnated with adhesives, and these layers are used to separate the layers of copper plating. All of these layers are aligned and then bonded into a single board structure under heat and pressure. Multilayer boards with 48 or more layers can be produced with today's technologies.

In this research a four-layer multilayer board was considered. In four-layer multilayer PCB the external two layers are called signal layers in which all the circuit and electronic component

placement takes place and the remaining internal layers are dedicated for power and ground interconnections [1].

At the end of all manufacturing steps, malfunctioning of PCB circuits may be encountered due to the inaccuracies of the manufacturing processes. Levels of effects of the inaccuracies could be different due to the different nature and sensitivities of the processes.

In this research the levels of effects of the manufacturing inaccuracies on the malfunctioning of PCB circuits was investigated and analyzed.

1.2 Motivation

PCB is basic component which serves as a base of interconnection board to all components and circuits found in electronic systems and devices. The performance electronic devices mainly depend on the quality and accuracy of the manufactured PCB. If there is even a minor defect in the PCB, the whole PCB circuit may malfunction which finally results in failure of electronic device. Such a PCB doesn't meet the objective it is designed for. Most of the time, such defects happen due to problems or inaccuracies of PCB manufacturing processes. These types of possible failure are fatal and their levels of effects on malfunctioning of PCB circuits must be well known so that appropriate measures and precautions can be taken.

1.3 Problem Description

PCB manufacturing processes must be accurate to minimize the failure of circuits after final production. To avoid the possible failures in PCB circuits, analysis of effects of individual process inaccuracies on the level of malfunctioning of circuits is important. It helps give awareness in making processes accurate and avoid the possible causes of PCB process inaccuracy.

The study of manufacturing inaccuracies and their effects in circuits is very important as it paves way for making processes more accurate and building robust PCB circuits and then meets customer satisfaction.

As it is very well known, the inaccuracies of the processes followed by the manufacturing technology are the main reasons for circuit malfunctioning.

Therefore, in this research we are going to identify the individual process inaccuracies along with the factors affecting them and the corresponding effects on the level of malfunctioning of circuits.

Multilayer PCB processes will be the focus area as this is the main priority area in modern electronics Technology and with complex process that needs great attention.

1.4 Objectives

1.4.1 General Objective

The main objective of the research is to evaluate the effects of Multilayer PCB manufacturing inaccuracies on the level of malfunctioning of circuits

1.4.2 Specific Objectives

The specific objectives of the thesis are:

- To investigate Multilayer PCB manufacturing Processes
- To identify Individual Manufacturing Process inaccuracies
- To identify factors affecting the process inaccuracies
- To evaluate the effects of the inaccuracies on the level of malfunctioning circuits
- To create awareness about the effects of imperfection of PCB manufacturing processes
- To pave way for future researches on improving each process accuracy

1.5 Scope of the thesis

Scope of the thesis is limited to the investigation and evaluation of effects of manufacturing processes inaccuracies in four-layer multilayer PCB Manufacturing Processes focusing on major processes like Photolithography, Etching and Drilling.

1.6 Significance and Contribution of the Study

The significance of this thesis is to give an analysis of the effects of manufacturing processes inaccuracies on the level of malfunctioning of circuits and hence, create an awareness on PCB failure causes and the measure that has to be taken.

1.7 Thesis Outline

The thesis is organized in the following way. Chapter one discusses about the introduction of the research including the problem description and the objectives of the study. Chapter two is about Background study of PCB manufacturing processes and related works. Chapter three is on developing prototype-circuit model with each process inaccuracy which includes Circuit modelling and affecting parameters, behavior of circuits without inaccuracy, behavior of circuits with inaccuracy, and Simulation of effects on the level of malfunctioning of circuits. Chapter four discusses the Results and analysis of effects. Finally, Chapter five focuses on Conclusions and recommendations for future works.

Chapter Two

Background and Related Works

2.1 Introduction

In this chapter, the investigation of basic concepts and related works are addressed. In the first part, the discussions of the multilayer PCB manufacturing processes are presented followed by the survey of related works on this research.

2.2 Photo plotting

Photo Plotting is the process of transferring the electronic data called Gerber file for a layer onto an etch resist film that is placed on the conductive copper layer. Photo plots are developed according to Gerber file or vector graphics film extracted from the PCB designer. The most recent development related to photo plotting is LDI (Laser Direct Imaging) which utilizes a high-power laser or Xenon lamp to directly expose photoresist on a coated substrate instead of exposing photographic film [2]. This eliminates the handling of photographic film. The formats acceptable by the LDI photo plotters are Gerber format or another bitmap format.

2.3 Resist Lamination and Photolithography

Resist lamination is the process of lamination of internal layers with a photo sensitive dry resist under extreme conditions (temperature and pressure).

Photolithography is a process of exposing the resist to UV light using the photo plots. Exposure units can easily be made using standard fluorescent lamp ballasts and UV tubes. For small PCBs, two or four 8 watts 12" tubes will be adequate, for larger ones A3 units, four 5-watt tubes are ideal. To determine the tube to glass spacing, place a sheet of tracing paper on the glass and adjust the distance to get the most even light level over the surface of the paper. Even illumination is a lot easier to obtain with 4-tube units. They look white or occasionally black/blue when off, and light up with a light purple, which makes fluorescent paper etc. A timer which switches off the UV lamps automatically is essential and should allow exposure times from 2 to 10 minutes in 15-30

second increments. It is useful if the timer has an audible indication when the timing period has completed [3].

Generally speaking, overexposure is better than underexposure. In the manufacturing of printed circuit boards, chip scale packages (CSPs) and other complex circuitry, lithography techniques are used extensively nowadays. These allow for the creation of extremely small features with high accuracy. During a longtime period, the trend in the industry has been towards reducing the feature size while increasing the accuracy of placement. For feature sizes in the order of micrometers, mask photolithography using optical steppers is widely used. In this technique, optical radiation is used to image the pattern from a predefined transparent plate with a pattern (mask or artwork) created on the substrate using photoresist layers which cause a spatially selective etching. The photoresist is a light sensitive material that, when exposed, will either lose its resistance when attacked by an etchant or solvent (positive photoresist) or strengthen its structure and leave the unexposed portions soluble (negative photoresist).

2.4 Image development, Etching & Resist Stripping

The exposed inner layers are developed in a 1% sodium carbonate solution. Removes resist from areas that were not hardened (polymerized) by the light. In Inner Layer Etching copper is chemically removed from the areas where the dry film is removed. This creates the copper pattern that matches the film pattern. the traditional process of exposing the copper and other areas unprotected by the etch resist film to a chemical that removes the unprotected copper, leaving the protected copper pads and traces in place; newer processes use plasma/laser etching instead of chemicals to remove the copper material, allowing finer line definitions.

In Resist Stripping developed dry-film resist is chemically removed from the panel leaving the copper on the panel. In this Traces, pads, ground plane and other design features are exposed. Finally, Automated Optical Inspection (AOI) is done after resist stripping. Inner layers are then inspected against design rules using data from the Gerber files. After inspection, the panels are chemically coated with oxide to improve adhesion of the copper surface [3].

2.5 Laminated Panel/Pressing

The basic materials needed to build a multi-layer board are copper foil, pre-preg and inner-layer

cores. Inner layer core, copper foil and pre-preg are bonded together under heat and pressure, sometimes in a vacuum, during the lamination process. The result is a panel with several layers of copper inside as well as the foil on the outside. Pressing is the process of aligning the conductive copper and insulating dielectric layers and pressing them under heat to activate the adhesive in the dielectric layers to form a solid board material.

2.6 Primary Drilling

Holes of various sizes are drilled through a stack of panels. The locations are determined by the board's designer to fit specific components. the process of drilling all of the holes for plated through applications; a second drilling process is used for holes that are not to be plated through. Information on hole location and size is contained in the drill drawing file. this is required when holes are to be drilled through a copper area but the hole is not to be plated through. Avoid this process if possible because it adds cost to the finished board [3].

2.7 Deburr and Desmear

Deburr is an abrasive mechanical process that removes the raised edges of the metal or burrs surrounding the holes that occur during the drilling process. Any debris that may be left in the holes is also removed at this time.

On the other hand, Desmear is a chemical process that removes the thin coating of resin from the inner layer connections that is produced by the heat and motion of the drill bits as they create the holes. Deburr & Desmear Removing the resin smear improves the electrical connectivity.

2.8 Electroless Copper Deposition

A thin coating of copper is chemically deposited on all of the exposed surfaces of the panel, including the hole walls. This creates a metallic base for electroplating copper into the holes and onto the surface. It is also the process of applying copper plating to the pads, traces, and drilled through holes that are to be plated through; boards are placed in an electrically charged bath of copper.

Finally, the above process steps are repeated for the outer layers. Completed boards are also tested for functional performance to ensure their output is within the desired limits. Some boards are

subjected to environmental tests to determine their performance under extremes of heat, humidity, vibration, and impact.

2.9 PCB manufacturing rules

2.9.1 Component Placement

Components that need to be in specific locations are placed first. This includes connectors, switches, LEDs, mounting holes, heat sinks or any other item that is mounted to an external location. Careful thought must be given when placing component to minimize trace lengths. Put parts next to each other that connect to each other. 0.350″ – 0.500″ gap is given between ICs, for large ICs even more is allowed. It is very important to measure the pin spacing and pin diameters as accurately as possible.

After placing all the components, a copy of the layout is printed out. Place each component on top of the layout. Availability of enough space for every part to rest without touching each other is checked.

2.9.2 Placing Power, Ground and Signal Traces

After the components are placed, the next step is to lay the power and ground traces. It is essential when working with ICs to have solid power and ground lines, using wide traces that connect to common rails for each supply. It is very important to avoid snaking or daisy chaining the power lines from part-to-part [4].

When placing traces, it is always a good practice to make them as short and direct as possible. Vias (feed-through holes) are used to move signals from one layer to the other. A via is a pad with a plated-through hole. Generally, the best strategy is to lay out a board with vertical traces on one side and horizontal traces on the other. Add via where needed to connect a horizontal trace to a vertical trace on the opposite side.

A good trace width for low current digital and analog signals is 0.010. Traces that carry significant current should be wider than signal traces. The table below gives rough guidelines of how wide to make a trace for a given amount of current.

No	Trace width (in inches)	Current carrying capacity (in Amps)
1	0.01	0.3
2	0.015	0.4
3	0.02	0.7
4	0.025	1
5	0.05	2
6	0.100	4
7	0.15	6

Table 1:Trace width Vs Current carrying

When placing a trace, it is very important to think about the space between the trace and any adjacent traces or pads. You want to make sure that there is a minimum gap of 0.007″ between items, 0.010″ is better. Leaving less blank space runs the risk of a short developing in the board manufacturing process. It is also necessary to leave larger gaps when working with high voltage.

It is a common practice to restrict the direction that traces run to horizontal, vertical, or 45-degree angles. When placing narrow traces, 0.012″ or less, avoid sharp right angle turns. The problem here is that in the board manufacturing process, the outside corner can be etched a little narrower. The solution is to use two 45-degree bends with a short leg in between.

Especially in analog circuits, it is important that "ground" means the same voltage throughout the PCB. If you use traces to route the ground signal, their resistance will create voltage drops that will make different "grounds" in the PCB have different potentials. To avoid that, we should create a ground plane, i.e., a large area of copper (or even better, reserve a layer for the plane) where the components connecting to ground can do it directly through vias.

2.10 Related Works

2.10.1 Effect of type of material and trace roughness on insertion loss

Marina Y. Koledintseva and Praveen K. R. Anmula [5] from Missouri University of Science & Technology correlated the effect of conductor roughness to insertion loss. The insertion loss due to copper roughness induced is less significant at lower speeds but cannot be ignored at frequencies

above a few GHz. Accurate estimation of PCB laminate dissipation factor (Df) is another goal integral to SI modeling. Industry-standard methods again assume the smooth copper case, with consequent frequency-dependent error introduced into extracted values of Df. Researchers have correlated the cooper trace roughness to insertion loss using different stripline PCB test vehicles [5]; the main errors induced in extracted values of Df resulting from increased conductor losses due to surface roughness have been analyzed. It was found that the copper foil type was of considerably greater significance than the inner-layer surface treatment.

The changes in dielectric constant and dissipation factor values for a variety of PCB laminate materials and different operating temperatures were also analyzed [6], and the results show that at the stage of SI modeling, circuit designers contemplating use of such materials should account for significantly higher Dk and Df values than those at room temperature. The Dk value for most materials is stable (less than 1% change) over the temperature range from 23-75 ^{o}C except for some materials about 9% change, but the Df value changes by an average 22% increase for most materials when going from room temperature to higher temperature (23-75 ^{o}C).

In [7], [8] an analytical model was presented to predict laminate deformations of PCBs in relation to their manufacturing process steps. The observation was the shape of the laminate is cylindrical. The short side is almost flat. Curvature along the long side of the laminate changes the moment of inertia of the sample. A clear increase in deformation was found when the ratio width vs. length reaches unity. The model can predict the behavior of bi-layer samples and multiple press steps; however, it struggles with accurate predictions for the plating process and patterned layers.

2.10.2 Photolithography Process

High Overlay Accuracy Using Scaling Method in PCB Photolithography to enhance product yield and overlay pattern accuracy was proposed [9]. It uses step and repeat projection exposure method which allows non-contact patterning. The performance of critical dimension uniformity with new lens will achieve within ±1.5 μm for 100μm focus range, and evaluation has proved that the overlay accuracy of approx. ±3 μm can be achieved by optimizing the exposure area.

Moreover, in other researches such as [10-13], machine vision technique was used to inspect problems in solder joint integrity and top-surface component placement in PCBs. in this study, several production stages are addressed in which automated visual inspection plays a key role,

from artwork to lamination of multiple layers and plated-through holes. Spectral-reflectance measurements were made on the substrate and the inks of some circuit modules, and the result indicated that maximum contrast should be attained in the 0.4-0.6-pm wavelength range.

2.10.3 Drilling Process

Another study, [14] indicates the use of quality tools to optimize the drilling process and the production yield at the Chippewa Valley Wisconsin company. An analysis of variance study was used to determine the optimal machine vision targeting method and cycle time performance. The optimizer has provided a 2% increase in machine utilization and has provided a reduction in internal shorts due to drill registration. In [15], analysis of influencing factors of holes' position accuracy and drilling optimization was also done. From that study value of CPK will increase with the spindle speed, retraction speed and drill diameter; and it will decrease with the increase of the feed speed, the number of drilled holes and the thickness of entry board.

2.10.4 Effect of Vibration on PCB

PCBs are prone to failure due to shock or vibration loads [16]. Investigation of the contributions of PCB manufacturing variability including variability in materials and assembly on PCB failures due to Vibrations was made. Finite element model is used to predict the local vibration response.

In [17], the printed circuit board (PCB) industry has long used a lithography process based on a polymer mask in contact with a large, resist-coated substrate. There is a limit to this technique since both the masks and PCB substrates themselves may undergo distortion during fabrication, making high resolution or tight registration difficult. The industry has increasingly turned to digital lithography techniques which, in addition to eliminating the masks, can actively compensate for distortions. Many of these techniques rely on a "dot-matrix" style exposure technique that uses "binary" pixels and small pixel or dot spacing to achieve the required resolution. This results in limitations in write speed and throughput, since many small pixels or dots must be written over a relatively large area PCB substrate. A patented gray level technique1 based on a commercially available digital micro-mirror device (DMD) achieves required resolutions with a relatively large projected pixel size, and thus offers a higher speed alternative to conventional digital techniques.

The technique described is not limited to PCB but may be applied to any lithography or printing-based application where high speed and accurate registration are concerns.

In [18], A Printed Circuit Board (PCB) consists of circuit with electronic components mounted on surface. There are three main steps involved in manufacturing process, where the inspection of PCB is necessary to reduce the defects. First step is printing; second step is the components fabrication over the PCB surface and third is the components soldering. In this paper Machine Vision PCB Inspection System is applied at the first step of manufacturing, i.e., the making of bare PCB. We first compare a standard PCB image with a PCB image to be inspected, using a simple subtraction algorithm that can detect the defected regions. Our focus is to detect defects on printed circuit boards. Typical defects that can be detected are over etchings (opens), under-etchings (shorts), holes etc.

2.10.5 Etching Process

There are two basic ways to remove unwanted copper from copper clad substrates to form electronic circuits:

1. Mechanical etching: involves the use of a machine tool and a special cutter to remove a narrow strip of copper from the boundary of each pad and trace - this electrically isolates the circuit element from the rest of the foil

2. Chemical etching: relies on the action of a corrosive liquid to dissolve away unwanted copper in order to define the desired circuit. In [19], chemical Etching is usually done by total immersion of the board in the chemical and agitating by bubbling air through the bath. The copper which is to remain on the PCB is protected from the etchant by an etch resist. The process of chemical etching in PCB is low in cost, fast, and easily repeatable.

Impact of etch factor on characteristic impedance, crosstalk and board density are [20]:

- The effect of three different etching shapes on characteristic impedance.
- The shape of the trace cross section has influence on the inductance and the capacitance of the trace

- A higher etch factor results in lower inductance and higher capacitance which bring the characteristic impedance of the trace closer to the theoretical value considered by board designers.

2.11 Summary of Literature

To summarize the above literatures and intended area of study, most of the researches done so far are focusing on optimization of single Processes like drilling, photolithography; and study of change in dielectric constant, dissipation factors and PCB failure due to vibrations. On the other hand, researches on PCB Manufacturing processes inaccuracies and their levels of effects in the PCB circuits are left for further researches. The study of manufacturing inaccuracies and their effects in circuits is very important as it paves way for making processes more accurate and building robust PCB circuits and then meets customer satisfaction.

As it is very well known, the inaccuracies of the processes followed by the manufacturing technology are the main reasons for circuit malfunctioning.

Therefore, in our research we are going to identify the individual process inaccuracies along with the factors affecting them and the corresponding effects on the level of malfunctioning of circuits.

Chapter Three

Effects of PCB Manufacturing Processes Inaccuracies

3.1 Introduction

In this Chapter, the effects of each process inaccuracies on circuits as well as how the processes are related with the affecting parameters are addressed. Process Control parameters for each manufacturing processes are discussed. The concept behind interpreting the effects of inaccuracies into circuit modelling prior to simulation is also presented. The model must show how the manufacturing process depend on the process control parameters. Moreover, process sensitivities are estimated by the model. The process sensitivity to some changes in their control parameters are also theoretically addressed.

Once representation of effects (model) is available, it is possible to understand the consequences of such inaccuracies on circuits as well as understanding the way how they can be solved to mitigate such manufacturing problems. Once the circuit model is available, it is convenient to do the simulation of the process steps in a computer program called OrCAD PSpice.

3.2 PCB Defects

As there are some defects commonly found on PCB. Most of the time such defects occur due to the inaccuracies in the manufacturing processes. There are two categories of defects of PCB due to manufacturing problems. These are called potential and fatal defects. Fatal defects are those in which the PCB does not meet the objective for which it is designed for, while the potential defects are those which compromise the PCB performance during utilization. Conductor breaking and short-circuit are characterized as fatal defects. Pinhole, breakout, over etch, and under etch are characterized as potential defects [21]. During etching process, the anomalies occurring on bare PCB could be largely classified in two categories: one is excess of copper and the other one is missing copper. The incomplete etching process leaves unwanted conductive materials and forms defects like short, extra hole, protrusion, island, and small space. The excessive etching makes open, pin hole, nick (mouse bite), and thin pattern. In addition to the defects mentioned above,

some other defects may exist on bare PCB, for example, missing holes (due to tool break), scratch (due to handling mistake), and cracks.

These different types of PCB defects cause failure of the board which includes Board delamination, Component misalignment, Broken metal lines, Cold-solder joints and poor die bonding, Surface contamination by metal and ionic residues.

Because of the complex nature of the PCB manufacturing processes, these defects must be analyzed and inspected through an automated system such as by machine vision using algorithms developed for it. So, machine vision provides a measurement technique for regularity and accuracy in the inspection process. Machine vision is concerned with the theory behind artificial systems that extract information from images and sequence of images. The image data can take many forms, such as video sequences, views from multiple cameras, or multi-dimensional data from a medical scanner.

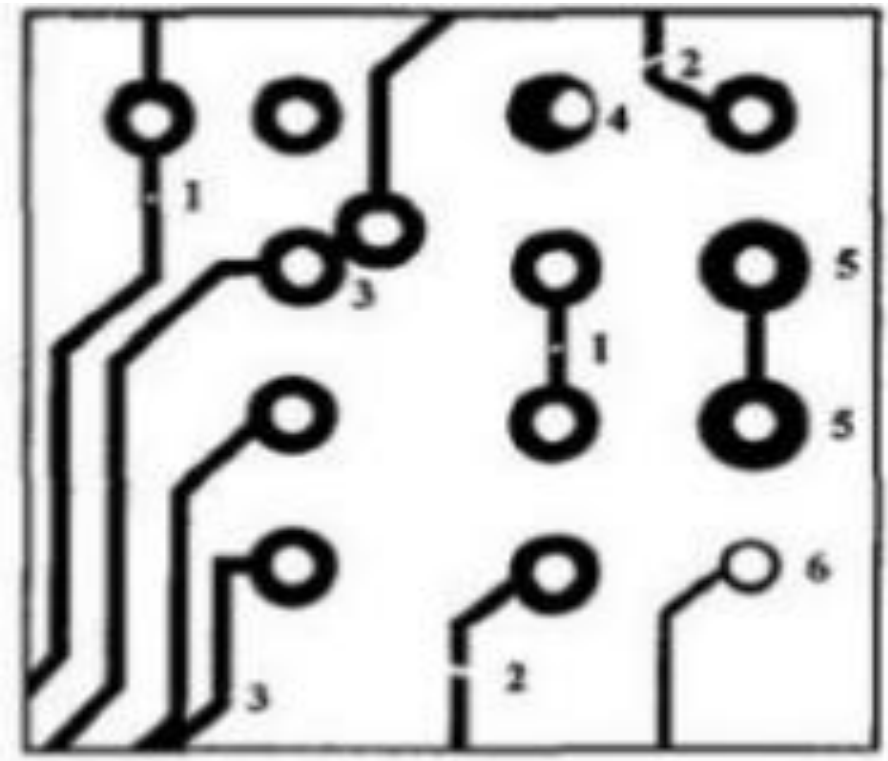
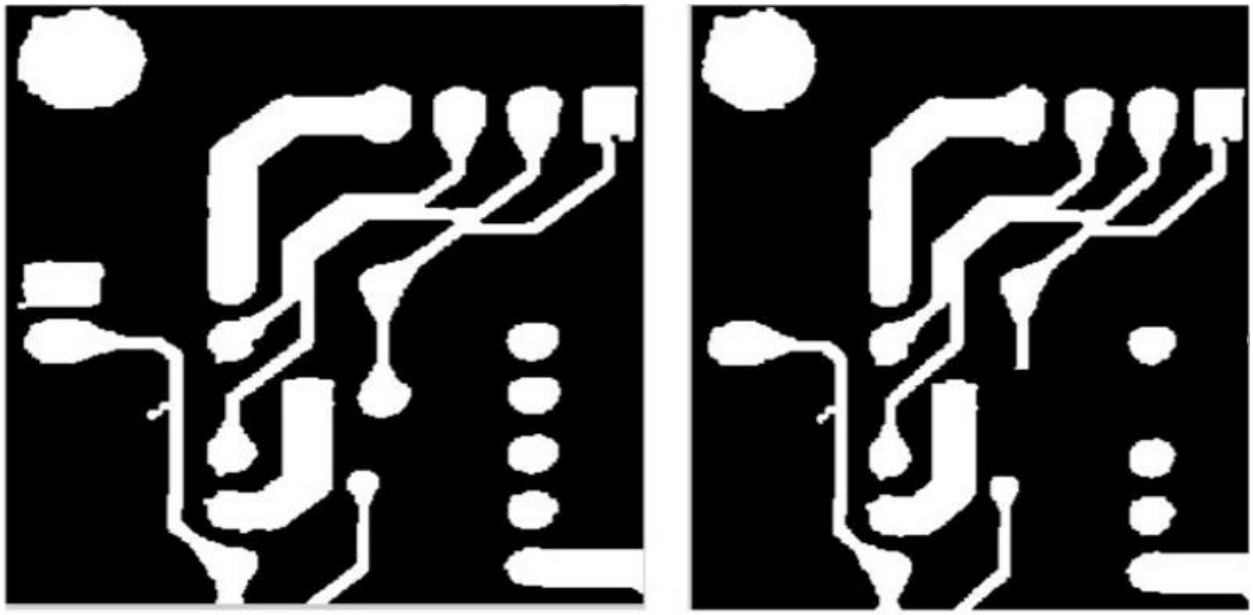


Figure 1: PCB defects [21]

1-pin hole, 2-conductor breaking, 3-short circuit, 4-breakout, 5-underetch, and 6-overetch



a) Good PCB b) Defective PCB

Figure 2:Comparison of images of good PCB and defected PCB [21]

FATAL	1 Breaks	1.1 Fracture
		1.2 Cut
		1.3 Scratches
		1.4 Cracks
	2 Shorts/bridges	
	3 Missing conductor	
	4 Incorrect hole dimension	
	5 Missing hole	
POTENTIAL	6 Partial Open	6.1 Mouse bit
		6.2 Nicks
		6.3 Pinholes
	7 Excessive spurious	7.1 Specks
		7.2 Spurs/protrusions
		7.3 Smears
	8 Pad violations	8.1 Under etching
		8.2 Over etching
		8.3 Breakout
	9 Variations between the printed lines	9.1 Small thickness wiring
		9.2 Large conductors
		9.3 Excessive conductors
		9.4 Incipient short (conductor too close)

Table 2:PCB error classification [21]

3.3 Photo plotter Inaccuracies and affecting parameters

The affecting parameters in photo plotting are drum speed, resolution and ratio of track to track spacing. If the photo plotter is high speed with wrong resolution, a blurred edge of tracks, pads and wrong sizes of tracks may occur. In that case, when UV light is exposed, there will be

misalignment blurred tracks with wrong sizes and spacing which can finally result in poor circuit performance and malfunctioning.

Considering figure 3 we can observe that the correct versus wrong track to track spacing. The correct diagonal track-to-track spacing on mitred corners is 25mil with track width of 12.5mil.

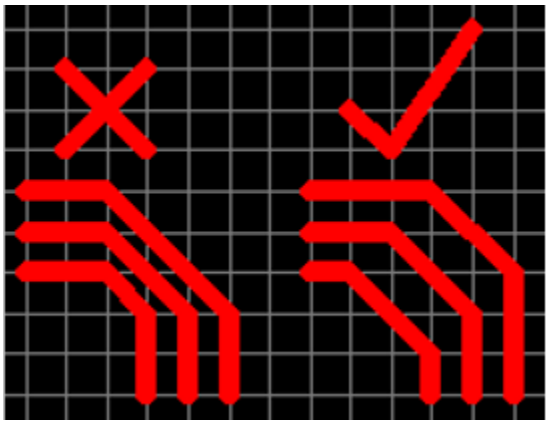


Figure 3:Bad versus good PCB photo plotting [23]

3.4 Photolithography Inaccuracies and Process affecting parameters

Photolithography is one of the PCB manufacturing processes used in microfabrication to pattern parts of a thin film or the bulk of a substrate[24]. Photolithography lays down patterns on layers, allowing other processes to produce the required circuit devices and interconnections.

In photolithography light is used to transfer a geometric pattern from a photomask to a light sensitive chemical photoresist on the substrate. The photolithography process controlling parameters are depth of focus, dose and mask bias variations [25]. Small changes in the process parameters like changes in dose, focus, or mask bias results in change in the delay and leakage. This finally has a direct effect on the performance and functionality of PCB circuits. The effects of these parameters are discussed as follows.

Depth of focus

Depth of focus is the parameter that defines how accurately the thickness of the layer is reflected while printing the pattern onto mask/silicon. During photo plotting, each layer has a separate mask which has to be aligned and mirrored accurately with respect to the other layers. Each layer has a finite thickness so during photolithography it is required that the actual thickness of the layer be

reflected while printing the pattern on the mask/silicon. The greater the depth of focus, the better will be the alignment between the masks. A process with small depth of focus has poor alignment and wrong patterns. This finally results in wrong circuit/component connections which results in malfunctioning of the circuit or poor performance of circuits depending on the value of the depth of focus.

Dose

During photolithography, when the substrate is exposed to the light through the mask, the applied positive photoresist becomes more soluble in the developer solution. In order to completely remove the photoresist from the exposed regions, the exposed resist must absorb a sufficient intensity of light otherwise the exposed resist won't be completely removed in the developer solution and will leave some resist in those regions. In addition, there may be variations in the intensity of light in various regions of the substrate. If the wrong dose is used, all the resists exposed may not be completely removed and hence, unnecessary strips of copper results. On the other hand, if the intensity of the UV light is not uniform, a similar situation may appear. This finally results in printing imperfections and therefore poor yield and circuit performance.

Mask bias variations

These are mainly introduced during the manufacturing of the mask itself. The silicon printed images are simulated for variations in the process parameters discussed above and a contour is obtained. A Process Variation (PV) band is the representation of the possible simulated contours obtained by the variations in the process parameters. Several contours combined together make a PV-band. PV-bands show how much and where a design will vary in response to process variations. Each PV-band represents all possible printing locations resulting from one set of doses, focus, mask bias, resist, and etch variation conditions. Figure below represents a typical process variation band for a given set of process parameters namely, dose and focus.

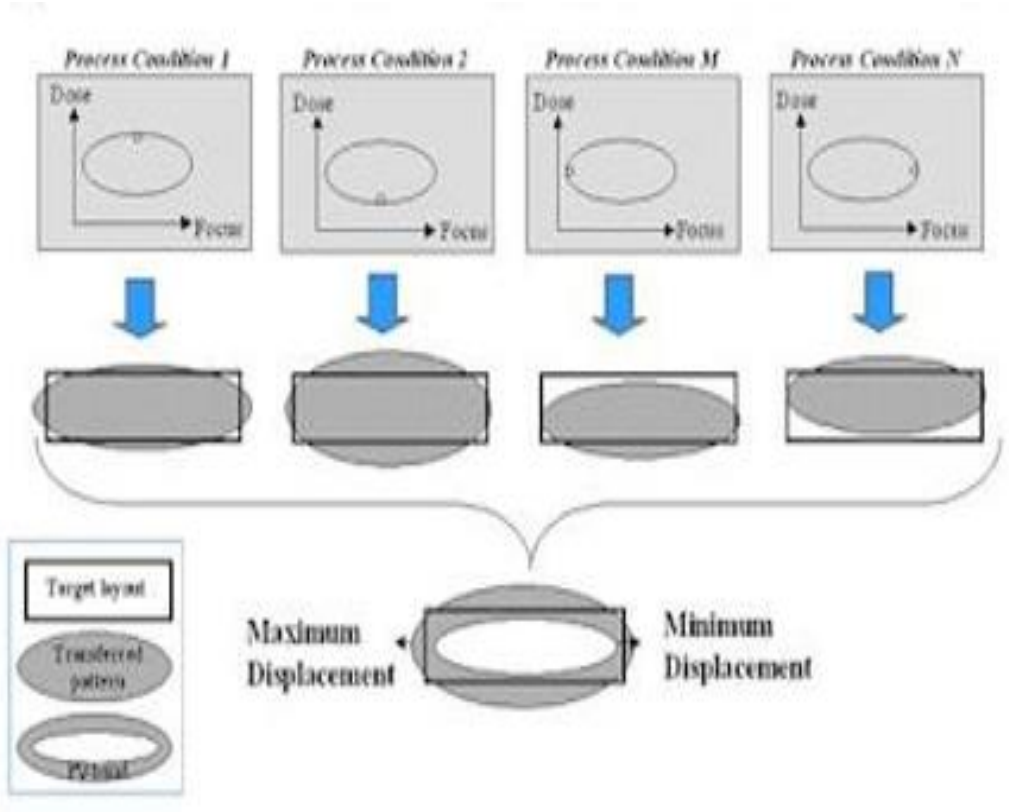


Figure 4:Process Variation Band [25]

Evaluation of Photolithography inaccuracies on the level of Malfunctioning circuits

[25] Inability of the complex conditional and recommended Design Rule Checks (DRC) to model the sensitivity of a Photolithographic process window to the actual features being printed has made designers to comply with Lithography Friendly Design (LFD). The LFD flow describes common printability failures to maximize the yield of the design.

Identification of hotspots using PV-Bands

The following terms are very important and explained as follows.

Inner tolerance band is the edge of the printability region (region independent of process variations) which is defined by the minimum LFD width. Minimum LFD width is the minimum value of the width which a pattern should have to get printed without resulting in any manufacturability failure. It is similar to minimum allowed width of a metal route as defined in the DRC rules.

Outer tolerance band is the outermost edge of the PV band which is allowed so that the spacing between the PV bands of the adjacent patterns does not go below the minimum LFD spacing between the two adjacent PV bands.

Lithography inaccuracy levels of failures on circuits

Pinching failure

If the inner edge of the PV band of a target pattern lies within the inner tolerance band, then pinching failure occurs. This is because the width of the PV band of the target pattern becomes less than the minimum LFD width. This can be detected by overlapping the PV band of target pattern with the inner tolerance band. Pinching may result in opens or voids in the pattern. This failure is shown in figure 5.

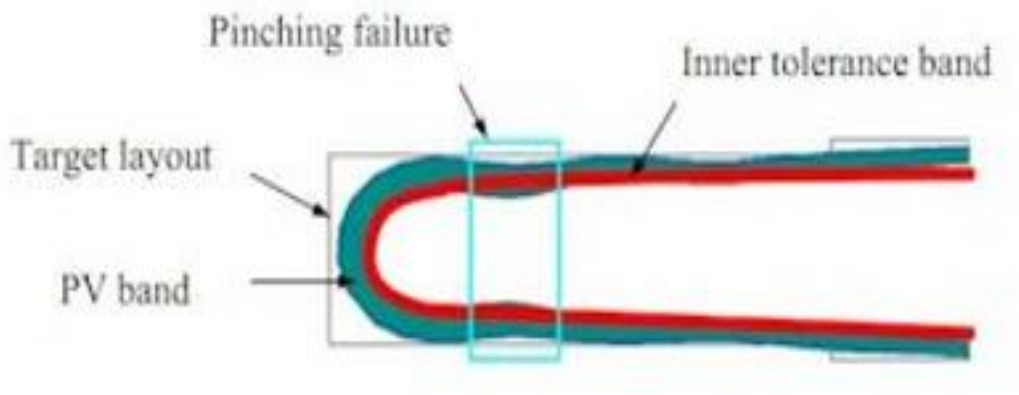


Figure 5:Pinching failure [25]

Bridging failure

If the PV band of a target pattern lies outside the outer tolerance band, then bridging occurs. This is because the spacing between the PV bands of the adjacent target patterns may become less than the minimum LFD spacing. A bridging failure can be detected by overlapping the PV band of the target pattern with the outer tolerance band and it exposes locations (on the PV band) that lie outside the outer tolerance band, which indicate bridging hotspots. Due to bridging, the PV-band for one feature overlaps or comes very near the PV-band of another feature which may result in

shorts. This failure is shown in figure 6. Circuits with this type of failures malfunctions due to formation of short-circuits which is a fatal error or gives undesired result and performance of a circuit.

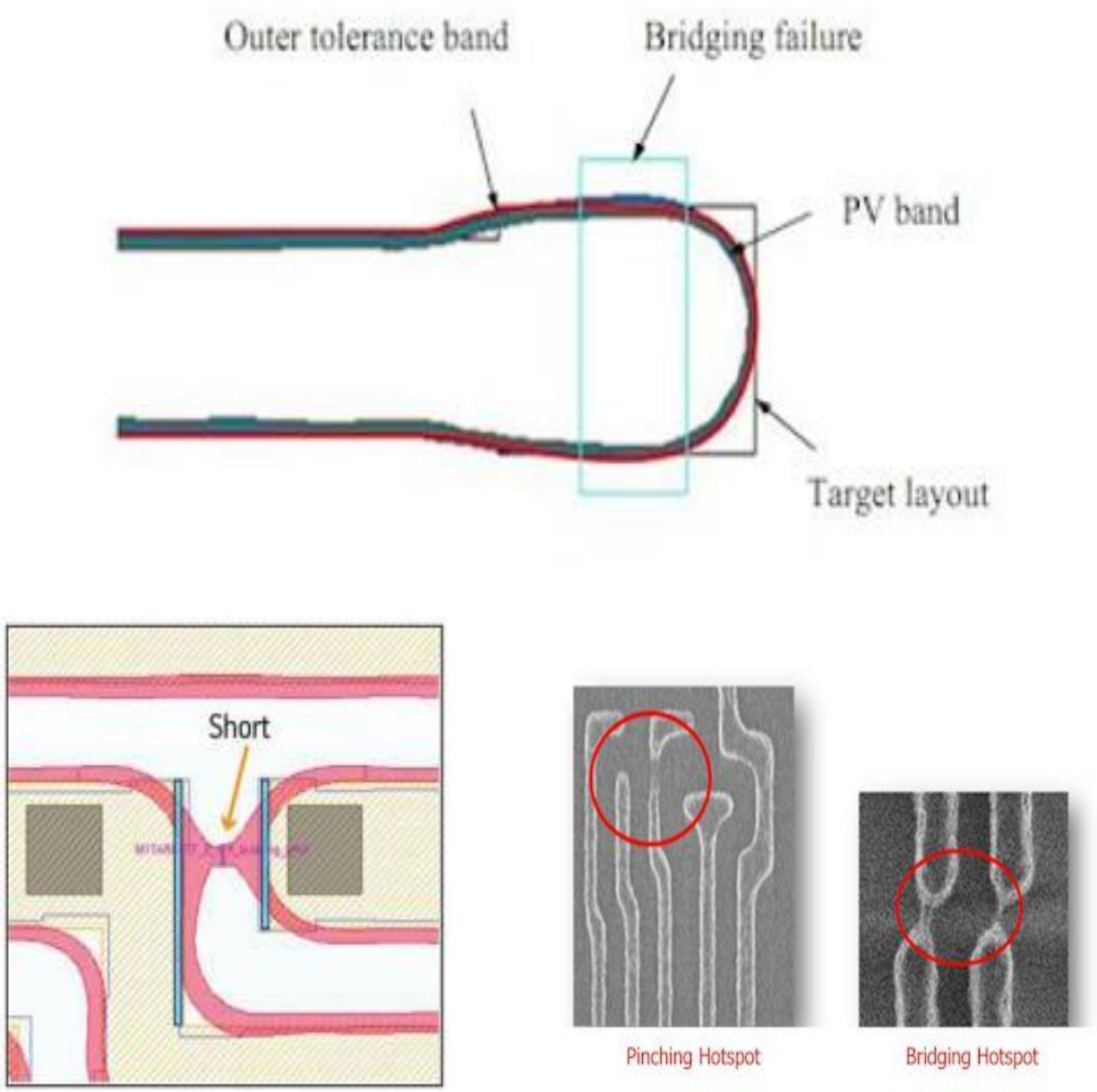


Figure 6:PV band Bridging failures [25]

3.5 Etching Process Inaccuracies and Affecting parameters

PCB circuits can be malfunctioned due to the inaccurate etching of traces in the etching manufacturing process. The inaccurate etching results in either more width of cupper (more width of traces than normal) or small width of traces (small cupper). In addition, the inaccurate etching process leaves unwanted conductive materials, creates unnecessary holes or open circuits. This inaccuracy of PCB etching which results in thicker width of traces and unwanted copper on the board may result in short circuits. On the other hand, the excessive etching which happens in thinner traces and gaps may result in open circuits. Those defects are called fatal defects. There are also other forms of defects due to the inaccurate etching process which doesn't directly malfunction PCB circuits. Those types of irregularities form neither short circuits nor open circuits immediately. Due to the inaccurate size of traces and holes on PCB circuits, the performance of the circuit is compromised. Such defects are called potential defects.

Since copper is not a perfect conductor, the inaccurate etching or inexact sizes of traces and holes (smaller sizes) presents a certain additional amount of impedance to current flowing through it, this additional impedance results in extra energy lost in the form of heat [27]. Moreover, when signal traces are smaller in width than normal, signal loss in the circuit occurs.

3.5.1 Controlling parameters of Etching process

There is a need to study the combined effects of all other parameters on etching. The measuring parameters that affect the performance of etching process (parameters that influence the accuracy of etching process) are material removal rate, etch factor, undercut, concentration of etchant, etching time and etchant temperature. An optimal parameter combination for maximum material removal rate and undercut within the range selected control parameters are obtained by using analysis of variance [27].

Parasitic impedance in high-speed PCBs destroys circuit performance [28]. PCB parasites are in the form of undesired capacitors, inductors and resistors embedded within the PCB.

Trace/Pad capacitance

A trace capacitance is given as follows. Capacitance decreases with increasing board thickness or layers, reducing trace/pad area, and with removal of ground plane.

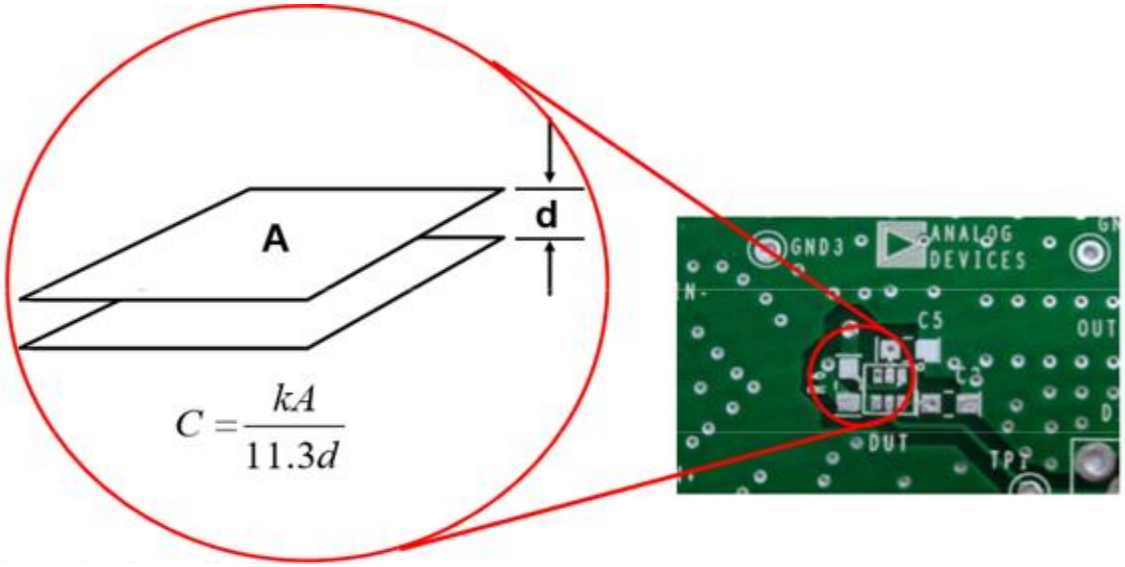


Figure 7:Trace/Pad capacitance in a PCB [28]

Where K=relative dielectric constant, A=trace/pad area in cm^2, d=spacing between plates in cm.

Trace Inductance

The trace inductance in a given PCB circuit is defined in equation (3.1) considering the geometrical structure of the trace as it is shown in figure 8.

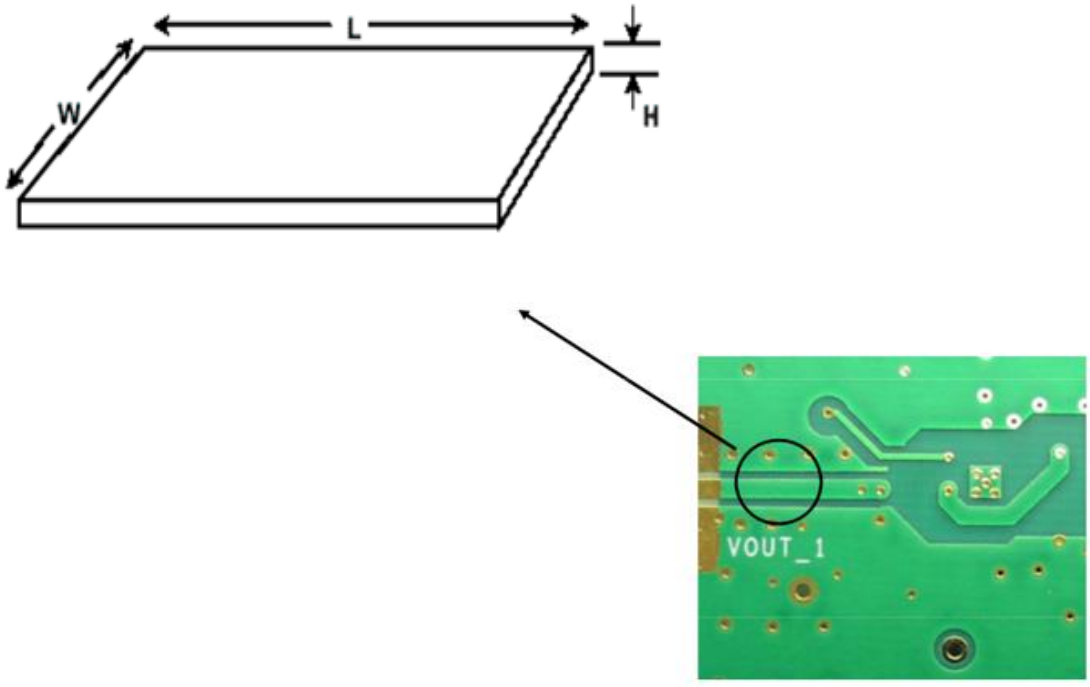


Figure 8:Trace Inductance [28]

$$sL = 0.0002L[\ell n\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5]\ \mu H \ldots\ldots\ldots\ldots\ldots\ (3.1)$$

Where sL=strip inductance and all dimensions are considered in millimeters. Minimization of inductance is done by using ground plane, shortening trace length and reducing the trace width.

Via Capacitance and Parasitics

The formula for calculating the capacitance and inductance of a via parasitics are indicated in equations (3.2) and (3.3).

$$L = 2h[\ell n\left(\frac{4h}{d}\right) + 1]nH \ldots\ldots\ldots\ldots\ldots\ (3.2)$$

Where L=inductance of the via, nH; H=length of via, cm; D=diameter of via, cm

$$C = \frac{0.55\varepsilon r TD1}{D2-D1}\ pF \ \ldots\ldots\ldots\ldots\ (3.3)$$

Where D1=diameter of pad surrounding via, cm; D2=diameter of clearance hole in the ground plane, cm; T= thickness of printed circuit board, cm; Ɛr= relative electric permeability of circuit board material; C= parasitic via capacitance, pF.

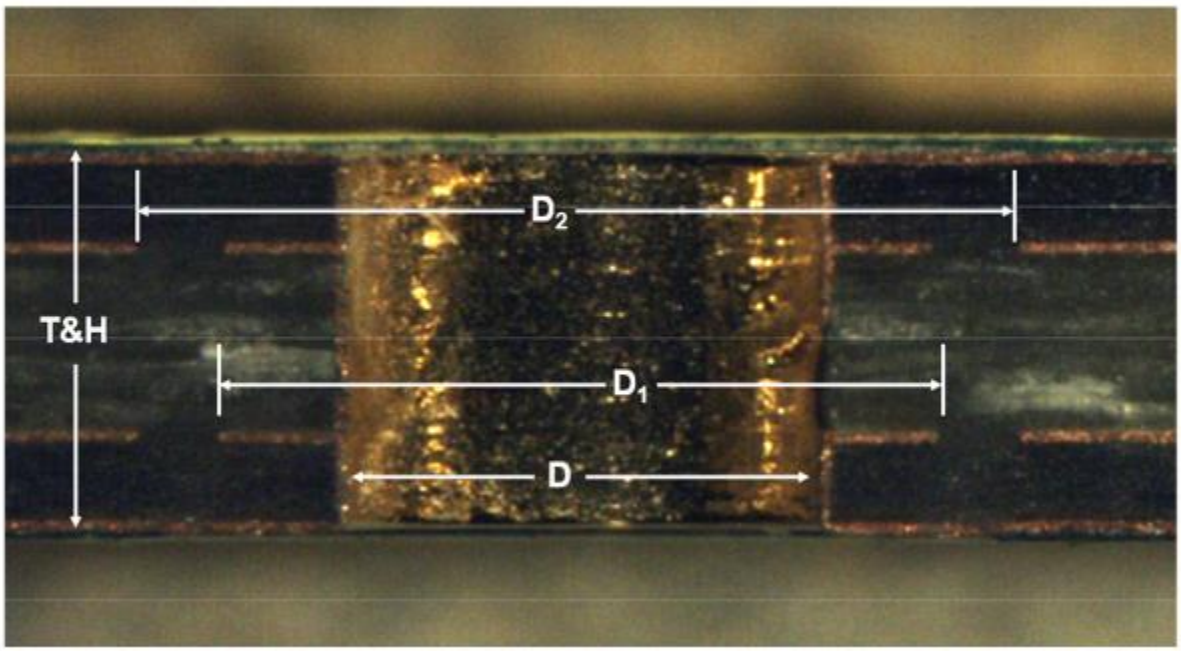


Figure 9:Via cross section [28]

Generally, there are three most important etching parameters which controls and affects the PCB during etching process. Three levels are considered for each controlling parameter, namely small, medium and large [29].

The influence of Etching parameter on undercut

In order to obtain the effect of the etching parameter on etching performance for each different level, the average response of each fixed parameter and level for each etching performance are summed up. The undercut increases with increase concentration. The affecting parameters for undercut are temperature, concentration and time. Out of these temperature and time are the most significant parameters on undercut.

Factor	Level 1	Level 2	Level 3	Max.- Min.
Temp. (^{o}c)	0.0560	0.1255	0.1688	0.1128
Conc. (gm/lit.)	0.0748	0.1023	0.1520	0.0772
Time (min.)	0.0760	0.0930	0.1800	0.1040
Mean value for the undercut = 0.1142				

Table 3:undercut in mm [29]

Average etching rate is considered for non-uniform etching [30]. In other words, not all the copper is removed evenly from the sample sheet at the same time as shown in figure 10. At this point, time is recorded and etching rate is calculated from the equation (3.4).

$$Average\ \ Etching\ Rate = \frac{Copper\ Thickness}{Total\ Etching\ Time} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.4)$$

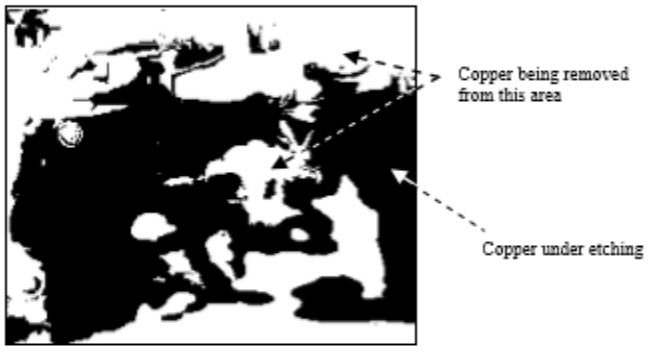


Figure 10:Typical circuit board under etching [30]

Copper Trace and Etching Tolerances

When copper is etched, the edge of the copper trace is neither a completely smooth nor a vertical wall. The roughness called the edge definition occurs because of mask resolution limitations, non-uniformity of the acid circulation, gas bubbling during etching and etc. The wall will have a slight angle to it because as the acid begins to work its way into the exposed copper a sidewall begins to form, which also is attacked by the acid. As it is shown in figure 11, the copper near the etch resist begins to be removed under the mask. This effect is called etch back or undercutting.

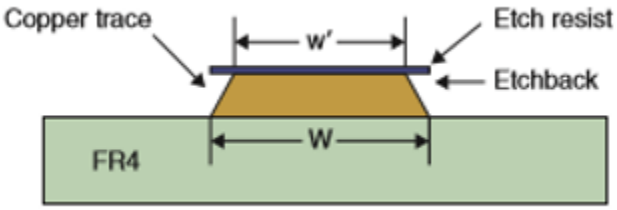


Figure 11:Result on finished trace width due to etch back [27]

3.5.2 Circuit Modelling

This section discusses the equivalent circuit or circuit model of various interconnection elements like traces, pads and holes.

Modeling Transmission Line

Interconnection traces in PCB can be modeled as microstrip and stripline type transmission line. These transmission lines are sometimes laid adjacent to each other and are considered as a single entity a multi-conductor transmission line.

Parasitics Modelling

Parasitics are those nasty little gremlins that creep into your PCB and cause destruction within a given circuit. They are the hidden stray capacitors and inductors that penetrate high-speed circuits.

They include inductors formed by package leads and excess trace lengths; pad-to-ground, pad-to-power-plane, and pad-to-trace capacitors; interactions with via, and many more possibilities.

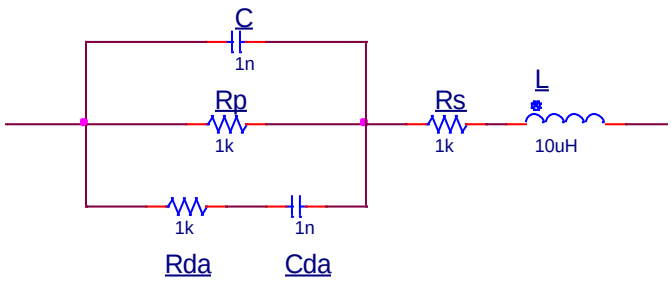


Figure 12:Capacitor parasitic model

Where C=Capacitor, R_P= insulation resistance, R_S=equivalent series resistance, L=series inductance of the leads and plates, R_{DA}=dielectric absorption, C_{DA}=dielectric absorption.

Resistor Parasitic Model

The equivalent circuit for parasitic resistor in PCB circuits is given in figure 13.

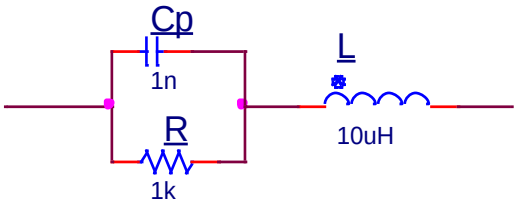


Figure 13:Resistor parasitic model

Where C_P=Parallel capacitance, L=equivalent series inductance, R=resistor

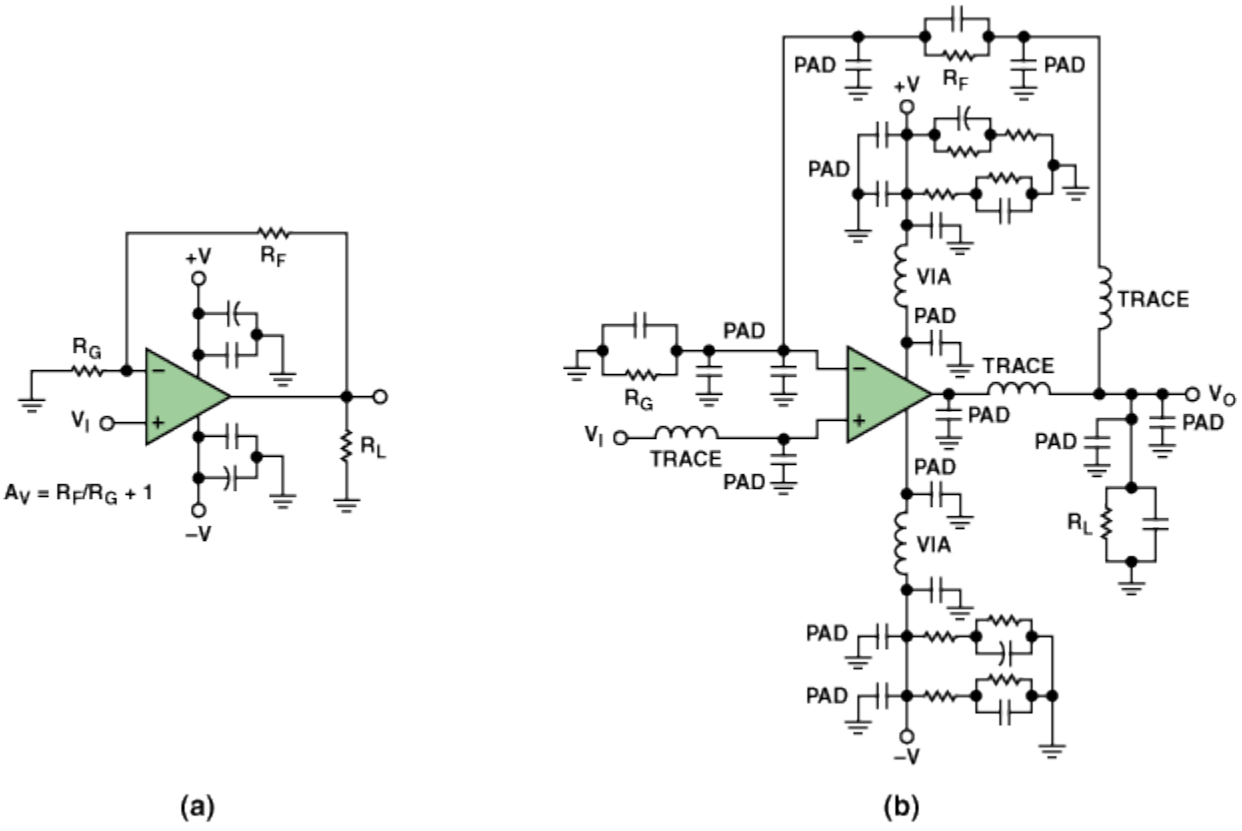


Figure 14:Opamp circuit [27]

(a) at low frequency (without parasitics) and (b) Op Amp at high frequency (parasitics taken into consideration)

Starting directly at the op amp's power-supply pins; the capacitor with the lowest value and smallest physical size should be placed on the same side of the board as the op amp—and as close to the amplifier as possible. The ground side of the capacitor should be connected into the ground plane with minimal lead- or trace length.

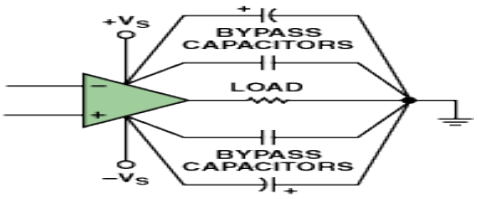


Figure 15: parallel capacitor rails to ground- bypassing [27]

In high-speed circuits, small picofarad is enough to influence the circuit. For example, 1 pF of additional stray parasitic capacitance presented at the inverting input can cause almost 2 dB of peaking in the frequency domain. If enough capacitance is present, it can cause instability and oscillations.

Drilling Inaccuracies and Affecting parameters

The most important drilling control parameters are spindle speed, feed rate, drilling tool size on material removal rate (MRR), surface roughness, dimensional accuracy and burr [31]. The surface roughness is mostly influenced by spindle speed and feed rate. As the spindle and feed rate increases, the surface roughness will decrease. The tool diameter gives less influence on the value of surface roughness. The value of MRR is decreased when the tool diameter, spindle speed and feedrate decreases. As drilling tool diameter, feedrate and spindle speed increase the dimensional accuracy of drilled hole decreases.

In hole registration accuracy, the entry material allows the drill tool to maintain its original location and minimize deflection [32].

Hole positioning error

When several layers are drilled simultaneously for an efficient process, misalignment of holes from the ideal drilling coordinates occurs, particularly in the bottom layer. The hole positioning error for the bottom layer was greater than that for the top layer for all tool diameters, and the deviation increased with depth. This is because of the increasing trend of the tip deflection in accordance with length from the shank. The factors that result in misalignment of drilled holes must be identified to reduce the hole positioning error. One of the factors is spindle run-out with vibration can cause inaccuracy of the drilling point at high rotational speeds [32].

Method of measuring positioning errors for drilled holes

One way of measuring positioning errors in drilling is through an imaging of the drilled holes. An image of each layer is obtained using the optical microscope after a drilling operation. The image is processed using MATLAB to define the horizontal line of each hole by scanning the contours of the holes. Finally, the hole centers are determined from the vertical centers of the horizontal lines and were compared with the ideal drilling coordinates. For many circuit designers, plated

through holes (PTHs) form pathways, from one circuit plane to another, also known as via holes, can provide a path from a conductive layer to a ground plane, from one signal plane to another, and from high-current or power planes to signal planes [33].

The main reason for performing drilling experiments that continue until bit breakage occurs is to determine the various combinations of parameters leading to breakage [34]. The parameters affecting for burr formation are drill point geometry and point angle, drill bit material hardness, cutting speed and spindle speed.

Effects of Drilling inaccuracies

Plated through-holes and vias typically have lands on all layers even when there is no connection to it on that layer; these are called non-functional lands [36]. Non-functional lands should be used on internal layers when possible, but non-functional lands are not required on every layer if the board is over 10 layers thick, and they are not required on plane layers.

Overlapping of lands causes capacitive coupling between the pad and the plane, which can alter the characteristic impedance of the trace and could cause crosstalk problems at high frequencies.

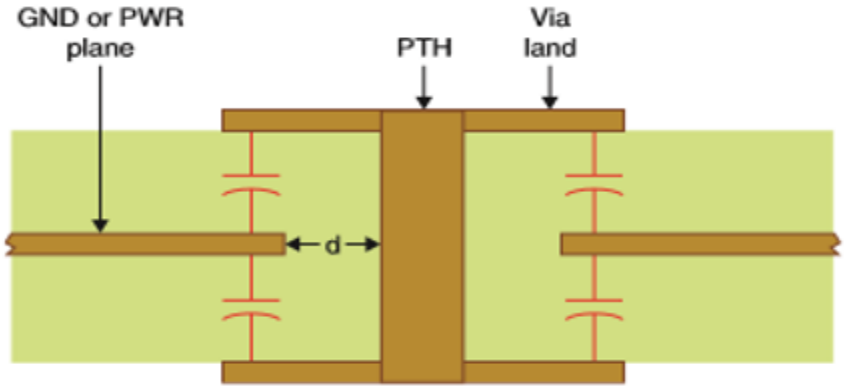


Figure 16:PTH or via with oversized lands overlapping plane [36]

Achievement of good surface quality remains a concern during micro drilling of printed circuit board (PCB) [37]. The current work utilizes finite element analysis-based simulation of deformation and stresses to explain the various parameters of hole quality such as diameter, delamination factor and burr thickness. Results indicated that stresses play a vital role in influencing hole qualities of PCB. Increase in feed rate resulted in reduction in hole diameter, whereas delamination factor and mean burr thickness increased with feed.

PCB failure and failure analysis in digital circuits

As logic gates are the building blocks of digital circuits, a circuit potentially contains many logic gates and stuck at faults. From a given logic fault models for an n input and one output logic circuits, potentially there exist a total of 2n+2 stuck at faults. The total number of manufacturing faults in such a circuit can be in the range from thousands to hundreds of thousands. Detecting any potential manufacturing fault in complex digital circuits is very difficult. The solution is to find a test vector to detect a high percentage of stuck at faults in a circuit.

Fault coverage is the percentages of the total number of potential manufacturing faults in some digital circuits detected [38]. Testing helps know what faults has occurred. The search for an appropriate fault coverage requires an analytical approach to a set of related variables. These variables include defect level, fault coverage, and yield. Defect level is an indicator of the percentage of circuits with defects not detected and shipped with the product. Then the defect level

$$\mathbf{DL=1-Y^{(1-T)}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.5)$$

Where, **Y** represents the yield, **T** is fault coverage for a given test that detects only **m** out of **k** stuck at faults. From equation (3.5) for improving the defect level, a very high fault coverage like more than 95% is required.

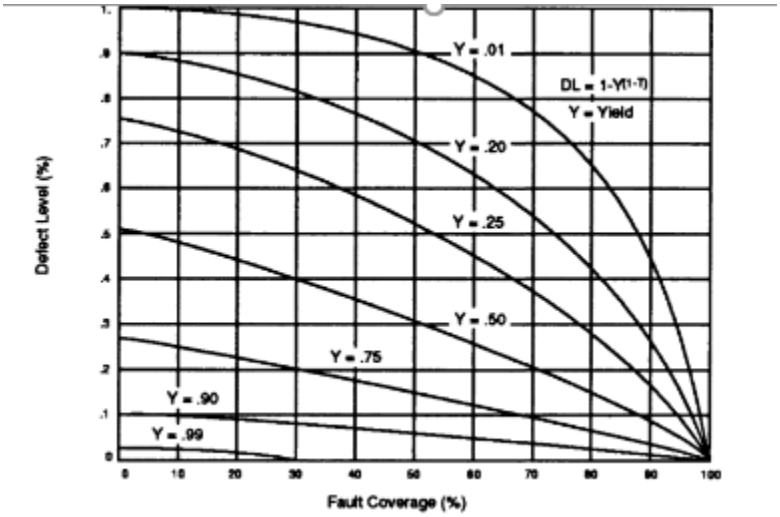


Figure 17:Defect level as a function of fault coverage and yield [38]

Circuit defect level and board failure rate

As all digital circuits are eventually mounted on a PCB before shipment as part of the product, it is important to understand the impact of the defect level of digital circuits on the failure rates for PCB containing many circuits. We can form a relationship between circuit defect levels and board failure rates. Assuming there are K number of circuits on the board and DL is the defect level. The probability of a circuit being good is 1-DL. The probability of all circuits being good on the board is given in equation (3.6).

$Pc=(1-DL)^k$ …….. (3.6)

The probability for the board to contain at least one bad circuit is given in equation (3.7).

Pa=1-Pc ……. (3.7)

Determining and Setting Appropriate PCB Parameters

In order to accurately simulate reflections, crosstalk and other signal integrity characteristics certain PCB parameters need to be determined [38]. These parameters are required for each of the boards to be correlated, as the parameters can change from board to board during the manufacturing of the PCBs. Generally, each of these parameters can be controlled within a certain tolerance by the PCB manufacturer. These are referred to as controlled impedance PCBs.

The PCB controlling parameters include Dielectric constant of the isolation material, Dielectric thickness of the isolation material, Track width of an etch, Track thickness (usually controlled by controlling the amount of conductor, for example 1 Oz of copper is 1.44 MILs).

PCB Stack up planning/bonding press

The configuration of the PCB stackup depends on many factors, but to avoid a possible debacle, all signal layers should be adjacent to and closely coupled to a reference plane, creating a clear return path and eliminating broadside crosstalk [39]. Good interplane capacitance to reduce inductance at high frequencies.

High speed signals should be routed between the planes to reduce radiation. The substrate should be symmetrical with an even number of layers, which prevents the PCB from warping during manufacture and reflow. The stack up should accommodate a number of different technologies.

3.6 Implementation Methodology

In this section the method of analyzing the effects of inaccuracies of PCB manufacturing processes on the level of malfunctioning of circuits are discussed. The type of application software used for simulation as well as the procedures followed to study the effects are described.

3.6.1 Software Requirement

The Software selected to study the effects of manufacturing inaccuracies is OrCAD PCB designer. Among other softwares, OrCAD is the appropriate one for this purpose because of the features it has starting from schematic capture to layout design. Schematic development, PSpice simulation and layout design are the main task of the OrCAD software in this research.

OrCAD capture is a PCB schematic designer tool. The following is the screen shot of OrCAD Capture which is applied for designing the schematic circuit selected for studying the effects.

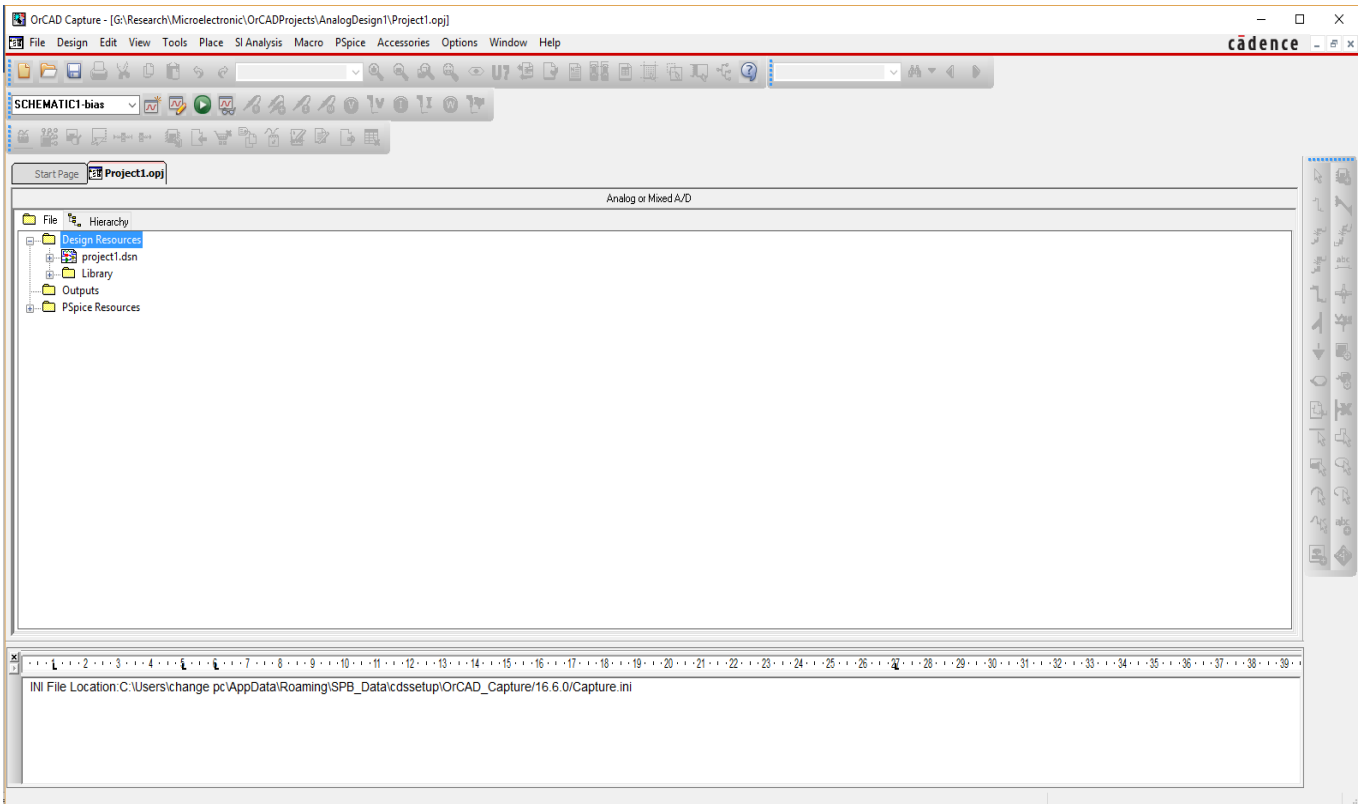


Figure 18:Screen shot of OrCAD Capture

OrCAD PSpice is an analog and digital simulator, PSpice simulates a captured circuit so that its performance can be investigated.

OrCAD PSpice technology is seamlessly integrated with OrCAD Capture which is one of the most widely used schematic design solutions allowing to easily cross-probe between the schematic design and simulation plot results and measurements [40]. This integration also allows to use the same schematic for both simulation exploration and PCB layout, reducing rework and errors

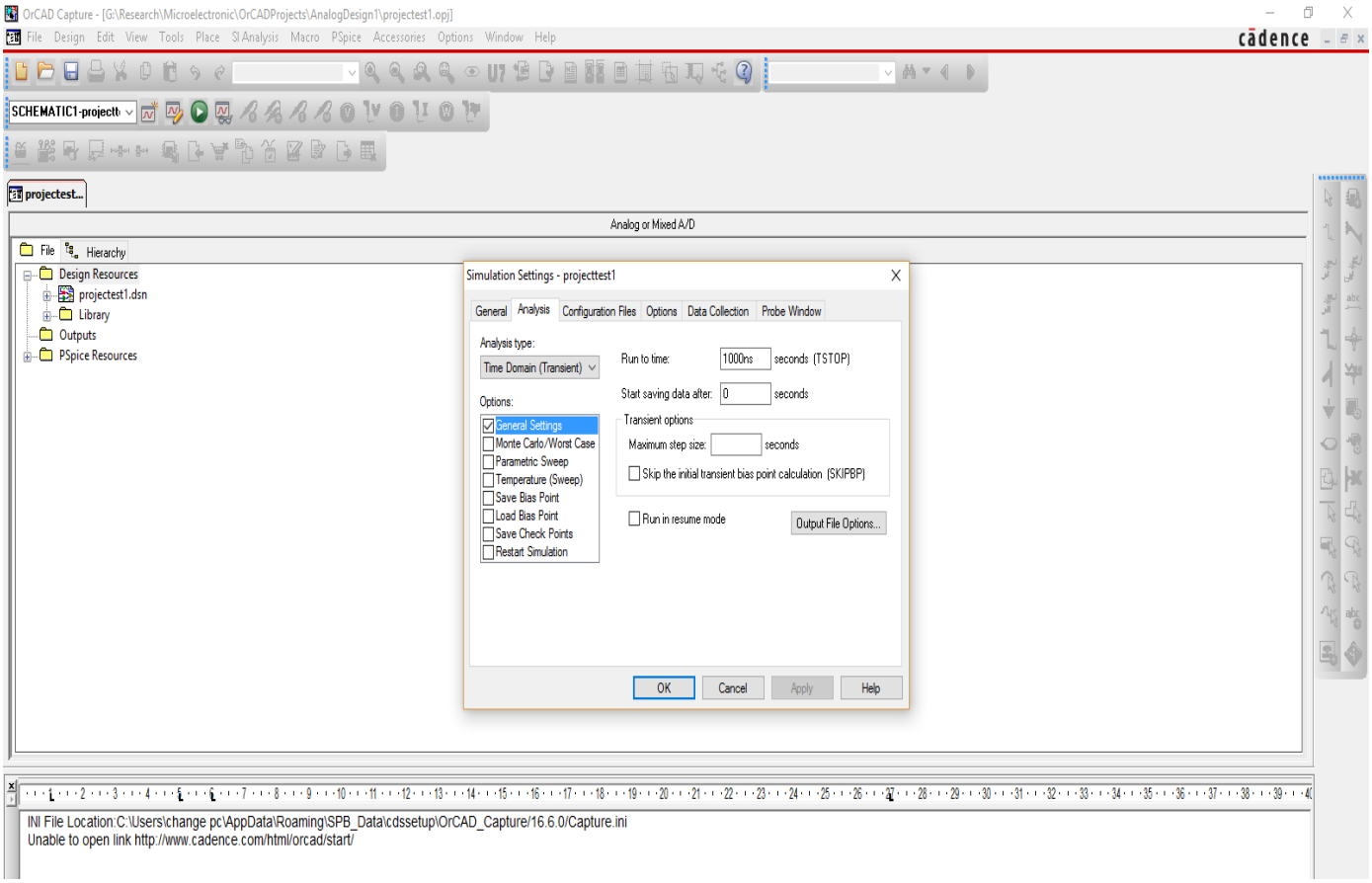


Figure 19:screen shoot of PSpice schematic simulator

PCB Editor is the application for laying out a printed circuit board. It includes an automatic router that works out the arrangement of tracks needed to connect your components on the PCB. The output is a set of files that can be sent to a manufacturer.

The main task in preparing the design or layout is to associate a footprint with each component. The footprint shows the physical outline of the components including the copper pads to which the pins are soldered.

The simplest way of creating a PCB is first to set up an empty PCB, then to add components and connections to the board.

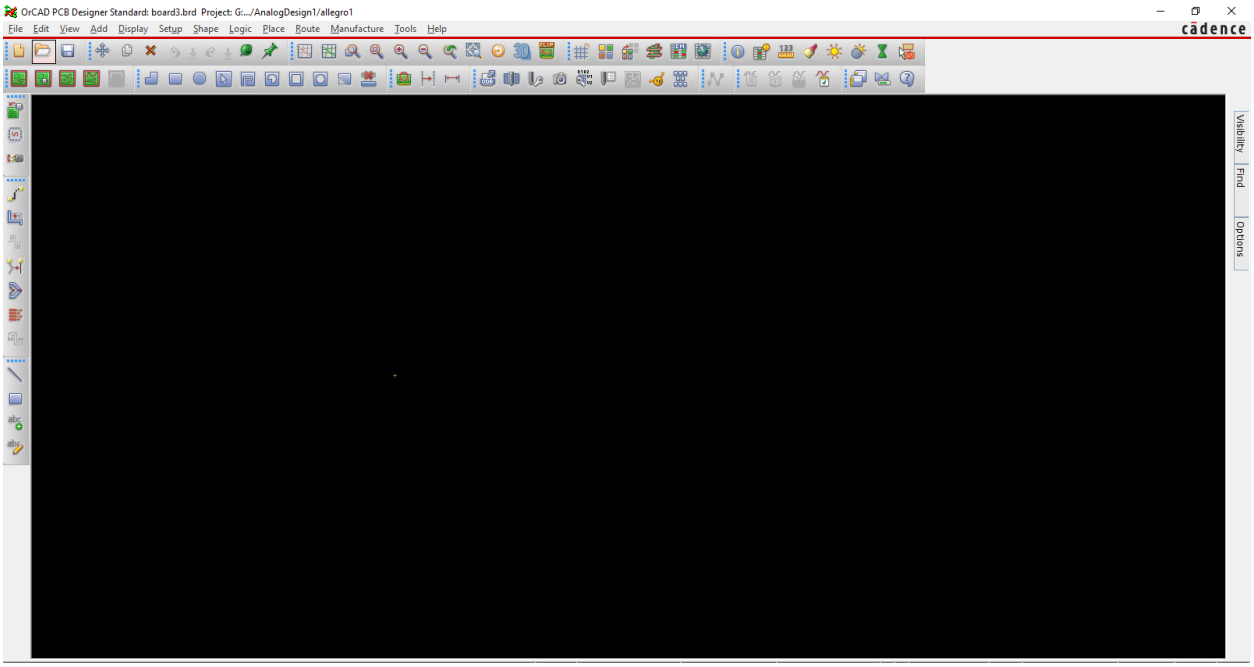


Figure 20:screen shoot of OrCAD PCB Editor (layout designer)

3.6.2 Implementation Procedures

The major PCB manufacturing processes namely, Photolithography, etching, and drilling are considered for analyzing and discussing the effects of manufacturing inaccuracies. The procedures followed to study the circuit effects of different scenario is given as follows.

1. In the first step, appropriate circuit which is a two stage BJT amplifier is selected.
2. The normal schematic circuit is captured on OrCAD PCB Capture.
3. Simulation of the given circuits is done on OrCAD PSpice.
4. A four-layer PCB layout is routed for the given schematic and the possible manufacturing inaccuracy scenarios are indicated on the circuit layout.
5. Equivalent circuit model for the given inaccurate scenario is developed.
6. Schematic capture incorporating circuit model for the inaccuracy scenario is done for the selected circuits.
7. Difference in circuit performance and any circuit malfunctioning is observed.

Chapter Four

Simulation Results and Analysis

4.1 Introduction

In this chapter, the simulations of selected circuits considering the different manufacturing inaccuracies are done. Firstly, the effects due to photolithography inaccuracy are simulated and analyzed. Secondly, the effects of etching and drilling are discussed. The effects considered are open circuit, short circuit, under etch, over etching, missing hole, inappropriate drilling, misalignment and so on.

4.2 Selection of circuits

Three types of circuits are selected for the purpose of simulating and analyzing the effects of PCB manufacturing inaccuracies on circuits. The circuits are Two stage BJT amplifier, 4-bit ADC and Opamp based amplifier.

4.2.1 Two stage BJT amplifier

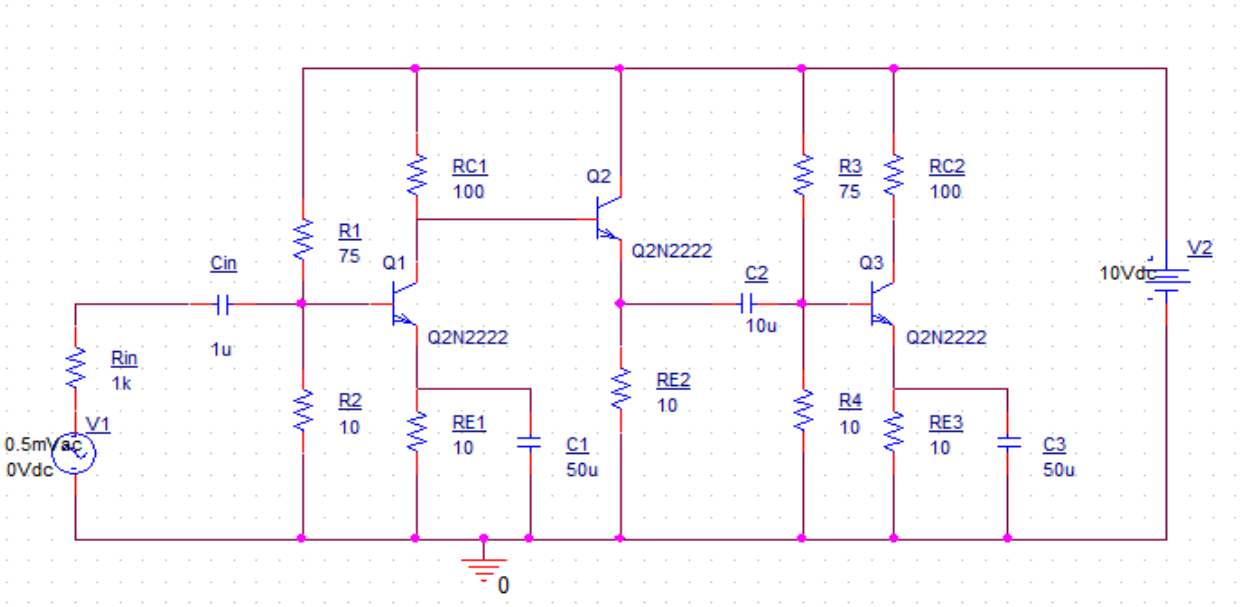


Figure 21:Two stage BJT amplifier, circuit1

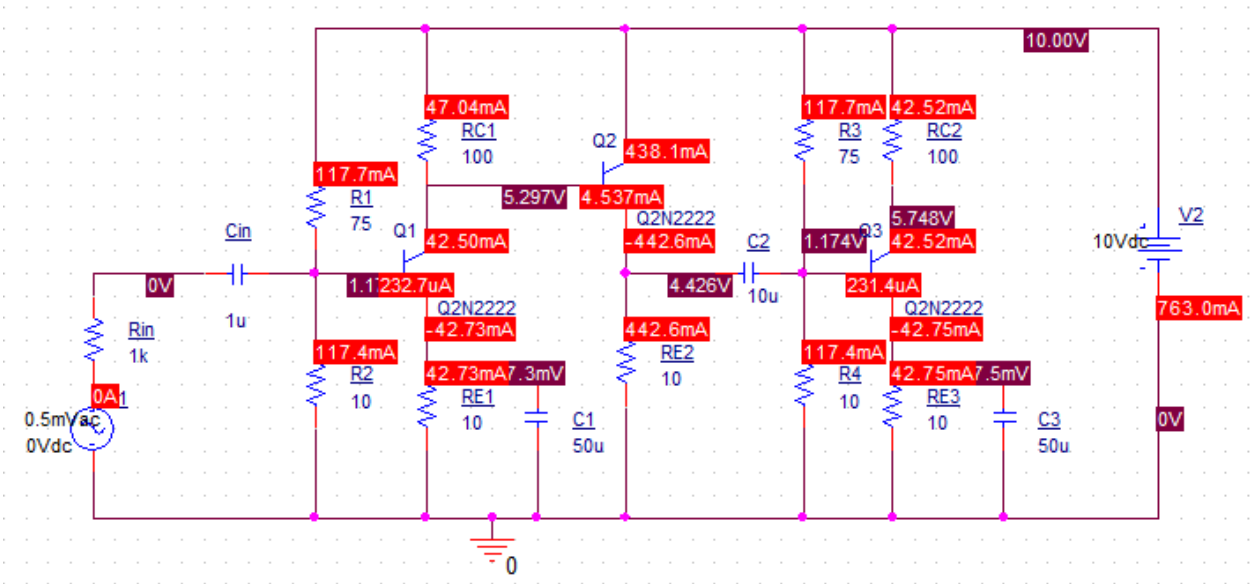


Figure 22:Two stage BJT amplifier biasing points

Four Layer PCB Routing

The electrical connections depicted by the ratsnest must now be replaced by copper tracks on the PCB. This procedure is called routing the board. Tracks should be drawn on the bottom of the board with the components placed on the top. The wires from the components pass through the holes in the pads and are soldered to the tracks on the bottom of the board. The ground and power planes are placed on the second and third layers.

It is important to model electrical properties of interconnections between nodes by their equivalent circuits and integrate them into the system simulation to make accurate predictions of system performance. The choice of electrical model to simulate the behavior of interconnect must consider the parameters such as Physical nature or electrical properties of the interconnect, Bandwidth or rise time and source impedance of signals of interest, Interconnect's actual time delay, Complexity and accuracy of the model.

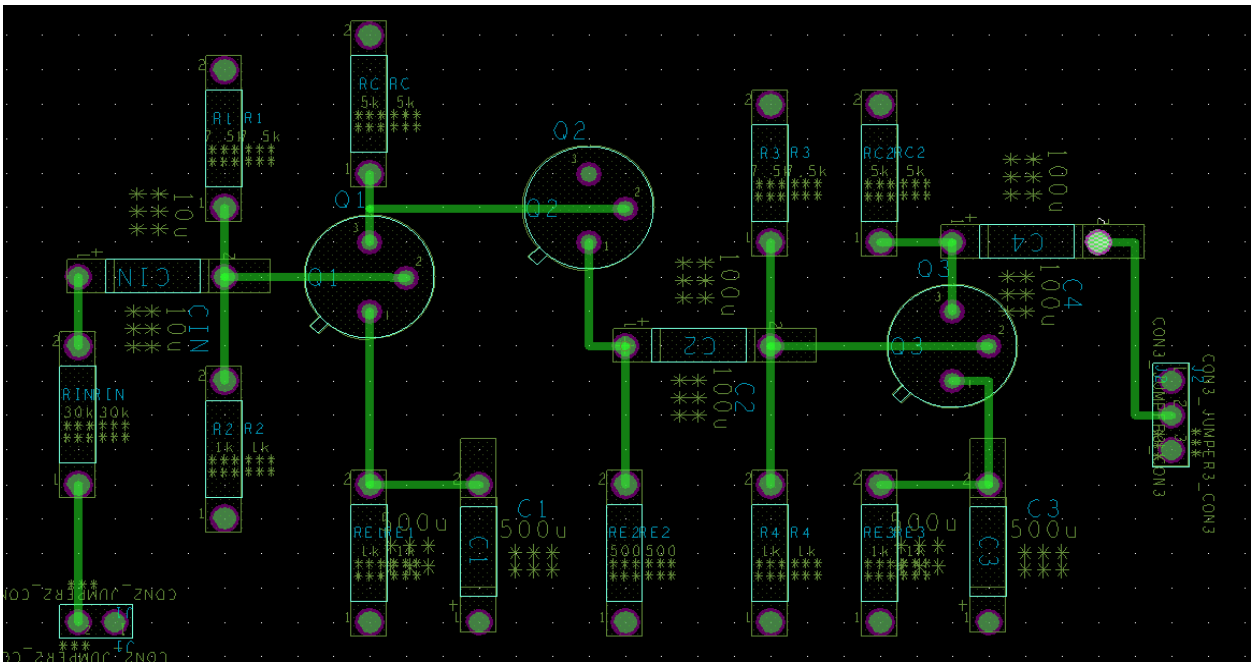


Figure 23:Layout for the two stage BJT amplifier

Effect levels of Etching inaccuracies

During etching process, the anomalies occurring on bare PCB could be largely classified in two categories: one is excessive copper and missing copper. The incomplete etching process leaves unwanted conductive materials and forms defects like Short-circuit, extra hole, protrusion, island and small space. Excessive etching leads to open circuit and thin pattern on PCB. In addition, some other defects may exist on bare PCB, i.e. missing holes, scratch, and cracks.

Figure 24 shows some of the common etching inaccuracy scenarios. By taking one scenario at a time, the corresponding possible effects are simulated and discussed. In the first step the simple etching problems are considered and their effects observed. In the next stage, more serious problems and some critical scenarios are considered and discussed.

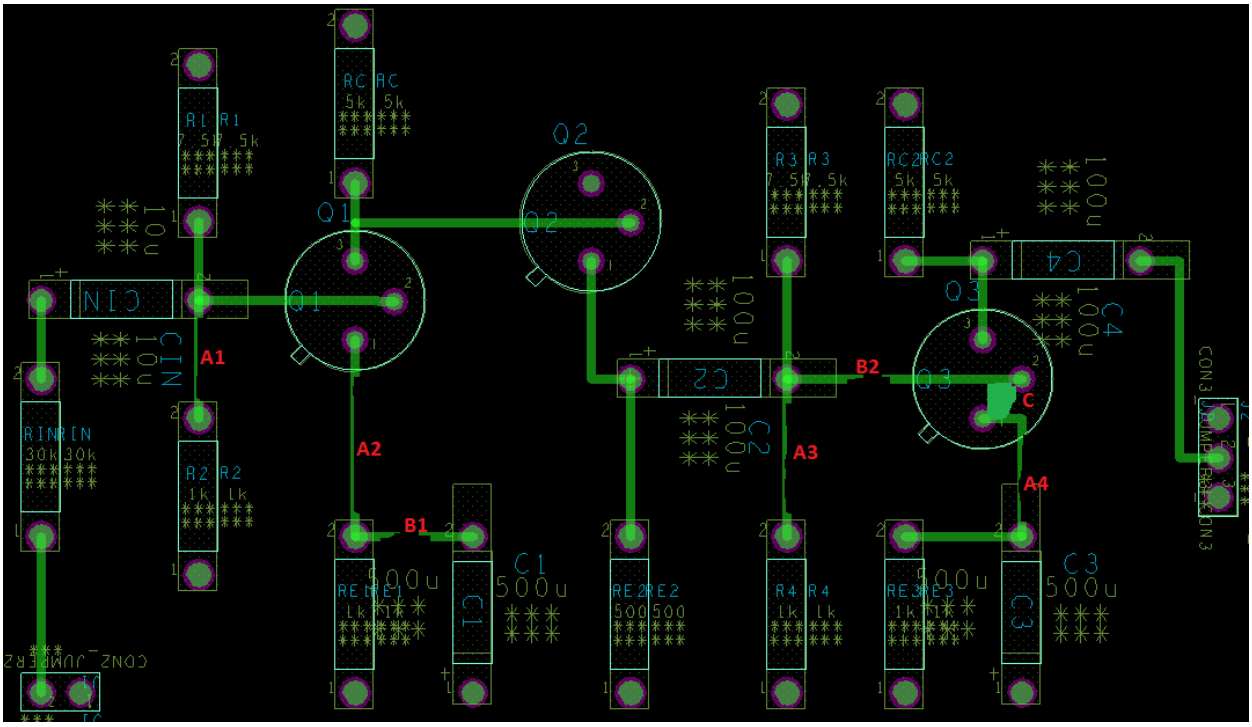


Figure 24: different inaccuracy scenarios

Scenario A1: Over etching

From figure 24, the general name for inaccuracy cases A1, A2, and A3 is over etching. The over etching scenario indicated by A1 is discussed in the following paragraphs. The other over etching scenario indicated by A2 and A3 are also discussed in a similar manner.

The above scenario is modelled into a circuit to see the effect on circuit performance and malfunctioning. For perfect etching case, the resistance of the tracks is assumed to be negligible. However, it has a considerable resistance value for the over etching scenario above. A formula for calculating the sheet resistance R of a copper trace, given the length Z, the width X, and the thickness Y is given by:

$$\boldsymbol{R = \frac{\rho Z}{XY}} \quad \text{..... (4.1)}$$

Where $\rho = 1.724 \times 10^{-6} \Omega cm$ is the resistivity of the copper.

The length of the trace with incorrect etching indicated with A1 is 300mil. The width of the traces as per the design is 25mil, (1000mil =1inch, or 393.7mil=1cm).

If the thickness of the trace becomes 5mil, the additional resistance due to over etching is given as follows.

Y=0.0036cm,

Z=300mil=0.762cm,

X=5mil=0.0127cm

$$RA1 = \frac{\rho Z}{XY} = \frac{1.724x10-6\Omega cm*0.762cm}{0.0127cm*0.0036cm} = 0.028733\Omega$$

For trace width X=1mil, R_{A1}=0.14367Ω and for X=25mil, R_{A1}=0.00575Ω which is almost negligible for the normal trace width. However, when the width of the trace roughly changes from 25mil to 1 mil the trace resistance increases and becomes significant. Finally, R_{A1} will be added in series to R2. The effect is to increase the resistive impedance as it is shown in figure 25.

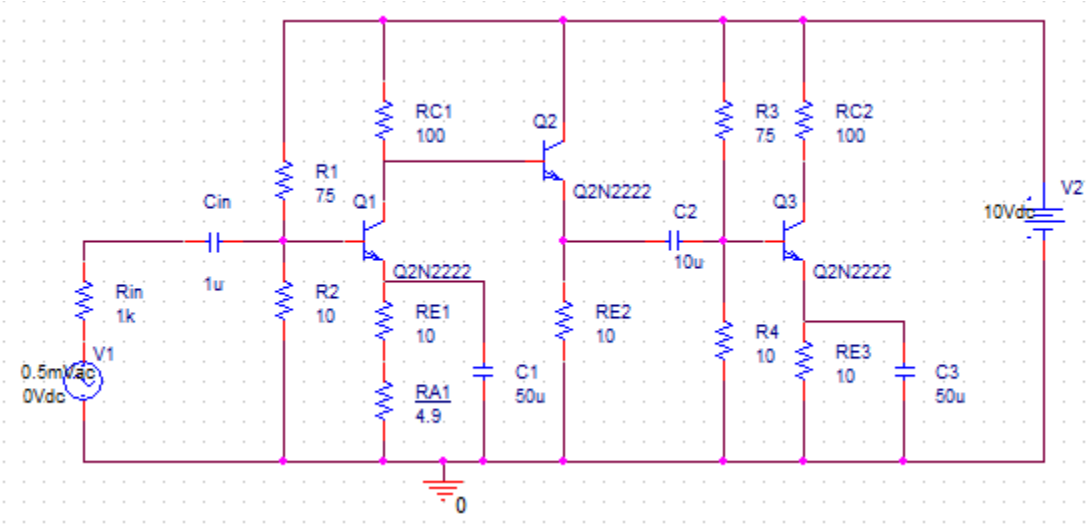


Figure 25: Equivalent circuit for scenario A1

Figure 26 depicts the frequency response of the circuit for different levels of over etching scenarios represented by A1 with the effect indicated by resistance R_{A1}. It shows that the gain is decreasing as R_{A1} keep increasing.

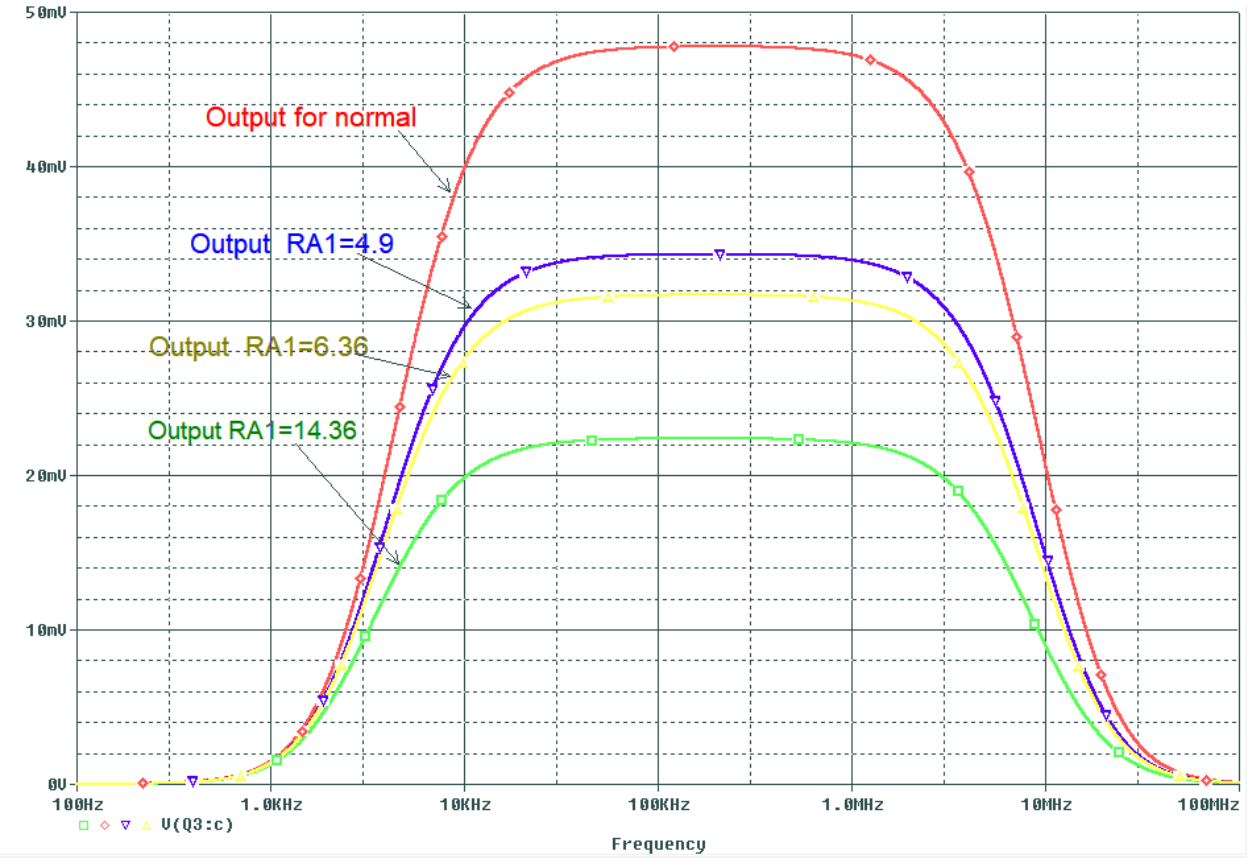


Figure 26: Frequency response for over etching scenario for different levels of RA1

Inaccurate etching can cause undesired signal output which is a decreasing effect. But the idea is that the effect of inaccuracy is an obstacle to getting the desired signal output. It makes the circuit fluctuate and deviate from the functionality it is designed for.

Scenario 2: No input to Transistor Q3

The input side is floating(open) due to over etching. Consequently, the equivalent circuit is depicted in figure 27.

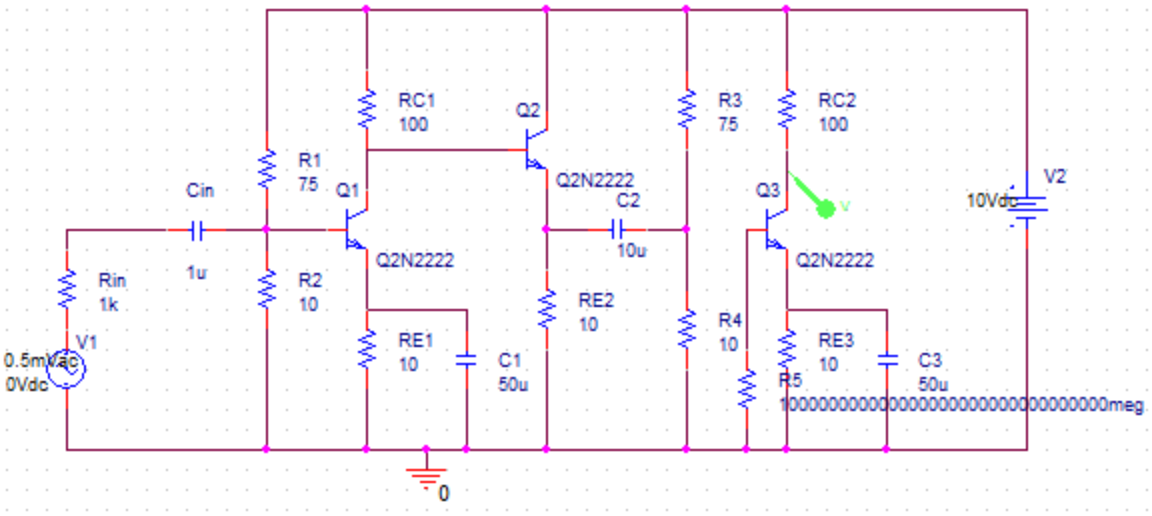


Figure 27:Equivalent circuit for scenario 2

The output for the the circuit given in figure 28 is shown in figure 29. It shows that the effect of scenario 2 is fatal and the ouput is zero.

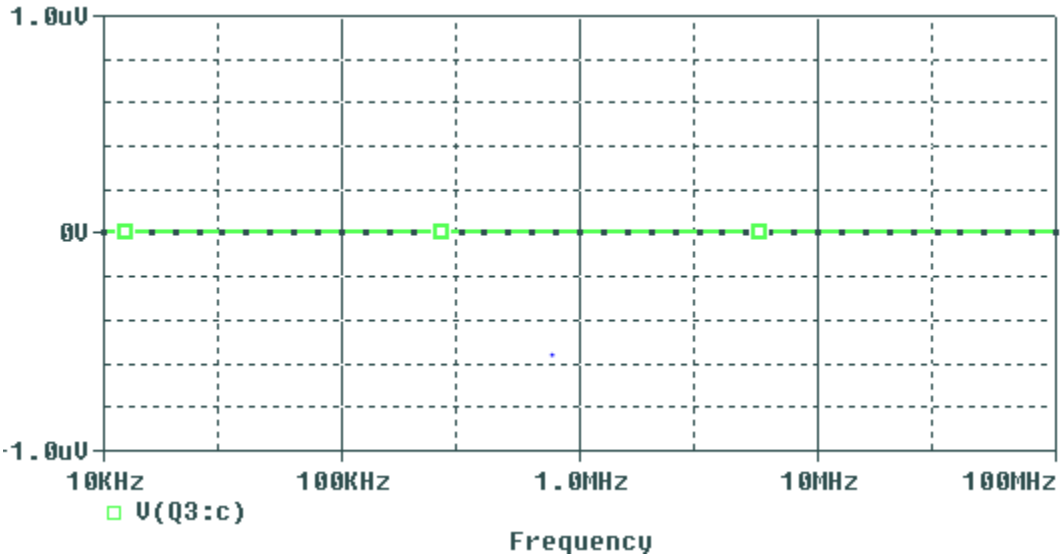


Figure 28:Frequency response for scenario2

Scenario 3: Emitter and Collector shorted in transistor Q3

The scenario is depicted in the circuit layout which is shown in figure 29.

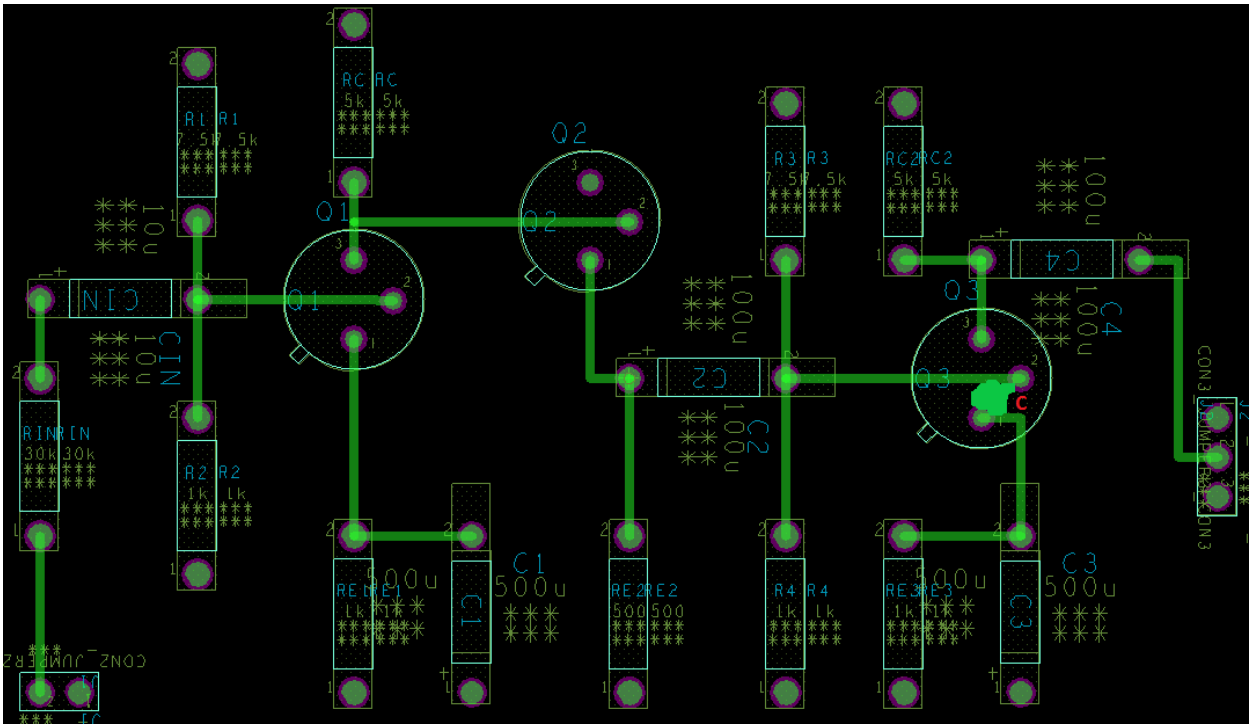


Figure 29: Illustration of scenario 3

The equivalent schematic for the scenario 3 is shown in figure 30.

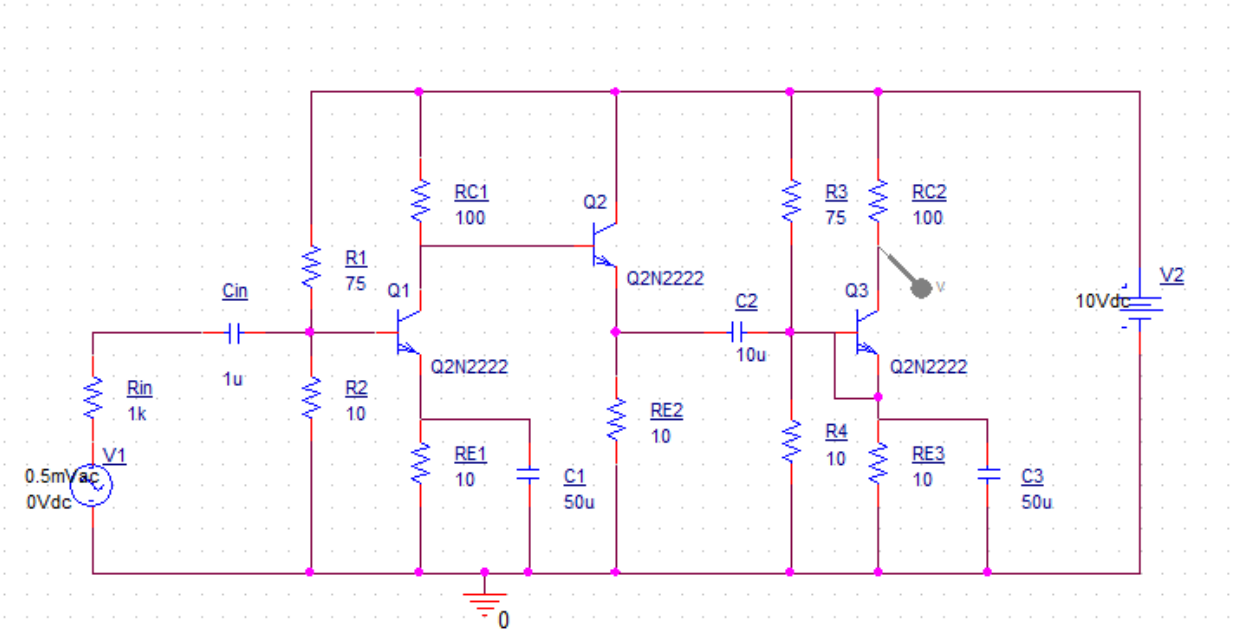


Figure 30: Equivalent schematic for scenario 3

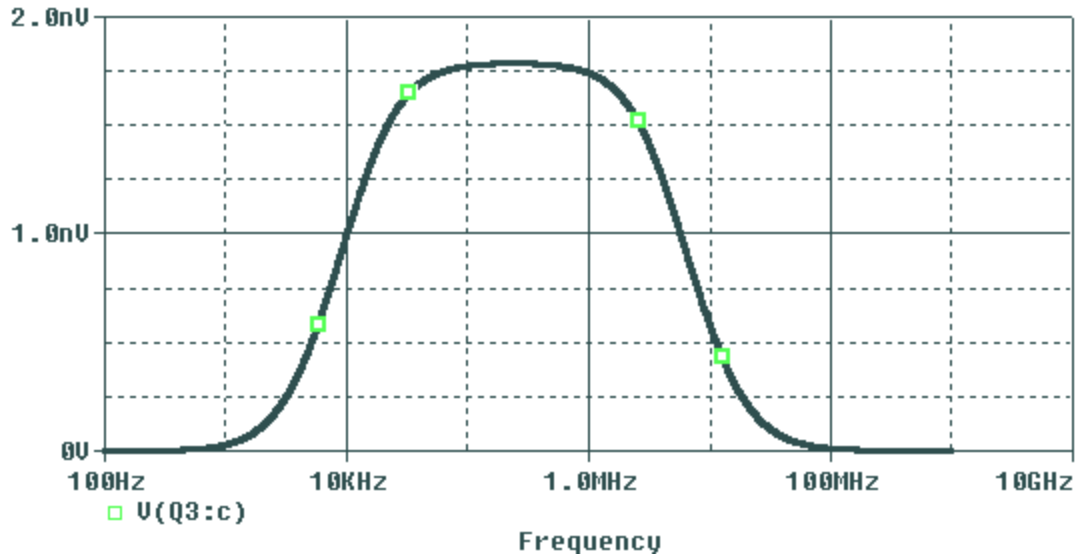


Figure 31: Frequency response for scenario 3

Capacitive effects

When the gap between two parallel traces is smaller than the standard spacing that it should be between traces, capacitive impedance will be introduced across the traces and results in cross talk and unstable output.

The capacitance between two parallel traces can be calculated using equation (4.2).

$$C = \frac{KA}{11.3d} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4.2)$$

Where A is area of a trace in cm^2, d is distance between traces and K is relative dielectric constant.

If the normal spacing between traces, d1=250MIL and is changed to d2=125MIL, then we can calculate the effective capacitance using equation (4.2).

K=4.8, d1 =250MIL=0.635cm

thickness =0.0036c, length=250MIL=0.635cm

A=0.635cm*0.0036

$A=0.002286cm^2$

C_1= (4.8*0.002286)/(11.3*0.635)

C_1=0.015292/7.1755

C_1=0.002131=21.31uF

For d2=125MIL=0.3175cm

C_2= (4.8*0.002286)/(11.3*0.3175)=30.584uF

Hence, the net effective capacitance which is denoted as C_4 in figure 33 is the difference between C_1 and C_2.

$C_4 = C_2 - C_1 = 30.584uF - 21.31uF = 9.274uF$

The equivalent circuit after introducing the net capacitance C_4 is shown in figure 32.

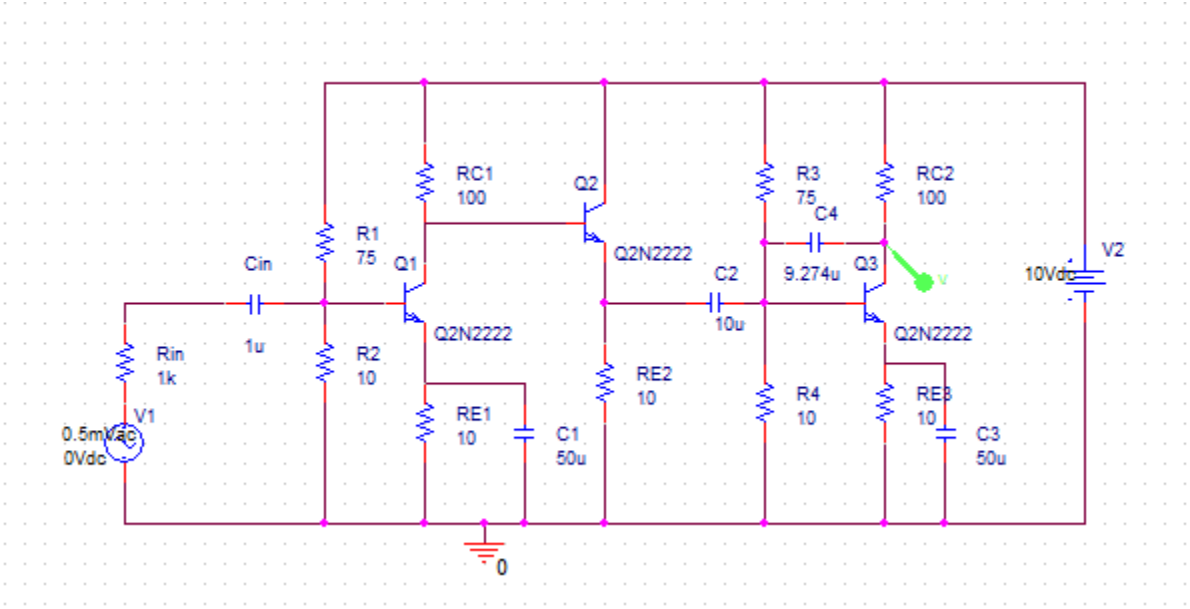


Figure 32: Equivalent circuit with capacitive effect

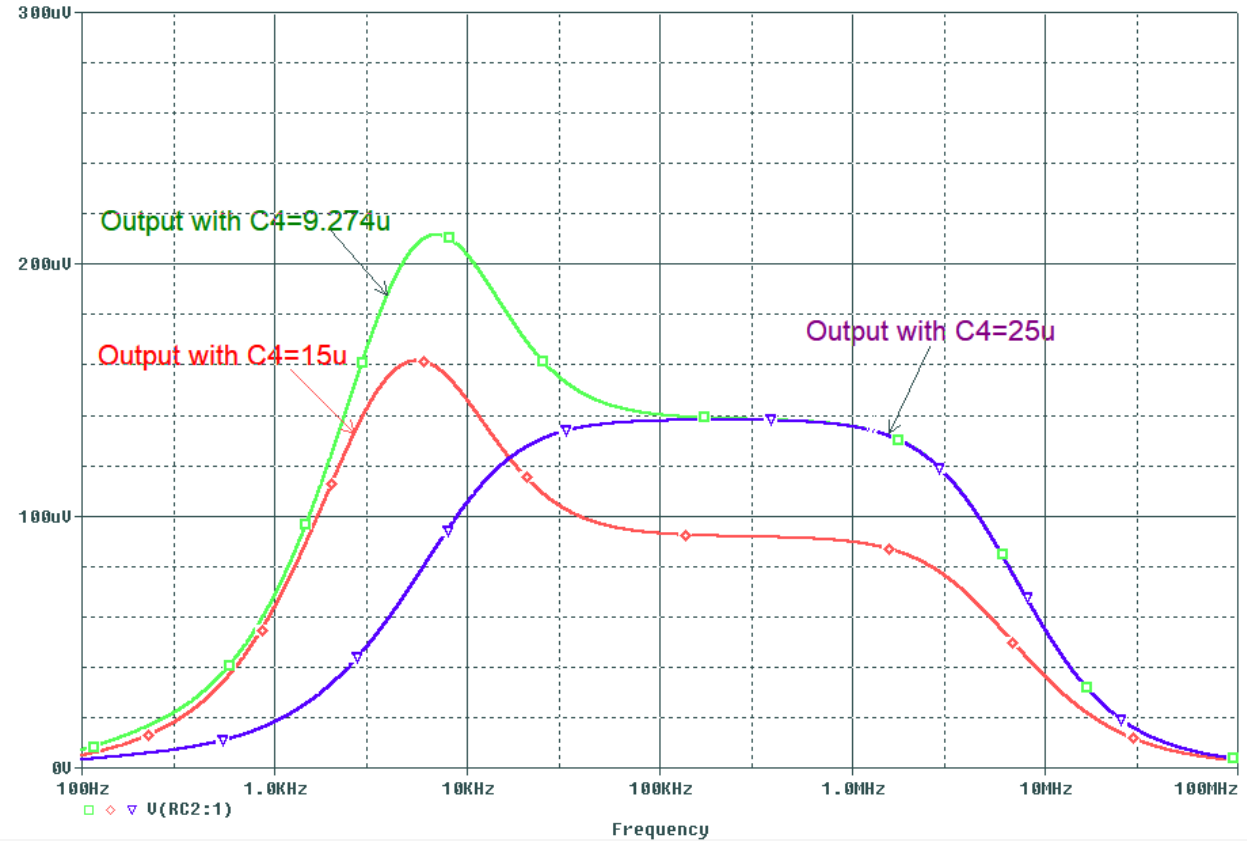


Figure 33: Frequency response for different capacitance values

Figure 33 shows the simulation output of the circuit depicted in figure 32 by considering different capacitive effects. As we can see from the simulation output, cross talk or unstable output occurs over the frequency on which the expected output should be stable.

When the capacitive impedance effect is 25uF, the output drops from around 50mV to 140uV and the output waveform looks like the waveform of the normal circuit. On the other hand, at lower capacitance values the output becomes unstable and gives a waveform with a different nature.

Capacitive and Resistive effects

In this section, the capacitive effects due to wrong spacing between traces as well as resistive effects due to over etching are considered and the equivalent circuit is depicted in figure 34.

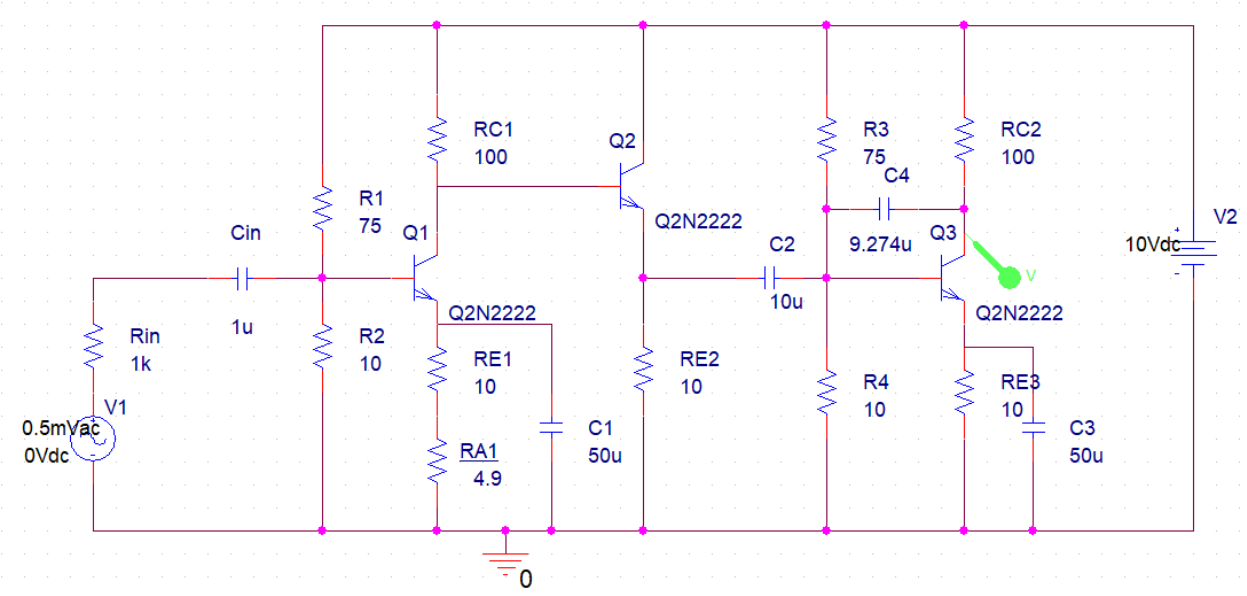


Figure 34: Equivalent circuit for capacitive and resistive effects

The simulation output for the circuit in figure 34 is shown in figure 35. As it can be understood from the output waveforms , the combined resitive and capacitive effects are shown. The output waveform results in instability and oscillations.

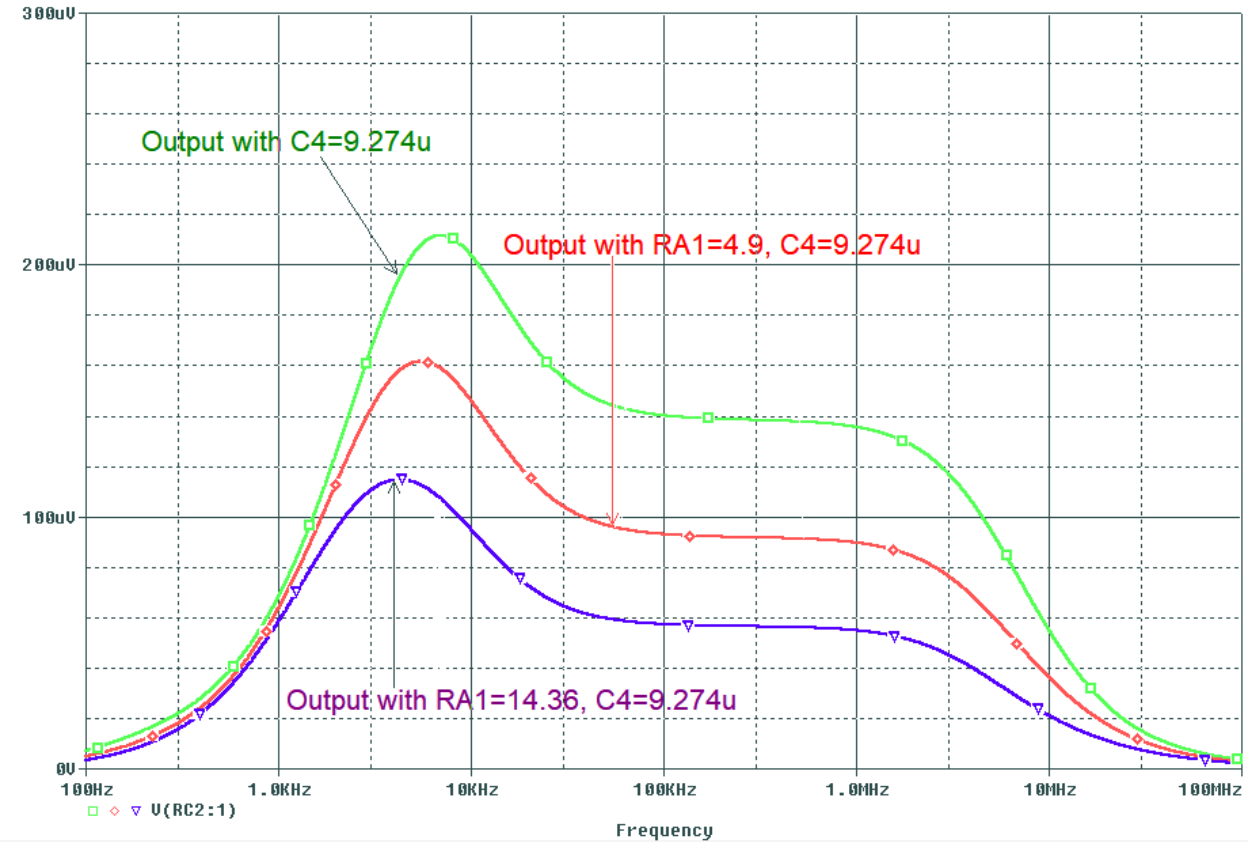


Figure 35:Frequency response for combined capacitive and resistive effects

4.2.2 Four-bit Analog to Digital Convertor (ADC)

Figure 36 shows the use of four comparators (Opamp without feedback) for building 4-bit ADC. The output of the comparators corresponds to digital word. When the input rises above Vin1, the comparator will switch to high output voltage causing the corresponding LED to light up, indicating 0001. When the input is above Vin3, all comparators will switch to output voltage high, indicating 1111.

All comparators work in parallel. This converter is very fast for this reason it is called a flash converter.

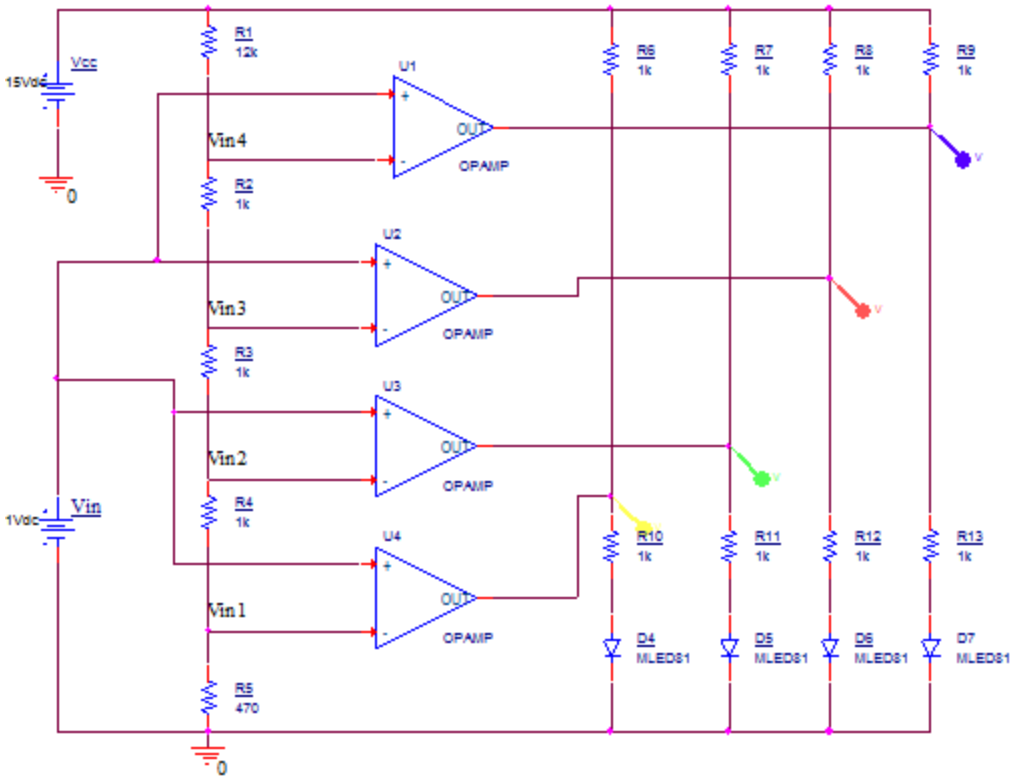


Figure 36:4-bit ADC implementation

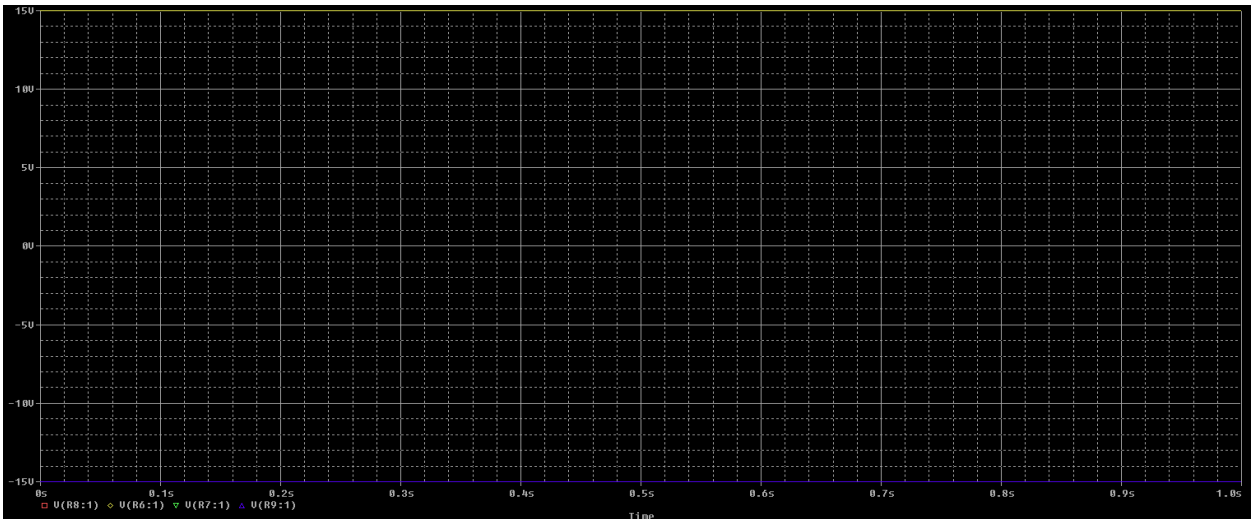


Figure 37: Output signal for the ADC

The PCB layout and possible inaccuracy scenarios of the 4-bit ADC circuit is illustrated in figure 38. For 1V input, the output is 0001 for the normal circuit.

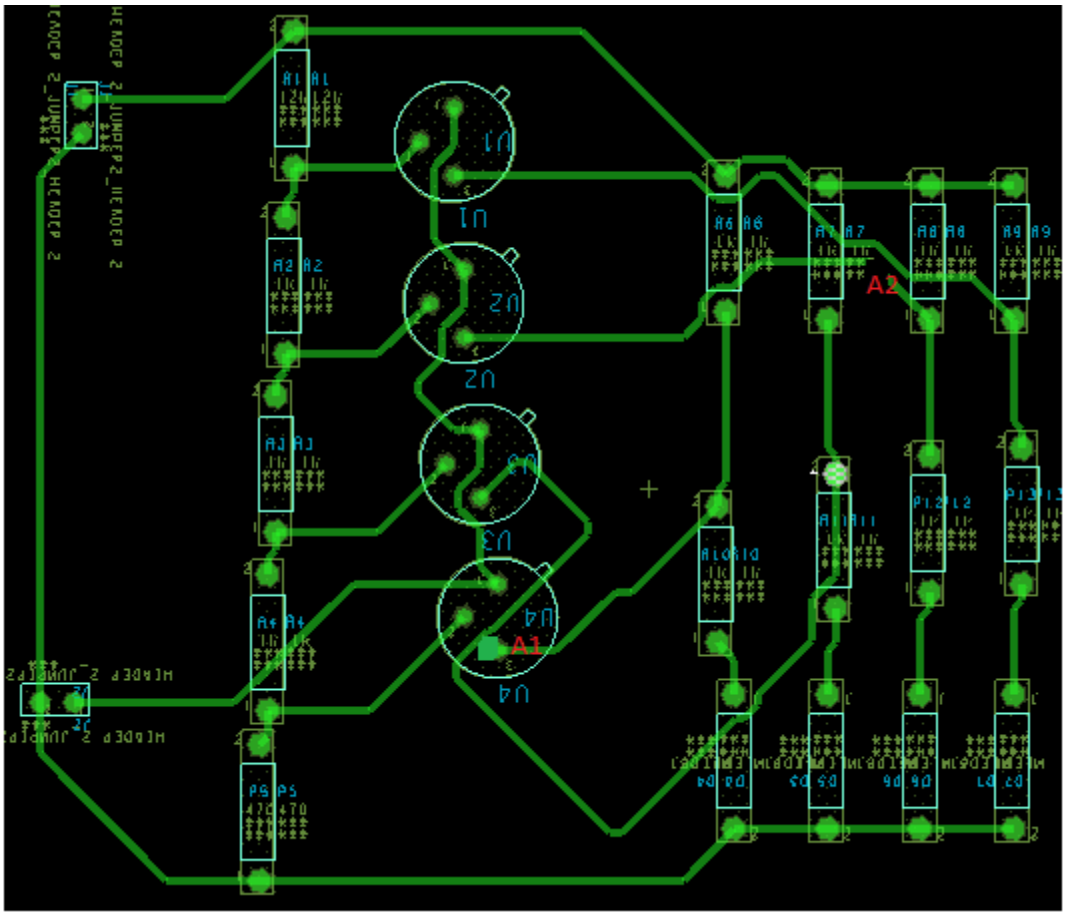


Figure 38: Layout after possible manufacturing defects are introduced

From figure 38, we have one short circuit and one open circuit defects represented by A1 and A2 respectively. For the short-circuiting scenario indicated with A1, the equivalent circuit represented in figure 39.

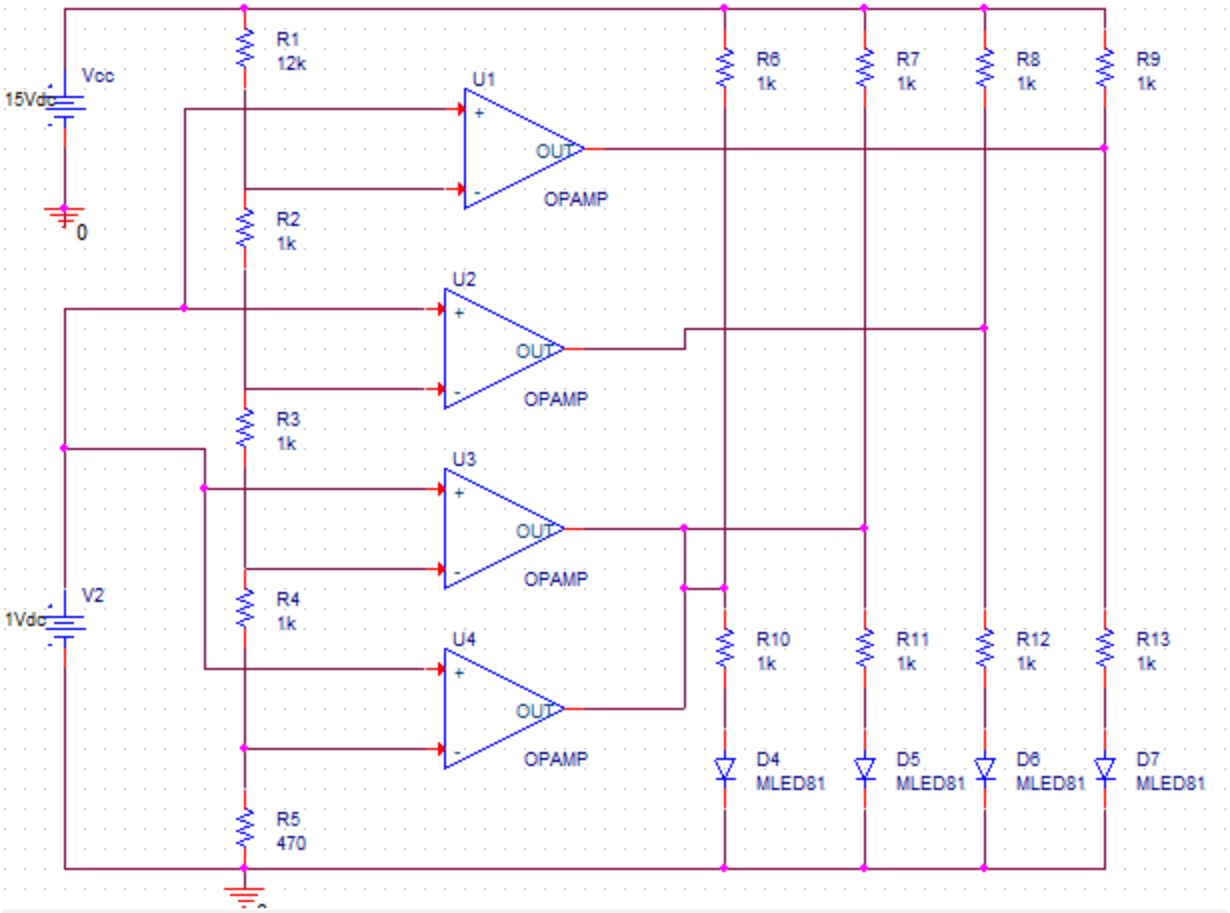


Figure 39:Equivalent Schematic with short circuit scenario

The PSpice simulator displays an error saying "ERROR(ORPSIM-15143): Voltage source and/or inductor loop involving E_U3." This means no output signal is displayed. As a result, the circuit is dead or malfunctioned.

Similarly, the equivalent circuit for the open circuit scenario depicted with A2 is given in figure 40.

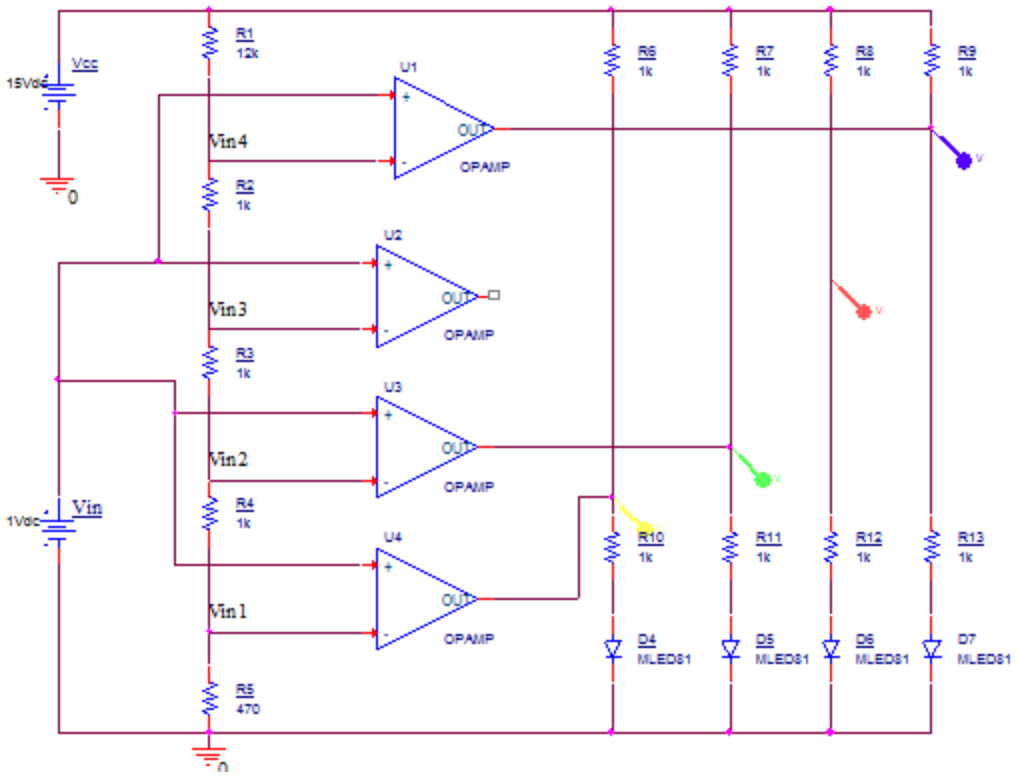


Figure 40: Equivalent circuit for open circuit scenario

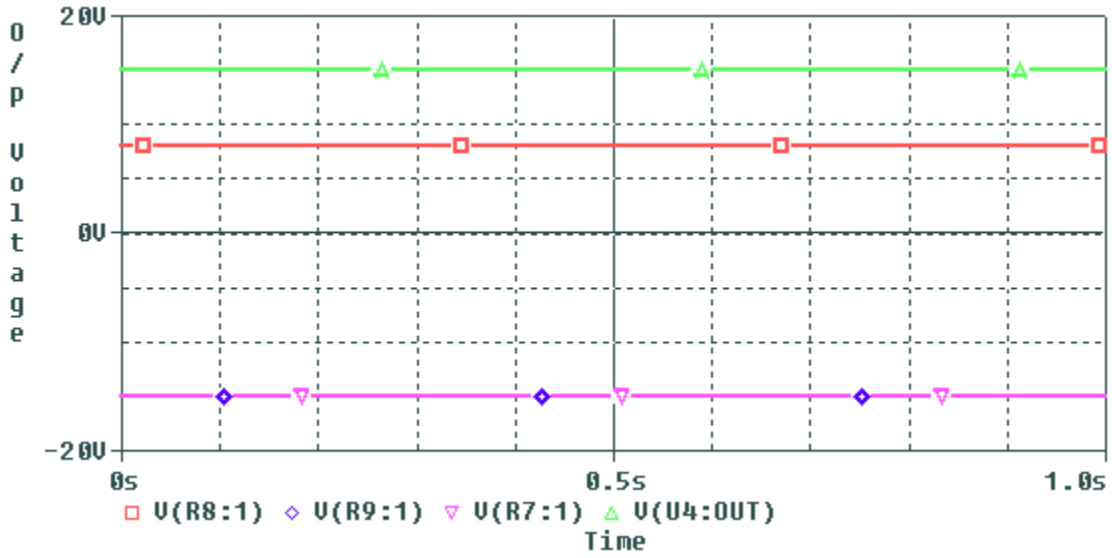


Figure 41: The output signal for scenario A2

As it is illustrated in figure 41, the output for 1V input is 0101 which is a wrong output due to pen circuit.

4.2.3 Amplifier with Opamp

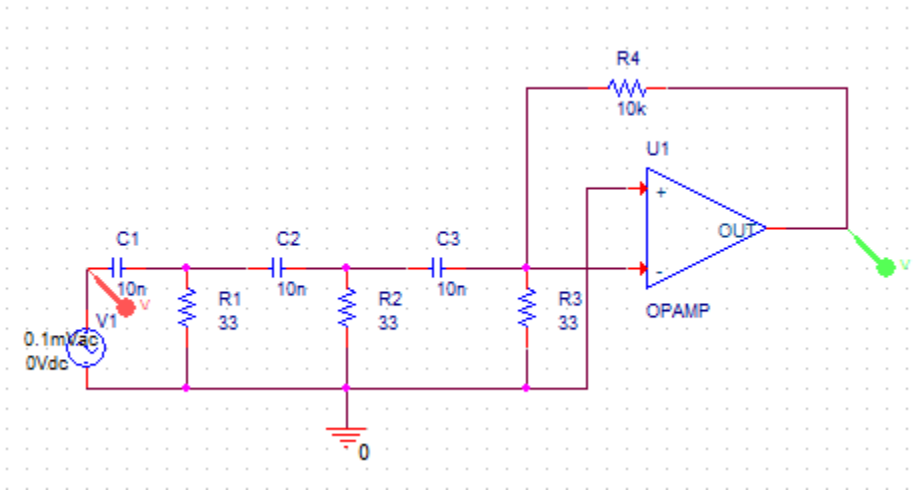


Figure 42: Schematic Capture for Amplifier with Opamp

We can produce layout for the above circuit in a similar way. The point of interest here is to demonstrate the effects of inaccuracies with regards to the amounts of the capacitance and resistance and the effects on the output or performance of the circuit.

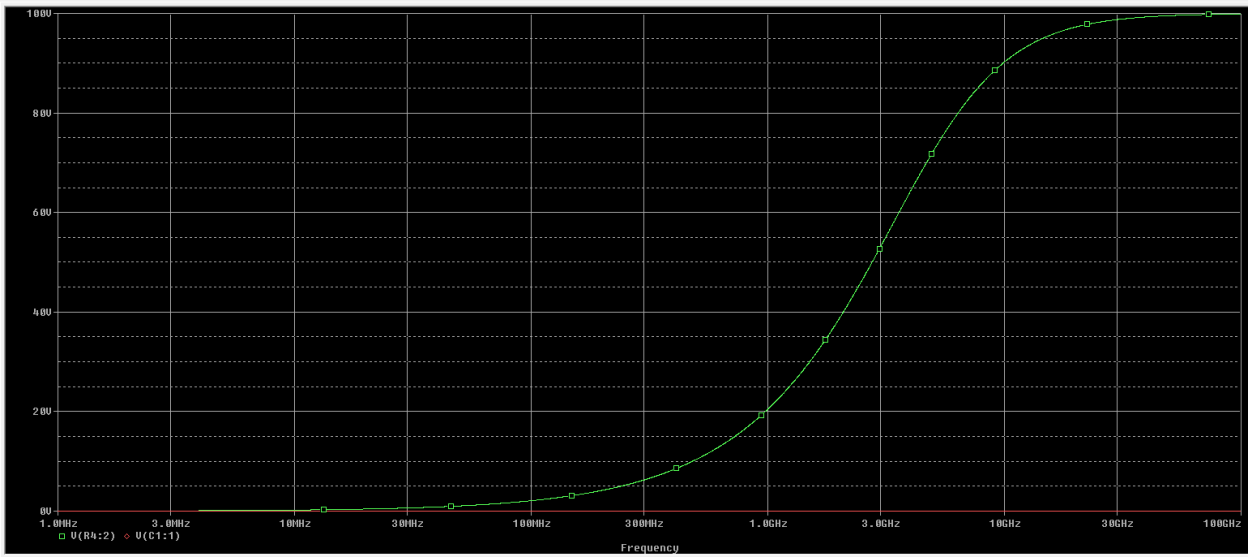


Figure 43: Frequency response for the amplifier

Effect levels of drilling inaccuracies

The costs caused by tool failures are considerably higher. The poor removal of chips in deep drilling of small diameter is often the cause of tool breakage and poor-quality surface.

It is interesting to know that there was an increase in burr thickness with progressive drilling of micro holes. This phenomenon might be described through gradual wear owing to indentation of chisel edge and adhesion of work material on chisel and cutting edges.

In PCB, several layers are stacked together and drilled simultaneously to improve the drilling quality. If there is a misalignment of the drilled holes on the top and bottom layers, there will be a degradation of PCB performance. The potential causes of drilling errors are spindle run out, severe dent, and adjacent holes machined a priori.

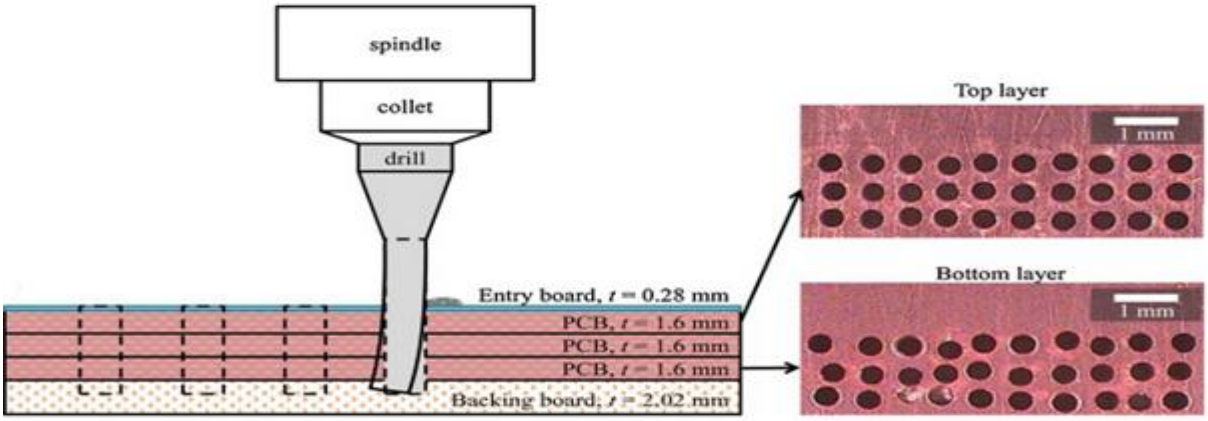


Figure 44: Drilling inaccuracy [37]

As it can be seen from figure 45, the drilling is done inappropriately that the top and bottom layers have different number and orientations of holes. In this case, the top and bottom layers may not be correctly connected. In other words, components on the top will not be connected fully and some of their terminals may be left floating. In addition, the spacing among some of the drilled holes in the bottom layer is below the standard and hence may cause short circuiting of nearby holes because of very small spacing between holes. The effect is poor circuit performance or malfunctioning depending on the level of drilling errors.

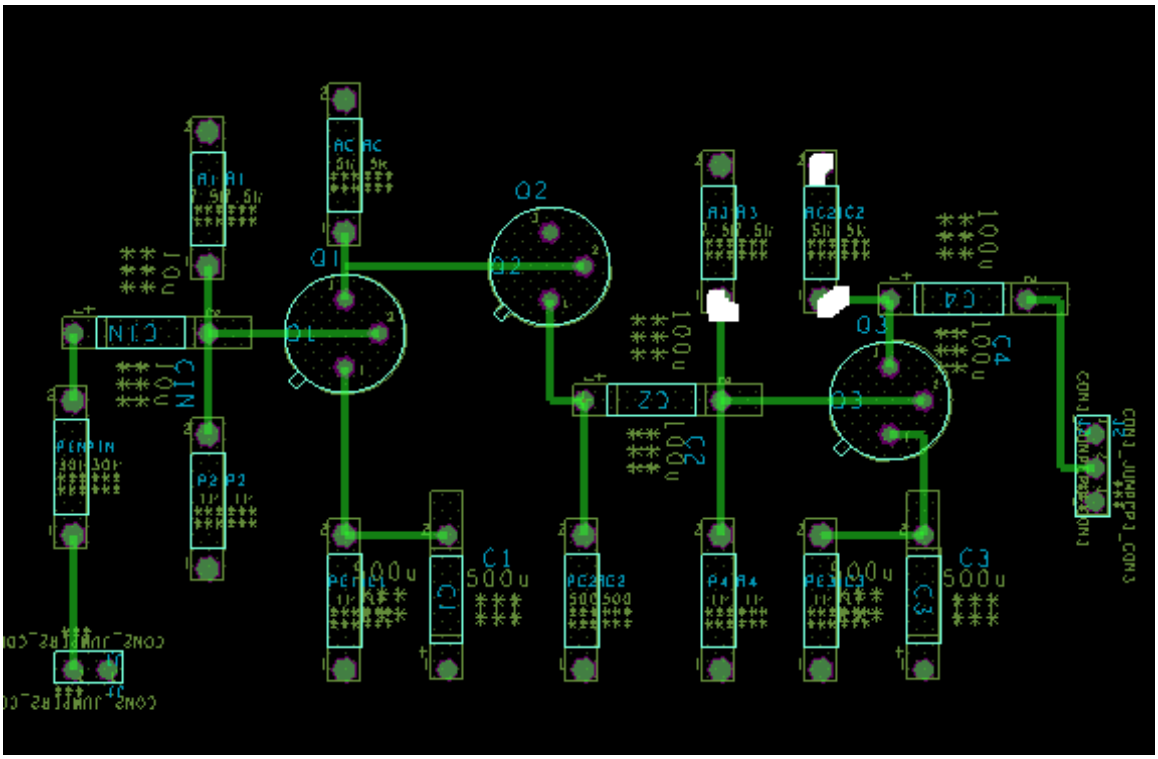


Figure 45:Components R3 and RC2 failed to get connected to bottom layer

The equivalent schematic circuit for the above scenario is given as follows.

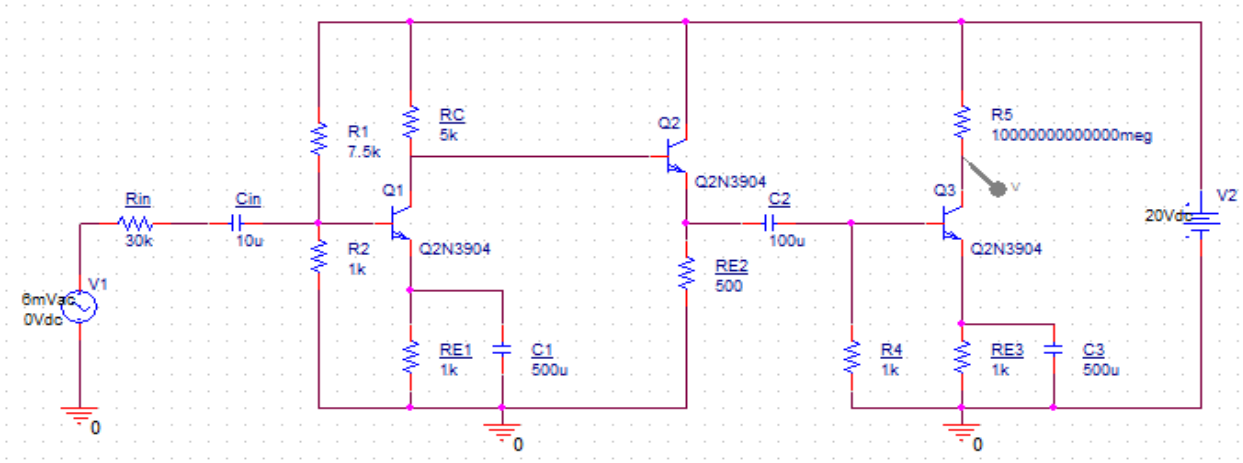


Figure 46: Equivalent circuit for drilling inaccuracy scenario

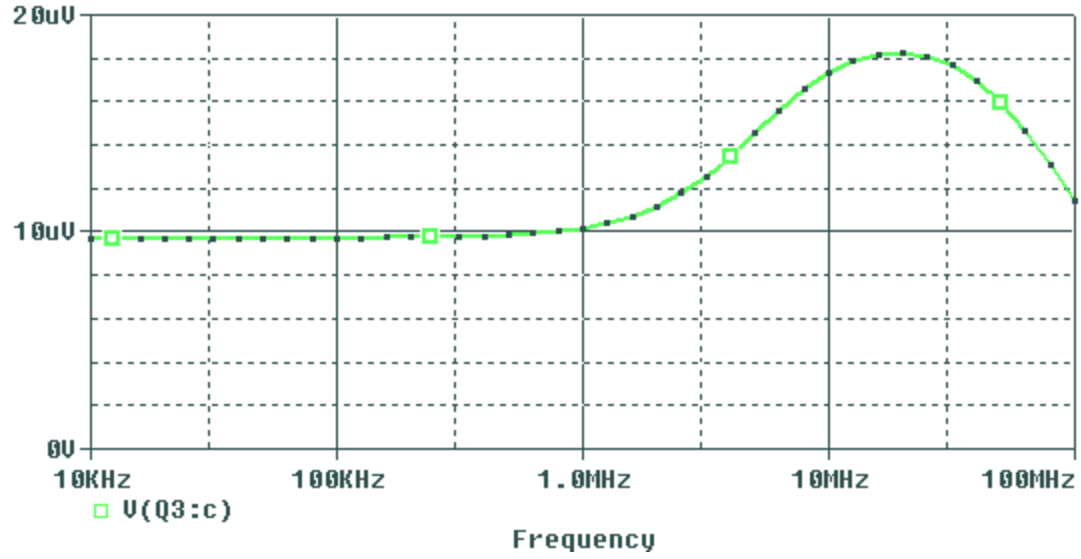


Figure 47:Vout versus frequency

Voids in holes/vias

As per IPC-600g-253 standards, the minimum quality requirement for holes in PCB are holes should not contain more than three voids or not more than 10% of the holes has voids. All voids should also be less than 90^{o} circumference of the holes. If these minimum requirements are not fulfilled the board will be defective.

Conductor/trace spacing

Edge copper roughness or copper spikes should not reduce conductor spacing by more than 20% in an isolated area. If it is failed to meet such criteria, defects can occur.

Results Summary

No.	Type of circuit	Gain (dB)
1	Normal	39.55
2	Scenario1, over etching A1, RA1=4.9Ω	36.78
3	Scenario1, over etching A2, RA1=6.367Ω	36.12
4	Scenario1, over etching A2, RA1=14.367Ω	32.99
5	Scenario2, B2, open circuit	No output
6	Scenario3, C, short circuit	-109.11 (very small output)
5	Drilling	-28.87 (diminished output)

Chapter Five

Conclusion and Recommendation for Future Works

5.1 Conclusion

This thesis work focuses on the effects of inaccurate PCB manufacturing on the levels of malfunctioning circuits. The affecting parameters for each PCB manufacturing processes are discussed.

The drum speed and resolution are the important parameters in photo plotting process while focus and dose are in photolithography. If the photo plotter is run with high drum speed and wrong resolution, a blurred image of traces and pads occur. Consequently, this causes misalignment, wrong sizes and shapes of traces and pads. In this case, the gap between traces will be abnormally too small or large which happens short circuiting and open circuiting or circuits with poor performance. On the other hand, with wrong dose and focus, circuit results in fringing and bridging errors.

In etching and drilling processes some simulations using OrCAD PSpice has been made to illustrate the possible effects on the different circuits given the possible manufacturing errors. From the samples, small change reduction of widths of traces (over etching) results in small performance reduction of the given circuit. If the over etching rate is medium, then a medium performance reduction happens. For much larger over etching rate, there is a higher probability of totally malfunctioning of the circuit.

Similarly, in drilling process when it is wrongly or inappropriately drilled, the top and bottom layers may not be connected. In this case components on the top will not be connected fully, one of their terminals may be left floating. The effect is poor circuit performance or malfunctioning depending on the level of drilling errors. Another scenario is short circuiting happens when drilling of nearby holes is unnecessarily too close. This can also cause malfunctioning of PCB circuits.

In the over etching scenario, output voltage drops from 50mV to 32mV when the resistance increases from 10 to 16.9 ohms which means 64 % of the output voltage reduction occurred for a 69% increase in resistance. This simply considering only one simple scenario the effect will be

even worsened when similar individual effects are added to it. For capacitive effects, the output becomes unstable and oscillating.

In view of the above, it can be concluded that the output of the circuits is affected as the manufacturing processes become inaccurate. Finally, it results in signal loss, poor performance of and malfunctioning of circuits.

5.2 Recommendation for Future works

In this research causes of circuit malfunctioning and the parameters for each process is presented. Some simulations are also done to illustrate the consequences of the effects in major manufacturing processes.

However, there are lots of tasks left open for next researches. Establishing relationship or developing mathematical model for each process and with their respective manufacturing parameters to see the possible effects for any change in the parameters.

Another thing, this thesis paves the way for further research on how to improve each manufacturing processes against their process controlling parameters.

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