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Department of Electrical and Computer Engineering

DIGITAL CONTROL FOR SWITCHED MODE CONVERTERS INPUT POWER FACTOR CORRECTION

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ABBREVIATIONS

AC	Alternating Current
APFC	Active Power Factor Correction
BSF	Band Stop Filter
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DF	Distortion Factor
EMF	Electromotive Force
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
IEC	International Electronic Community
IEEE	Institute of Electrical and Electronic Engineers
PF	Power Factor
PFC	Power Factor Correction
PI	Proportional Integral
PPFC	Passive Power Factor Correction
PSD	Power Spectral Density
PWM	Pulse Width Modulation

RMS	Root Mean Square
SMPS	Switched Mode Power Supplies
THD	Total Harmonic Distortion
UPF	Unity Power Factor
UPS	Uninterrupted Power Supply
VAR	Volt Ampere Reactive

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Input power factor of static power converters is generally low due to angular displacement between input voltage and current plus due to current distortion. On the other hand, static power converters usage is increasing continuously with the increase in use of power supply units to commercial, industrial and residential complex automation and communication systems. This increase in application of power converters has increased the reactive power demand from the utility grid resulting in inefficiency and overloading of the transmission and distribution network.

In this thesis, a digitally controlled switched mode PFC (power factor correction) converter has been designed, modeled and simulated. The three major control modes which are used for switched mode converter control are the voltage mode control, current mode control and the PFC mode control. These three control modes have been simulated using the MATLAB Simulink for 100%, 75%, 50%, 25% and 10% power loading. For the 100% load (full load) it has been found that the PFC mode controller achieves a near unity input power factor with power factor of 0.99975. At full load, the voltage mode and current mode controller have a lower power factor of 0.943 and 0.945 respectively. For the other loadings, the PFC mode controller has a near unity power factor which is greater than 0.99, whereas the voltage mode and current mode controller have a lower power factor. The PFC mode controller performs well even if there is variation in input voltage and load. In addition, the lowest total harmonic distortion (THD) and reactive power, and the highest power factor (PF) are obtained using the PFC mode control. From the results obtained, it can be concluded that the PFC mode controller is the best control scheme to be used for such control applications.

Digital control for power factor correction is an important field of study since it can be used to reduce the harmonics in the line current, increase the efficiency of power systems, and reduce customersô utility bills. The results of this study are useful for many applications such as an uninterrupted power supply (UPS), telecom power supply, motor drive inverter, personal computers, battery charging, DC motor drive, welding machine and other power supplies for electronic equipment.

Keywords: Power factor, PFC converter, Boost converter, Digital control.

CHAPTER 1

INTRODUCTION

1.1 Background

Switched mode AC to DC converters' applications are increasing exponentially with the growth in use of power supply to electronic automation, control and communication systems including DC drives. Most power supplies are designed to meet regulated output, isolation and power factor correction (PFC) [2].

Regulation means that the output voltage must be held constant within a specified tolerance for changes within a specified range in the input voltage and the output loading. Isolation is needed when the output may be required to be electrically isolated from the input.

Power factor correction (PFC) is becoming a very important field in power electronic world. Adding more generating capacity to the world's electrical companies due to higher demand recently is very costly and would consume additional resources. One method of using extra power capacity is to use the AC power more efficiently through the broad use of power factor correction. Most of researches in power factor correction are based on reduction of harmonic contents in the line current. In passive PFC, only passive elements are used to improve the shape of input line current. In active PFC circuit, an active semiconductor device is used together with passive elements to shape the input current and also controlling the output voltage [3, 5].

Beside these requirements, common goals are to reduce the converters' size and weight and to improve efficiency. Traditionally, linear power supplies have been used. However, advances in semiconductor technology have lead to switched mode power supplies, which are smaller and much more efficient compared to linear power supplies. The number of switched mode power supplies (SMPS) and other power electronics appliances are increasing since motors, electronic power supplies and fluorescent lighting now consume significant part of the generated electric

power in the world [6, 7]. SMPS are needed to convert electrical energy from AC to DC and are used as a replacement of the linear power supplies when higher efficiency, smaller size or lighter weight is required.

Efficiency of the utility system has led to increased demands for high power factor and low total harmonic distortion (THD) in the current drawn from the utility. Electromagnetic pollution of the power line introduced by power electronic systems include harmonic distortion due to nonlinear loads, typically, rectifiers. So, PFC converter circuits to improve the AC current waveform must be used. Single-phase diode bridge rectifiers with output capacitor filter are gradually being replaced by pulse-width modulation (PWM) PFC rectifiers to maintain a sinusoidal input current at near unity power factor and to satisfy the necessary harmonic regulations. Power factor correction (PFC) rectifiers with one active element are one of the cheapest topologies which used for providing this goal. Features of this type of converters have received considerable attention in the recent two decades [4, 7].

The demand for power, which has increased tremendously over the last few decades, has forced the power engineers to establish reliable network in order to supply quality power to the consumer. Over the years lot of research has been carried out for the supply of quality power to the consumers. This research got a tremendous boost with the strides made in the miniaturization of the electrical industry. The power electronic devices are very versatile devices capable of delivering power as high as 10KW. PFC converters are capable of working at frequencies in the range of hundreds of KHz and at the same time the control being only at the gate terminal of the devices, which makes these devices easily controllable. There are various types of single-phase PFC converter circuits. A sinusoidal current waveform in phase with the ac line voltage and the constant dc voltage can be obtained from these PFC converter circuits [2, 3, 7].

A power factor correction (PFC) system is commonly used in medium- or high-power power supply applications which require the ideal ohmic load character at the line input, low harmonic current injection into the line, and high efficiency. This would include such applications as an uninterrupted power supply (UPS), telecom power supply, motor drive inverter, personal computers, battery charging, DC motor drive, welding machine and other power supplies for

electronic equipment. Power factor correction (PFC) converters aim to increase the power factor (PF) and decrease the total harmonic distortion (THD) of the input current. Power factor correction (PFC) is necessary for ac-to-dc switched mode power supply in order to comply with the requirements of international standards, such as IEC-1000ï 3ï 2 and IEEE-519. PFC can reduce the harmonics in the line current, increase the efficiency and capacity of power systems, and reduce customersô utility bills. In order to achieve unity power factor in the switched mode power supply, many control methods can be used including average current control, peak current control, hysteretic control, nonlinear carrier control, etc [4, 6, 7]. In this study, average current mode control is employed.

The function of Power Factor Correction is to force the input current follow the input voltage by using control methods so as to achieve unity power factor. In power electronic area, the power factor will be decreased and result in loss if one of the following two conditions is satisfied:

(1) the input current is not a sine wave;

(2) the phase of the input current is not the same as the input voltage.

By applying the power factor correction circuit, the input current can be forced to be a sine wave with the same phase as the input voltage [1, 2]. Therefore, it is of great necessity to apply the PFC to the switch mode power system.

In many types of PFC topologies, the most effective topology for a PFC converter is the boost converter, because the boost converter has continuous input current that can be manipulated with an average-current-mode control technique to force the input current to track the changes in line voltage. Moreover, the boost PFC converter has many advantages such as increasing power density, reducing input current ripple and RMS current of the boost capacitor and reducing filter volume [5, 6, 7].

The analog control has been the conventional method of power factor correction (PFC) in switched mode power supplies (SMPS) for a relatively long time. But recently more attention is being given to digital control techniques. With the development of digital techniques, more and more control algorithms are implemented in power electronics circuits by the digital chips. One

reason is that digital control can implement more complicated algorithms. Another reason is that digital control has many advantages over analog control, including programmability, adaptability and reduced susceptibility to environmental variations, etc. In addition, it is possible to achieve better performance in digital implementation than that in analog implementation with the same cost [4, 14].

1.2 Statement of the Problem

The term ñpower factorò or PF in the field of power supplies slightly deviates from the traditional usage of the term, which is applied to reactive AC loads, such as motors powered from the AC power line. Here, the current drawn by the motor would be displaced in phase with respect to the voltage. The resulting power being drawn would have a very large reactive component and little power is actually used for producing work. However, in power electronics field, some of the equipment generates pulsating currents to the utility grids with poor power quality at high harmonics contents that adversely affect other users. The situation has drawn the attention of regulatory bodies around the world. Governments are tightening the regulations and setting new specifications for low harmonic current [17].

Since the number of electronic appliances is growing, an increasing amount of non-sinusoidal current is drawn from the distribution network. Consequently, due to the increasing amount of harmonic currents drawn, the distribution network becomes more and more polluted. As a direct consequence, available power from the grid becomes less. This is because unnecessary current components, which contribute to the root mean square (RMS) value of the line current is drawn from the grid which produces unnecessary power. On the other hand, the harmonic currents distort the line voltage waveform, and may cause malfunction in sensitive electrical equipment connected to the grid.

In Switched mode power supplies (SMPS), the problem lies in the input rectification and filter network [21, 26]. The equipment connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification. AC to DC rectifiers usually interfaced with the mains. These devices convert the sinusoidal line voltage to a DC voltage. However, the

rectification process produces a non-sinusoidal line current due to the nonlinear input characteristic. It is a well-known fact that the input current of an SMPS tends to have a non-sinusoidal, distorted waveform. The distorted line current of a power converter is composed of the line frequency component and higher frequency harmonic components of the current. It should be noted that only the line frequency component of the current is carrying the power when voltage is sinusoidal.

The current drawn by simple SMPS is non-sinusoidal and out-of-phase with the supply voltage waveform so the most common rectifier and SMPS designs have a very low power factor of less than 0.60, and their use in personal computers and compact fluorescent lamps presents a growing problem for power distribution. The use of digitally controlled PFC circuits significantly reduces this problem [5, 7].

In most of the PFC applications capacitor banks are used across the terminals and put into the system manually, depending on load current observation. These do not secure VAR (Volt Ampere Reactive) balance, sometimes under compensated or over compensated with over loading of the system [31]. In addition such system is bulky and needs frequent maintenance. When fine control of power factor is desired a large number of levels of compensation with a large number of capacitors, associated relays and contactors are required. Because of the above reasons it is advisable to use active power factor correctors which are controlled digitally.

1.3 Objectives of the Study

This research aims to implement the unity power factor (UPF) controller for single-phase rectifier which is used in designing the high-end SMPS by using the active power factor correction (APFC) approach. The preferable type of PFC is active power factor correction (APFC) since it provides a more efficient power usage. An active PFC uses a circuit to correct power factor and is able to generate a theoretical power factor near to unity. Active power factor correction also markedly diminishes total harmonics, automatically corrects AC input voltage, and is capable for a wide range of input voltage.

The main or noble goal of this thesis is to design and implement a reliable digital controller for switched mode power factor correction (PFC) converters.

The specific objectives of this thesis are:

- to evaluate different PFC converter topologies and choose the best among them.
- to design and model a PFC converter.
- to determine the best control mode for unity power factor (UPF) digital controller.
- to design a digital controller for the PFC converter.
- to simulate a digitally controlled PFC converter and to analyze the results.

1.4 Outline of the Thesis

This thesis is organized into six chapters including this introduction which provides a summary of the background of this work, statement of the problem and the objectives of the study.

Chapter two surveys the current literature in the field of digital control for power supply systems particularly for switched mode power factor correction (PFC) converters. Chapter three presents the design and modeling of a PFC converter without the controller. State-space representation of the PFC converters, modeling of the open loop system and the boost PFC converter design is presented in this chapter.

Chapter four describes the design of the digital controller for a single switch PFC converter. Modeling of the digital controller and design in z-domain are presented in this chapter. Chapter five presents the simulation of the digitally controlled PFC converter with three modes of control, namely the current mode, the voltage mode and the PFC mode control. Finally chapter six presents the conclusions and suggestions for future work.

CHAPTER 2

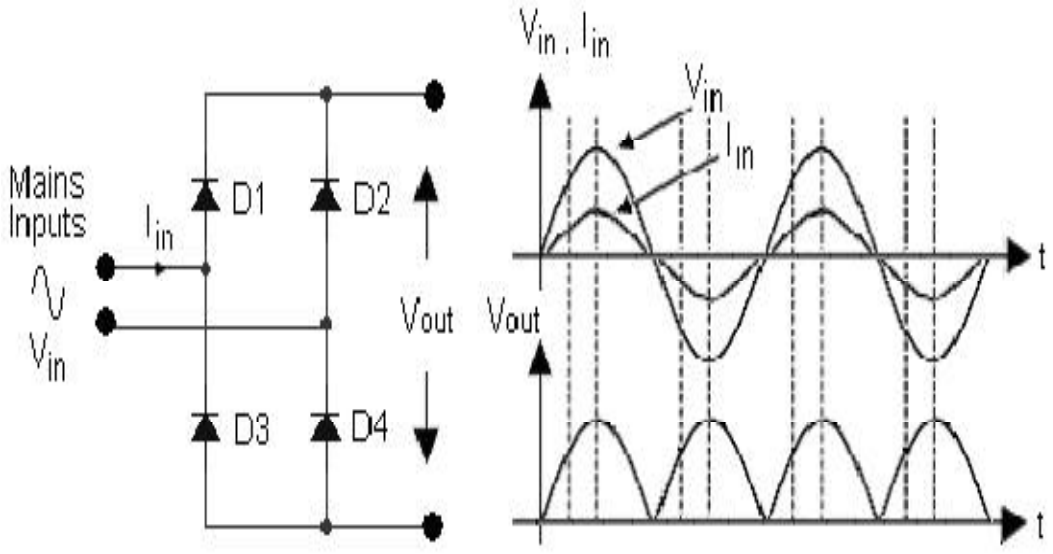
LITERATURE REVIEW

2.1 Introduction

The summary of results on previous research related to PFC techniques and input power factor corrected single-phase rectifier systems are introduced in this chapter. Numerous single-phase PFC topologies are classified and various PFC circuits for single-phase rectifiers are reviewed. The digital controller for the PFC circuit is also discussed in this chapter. Here, the study of PFC topologies is limited to single-phase systems since most SMPS are powered by a single-phase utility source.

2.2 Typical Power Supply Converters

In most power electronic applications, the power input from utility is a 50Hz sine wave AC voltage. For applications requiring DC, the AC voltage is then converted to a DC voltage by using rectifiers. The inexpensive way to convert AC to DC in an uncontrolled manner is by using rectifier with diodes, as shown in Figure 2.1 [35].



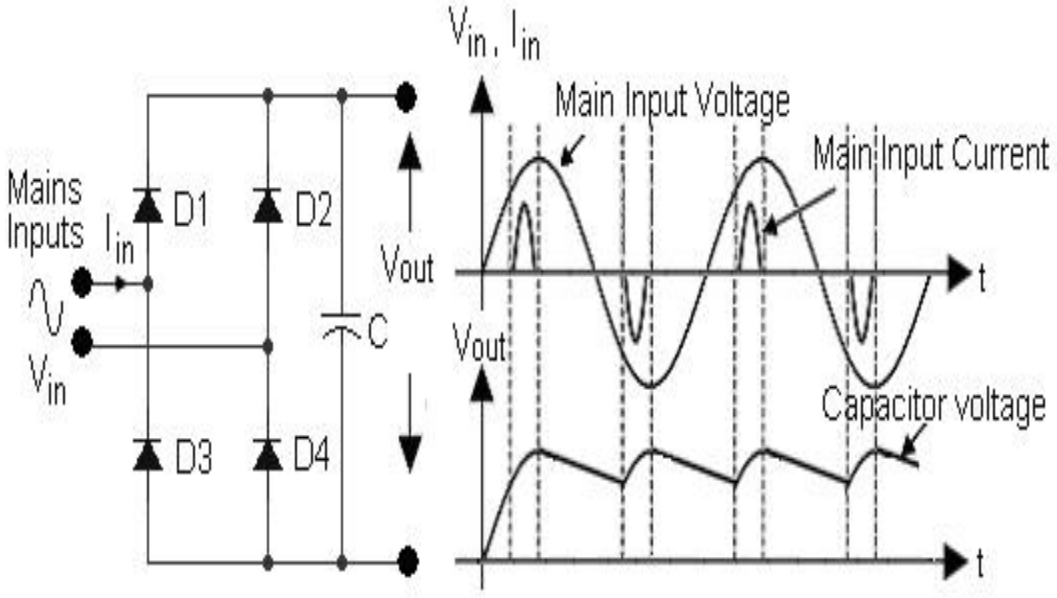
(a) Bridge rectifier (b) Inputs and Output waveforms

Figure 2.1: A diode bridge rectifier and waveforms [35].

The DC output contains high voltage ripple that is not suitable to supply a constant DC voltage. In most applications, the rectifiers are supplied directly from the utility source without a 50Hz transformer. The avoidance of this costly and bulky 50Hz transformer is important in most modern power electronic systems [20, 25, 35].

It should be noted in the circuit of Figure 2.1(a) that if a pure resistive is connected as load, the input current follows the waveform of input voltage. The voltage and current waveforms are shown in Figure 2.1(b). The circuit will have power factor equals to unity but a large output voltage ripple.

The conventional input stage of an off-line rectifier design associated with its waveforms is shown in Figure 2.2 [35].



(a) Off-line rectifier (b) Inputs and Output waveforms

Figure 2.2: A typical power supply with filter capacitor and waveforms [35].

It is comprised of a full-bridge rectifier followed by a large-input-filter capacitor. This input-filter capacitor reduces the ripple on the voltage waveforms into the DC converter stage. The problem with this input circuit is that it produces excessive peak input currents and high harmonic distortion on the line. The high distortion in the input current occurs due to the fact that the diode rectifiers only conduct during a short interval. This interval corresponds to the time when the mains instantaneous voltage is greater than the capacitor voltage. Since the capacitor must meet hold-up time requirements, its time constant is much greater than the frequency of the mains [20, 35].

The DC output voltage of rectifier should be as ripple free as possible. Therefore, a large capacitor is connected as a filter on the DC side. The capacitor will be charged during the peak of the AC input voltage and this will result in high peak input current. This rectifier draws highly distorted current from the utility.

The mains instantaneous voltage is greater than the capacitor voltage only for very short periods of time, during which, the capacitor must be charged fully. Therefore, large pulses of current are drawn from the line over a very short period of time, as shown in Figure 2.2 (b). This is true for all rectified AC sinusoidal signals with capacitive filtering. Twice per cycle every single-phase rectifier draws a pulse of current to recharge its capacitor to the peak value of the supply voltage. Between voltage peaks the capacitor discharges to support the load and the rectifier does not draw current from the utility. Therefore, the generation of harmonic currents due to the behavior of single-phase rectifiers, distorted currents are normally drawn from the input line resulting in low power factor, low distortion factor and high total harmonic distortion [20, 25, 29].

They draw high amplitude current pulses, the fundamental current of the line current is essentially in phase with the voltage, and the displacement factor is close to the unity [21]. However, the low-order current harmonics are quite large, close to that of the fundamental. From the line current spectrum it can be seen that the waveform contains a lowered fundamental frequency component plus 3rd, 5th, 7th, 9th and higher of current harmonics.

The addition of harmonic currents to the fundamental component increases the total RMS current. Because they affect the RMS value of the current, harmonics will affect the power factor of the circuit. A diode bridge rectifier with filtering capacitor is considered here as a non-linear load. The power factor for this circuit varies from 0.40 to 0.60 depending on the capacitance value. For a typical single-phase power supply shown above, it has 136% total current harmonic distortion, 59% distortion factor, unity displacement power factor and 0.59 true power factor [35].

2.3 Power Factor

Power factor (PF) is the ratio of average power to apparent power at an AC terminal [33].

$$PF = \frac{AveragePower}{ApparentPower} = \frac{avg[v(t) \cdot i(t)]}{V_{rms} \cdot I_{rms}} \qquad (2.1)$$

Assuming an ideal sinusoidal input voltage source, PF can be expressed as the product of two factors: the displacement factor $K_{d'}$ and the distortion factor K_d. The displacement factor $K_{d'}$ is the cosine of the displacement angle between the fundamental input current and the input voltage. The distortion factor K_d is the ratio of the root-mean-square (RMS) of the fundamental input current to the total RMS of input current. These relationships are given in equation (2.2) [33].

$$PF = \frac{V_{rms} I_{rms(1)} \cos\theta}{V_{rms} I_{rms}} = \frac{I_{rms(1)} \cos\theta}{I_{rms}} = K_d K_\theta \qquad (2.2)$$

Where: V_{rms} is the voltage total RMS value, I_{rms} is the current total RMS value, $I_{rms(1)}$ is the current fundamental harmonic RMS value, θ is the displacement angle between the voltage and current fundamental harmonics, $K_\theta = \cos\theta$ is the displacement factor, K_d is the distortion factor.

In Figure 2.3, examples of different current shapes show the different distortion factors and displacement factors [33].

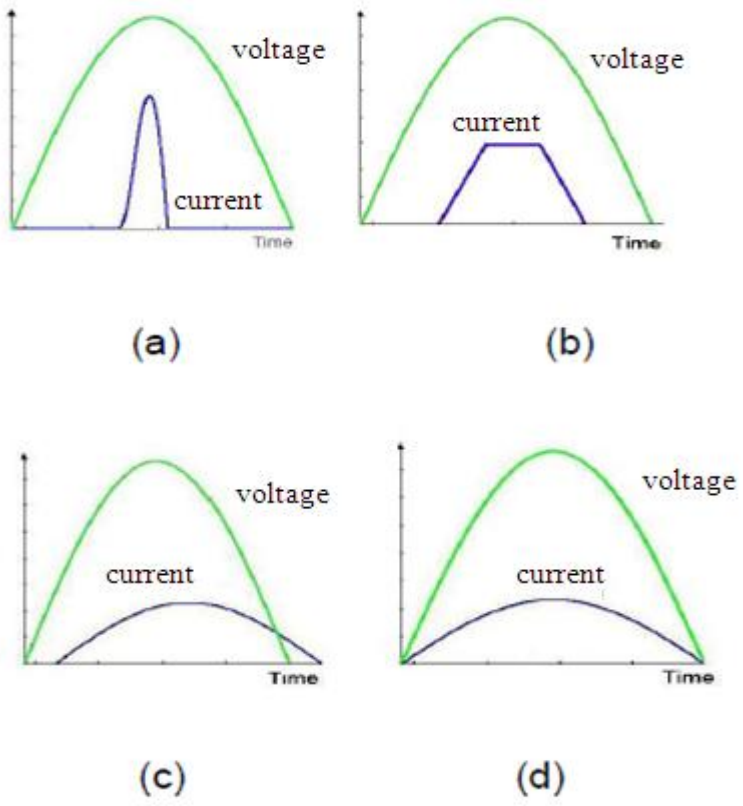


Figure 2.3: Illustration of PF relationship between current and voltage [33]:
(a) $K_d<1$, $K_d<1$, (b) $K_d=1$, $K_d<1$, (c) $K_d<1$, $K_d=1$, (d) $K_d=1$, $K_d=1$.

In the first case, a smaller K_θ means a larger apparent current for the same load. It is known that, current causes more losses in a supply and distribution system. Utility companies regulate customersô K_θ . In the second case, a small K_d means a large amount of harmonics in the current, which pollutes the utility power source and affects other users. All the power supplies have to meet PF standards, for example, the IEC 61000-3-2. Converting AC to DC, the conventional diode rectifiers always produce large amounts of harmonic current. Nowadays, the most advanced solution is to add PFC converter [21, 25, 33].

2.4 Power Factor Correction (PFC)

Due to the large harmonic content typical single-phase bridge rectifiers used for interfacing power electronic equipment with utility system may exceed the limits on the individual current harmonics and THD (Total Harmonic Distortion) specified by international standards [25, 35]. In view of low power factor drawbacks, some of alternatives for improving the input current waveforms are discussed along with their advantages and disadvantages. The technique used to improve the value of power factor is called Power Factor Correction (PFC). The classification of single-phase PFC topologies for diode bridge rectifier is shown in Figure 2.4 [35].

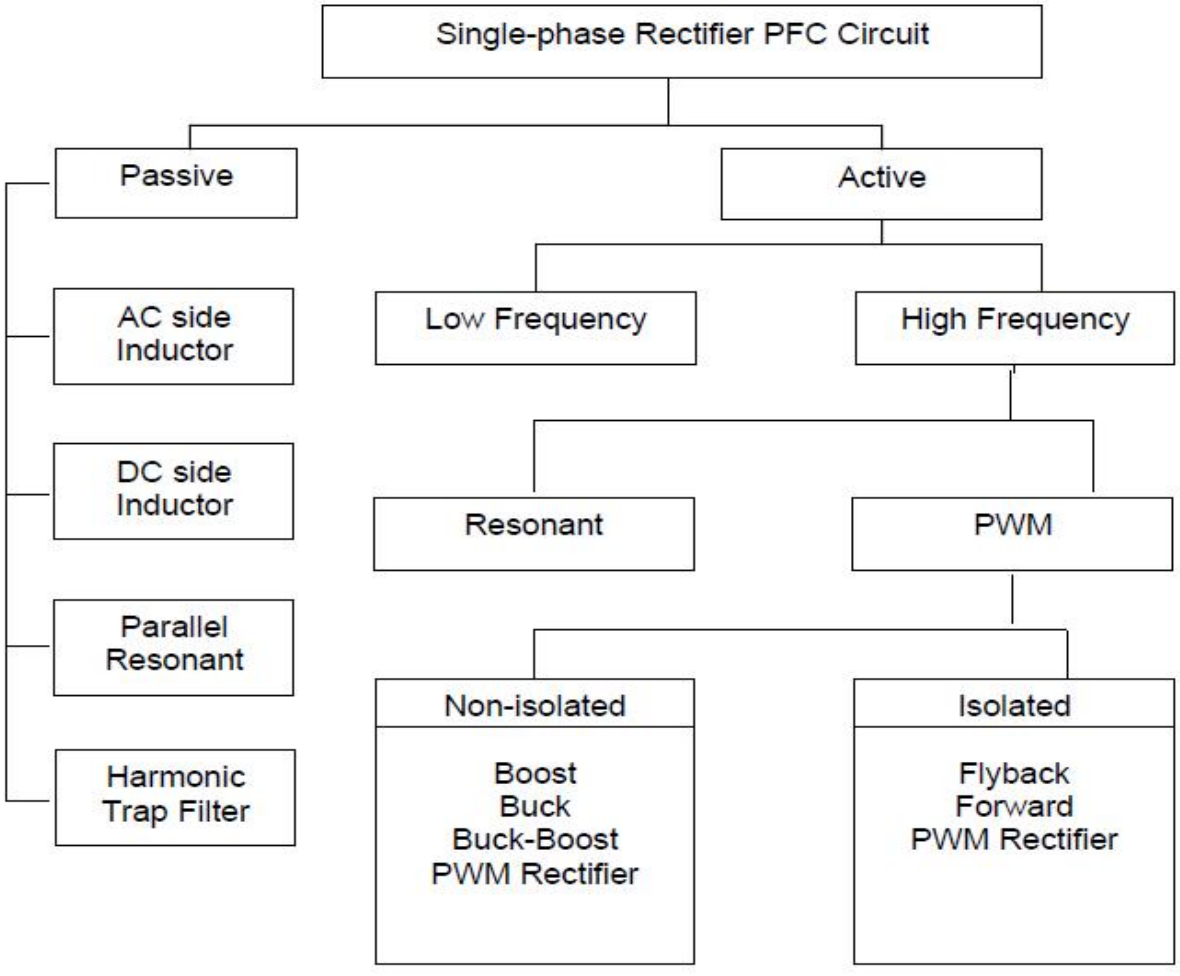


Figure 2.4: Classification of single-phase input PFC topologies for diode bridge rectifier [35].

PFC shaped the distorted input current waveform to approximate a sinusoidal current that is in phase with the input voltage. There are several effective techniques for getting a sinusoidal input current waveform with low distortion. The objective of PFC is to make the input to a power supply looks like a simple resistor. Two typical techniques for PFC can be divided into Passive Power Factor Correction (PPFC) and Active Power Factor Correction (APFC) [35].

Regardless of the particular converter topology that is used, the output voltage carries a ripple at twice the line-frequency. This is because in a single-phase system the available instantaneous power varies from zero to a maximum, due to the sinusoidal variation of the line voltage. On the other hand, the load power is assumed to be constant. Every single-phase PFC converter requires energy-storage (bulk) capacitor to handle difference between instantaneous input power and average output power [1, 35].

There are several approaches that have been taken by power designers to improve the value of power factor when they are designing SMPS. Most of them make use of PPFC as a solution to improve the waveform of line current in order to reduce the harmonic contents generated by SMPS. These approaches can be described as follows.

2.4.1 Passive PFC

The most common type of PFC is passive PFC. PPFC methods use additional passive components (capacitor or inductor) in conjunction with the diode bridge rectifier to correct poor power factor. A PPFC is more reliable than an APFC because no active devices are utilized. Because it operates at line frequency of 50Hz, PPFC requires relatively large fixed value inductors and capacitors to reduce the low frequency harmonic currents [10, 35].

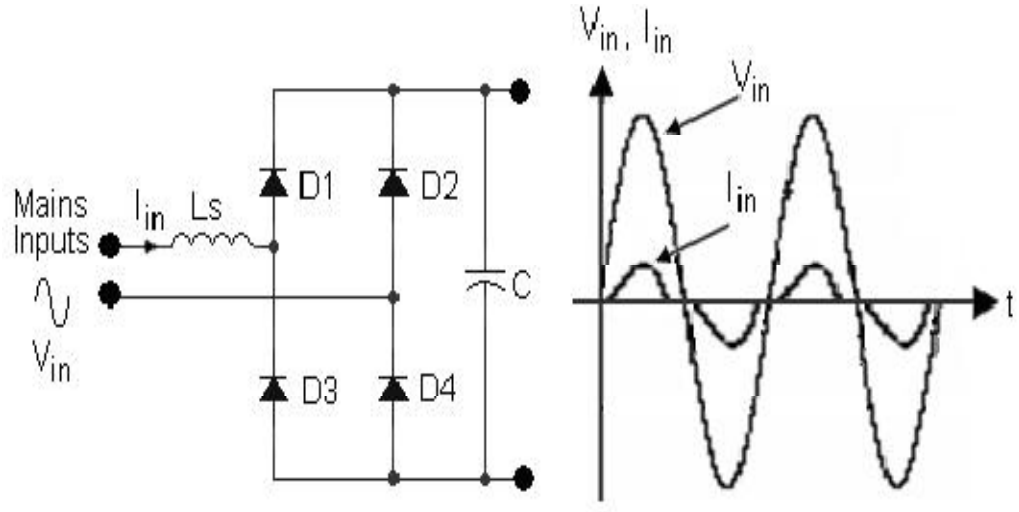
PPFC includes passive filters which can broadly be classified into series filters, shunt filters and a hybrid combination of the two. Series filters introduce impedances in series with the utility to reduce harmonic currents. Shunt filters provide a low impedance path for the harmonic currents generated by the rectifiers so that they are not reflected in the current drawn from the utility [10].

These filters use resonant pass or resonant trap circuits sensitive to both frequency and load. It is difficult to achieve unity power factor with PPFC. Also, very large currents may circulate in the filter. However, the passive is an effective PFC solution in cases where the line frequency, line voltage and load are relatively constant [35].

The various types of PPFC and the waveforms of input voltage and input current are discussed below and their associated waveforms are shown.

2.4.1.1 Rectifier with AC-side Inductor

The simplest methods is by adding an inductor at the AC-side of the diode bridge, in series with the line voltage as shown in Figure 2.5, thus to create circuit conditions such that the line current is zero during the zero-crossings of the line voltage [35].



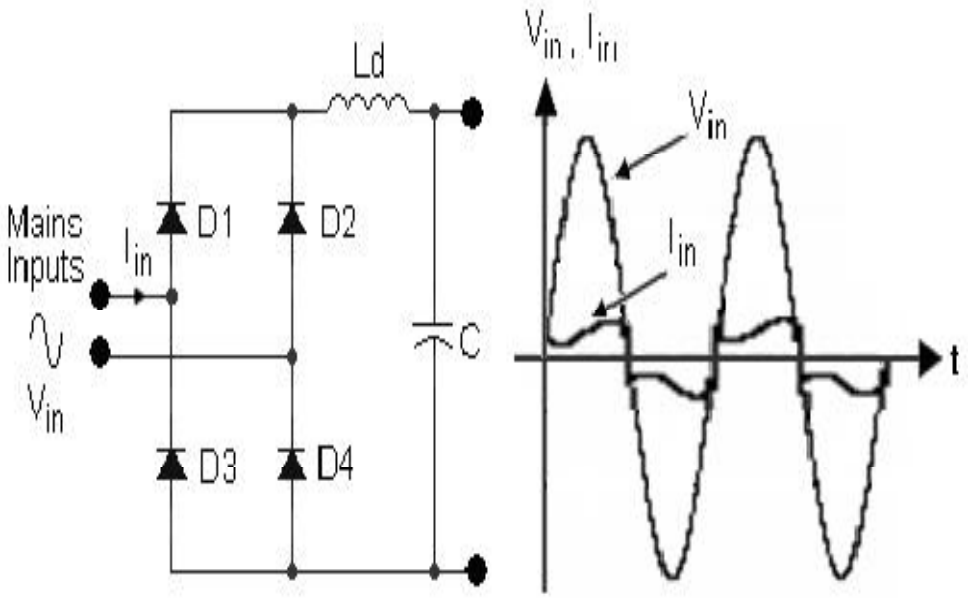
(a) AC-side inductor rectifier (b) Inputs waveforms

Figure 2.5: Rectifier with AC-side inductor and waveforms [35].

The advantages of this circuit are simplicity, low cost and improved shape of line current. However, the maximum power factor that can be obtained is 0.76 [35]. It can only improve harmonic current distortion to 30% to 40% at best. The output voltage cannot be controlled and it only slightly reduces small phase displacement of fundamental component.

2.4.1.2 Rectifier with DC-side Inductor

The inductor can be also placed at the DC-side, as shown in Figure 2.6. The inductor current is continuous for a large enough inductance Ld. In the theoretical case of near infinite inductance, the inductor current is constant, so the input current of the rectifier has a square shape [35].



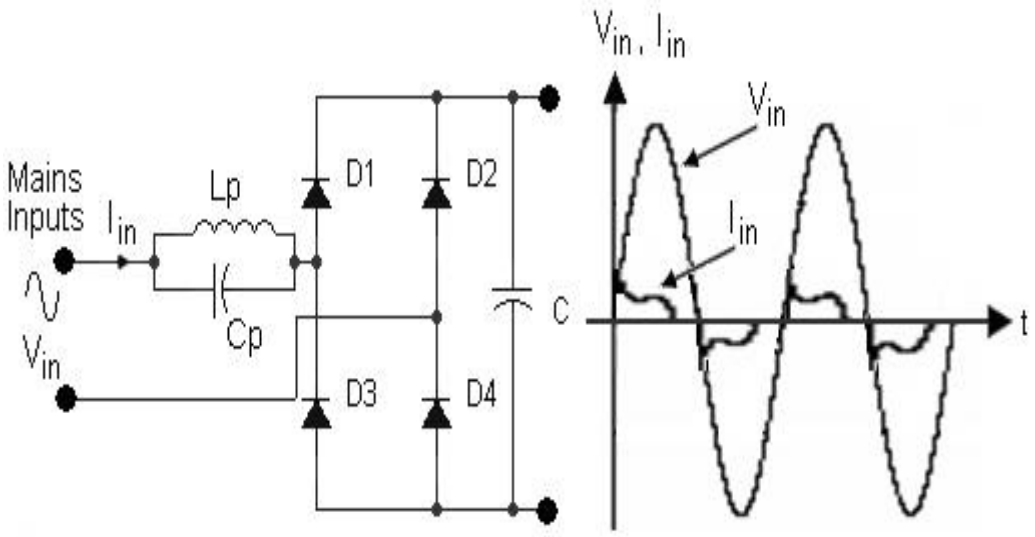
(a) DC-side inductor rectifier (b) Inputs waveforms

Figure 2.6: Rectifier with DC-side inductor and waveforms [35].

The advantage of this circuit is the shape of line current is improved. However, the maximum power factor that can be obtained is 0.85 [35]. Operation close to this condition would require a very large and impractical inductor. For lower inductance Ld, the inductor current becomes discontinuous.

2.4.1.3 Rectifier with Parallel-resonant Band-stop Filter (BSF)

The shape of the line current can be further improved by using a combination of low-pass input and output filters [30, 35]. There are also several solutions based on resonant networks which are used to attenuate harmonics. For example, a band-stop filter of the parallel resonant type as shown in Figure 2.7, tuned at the line frequency, is introduced in-between the AC source and the load [35].



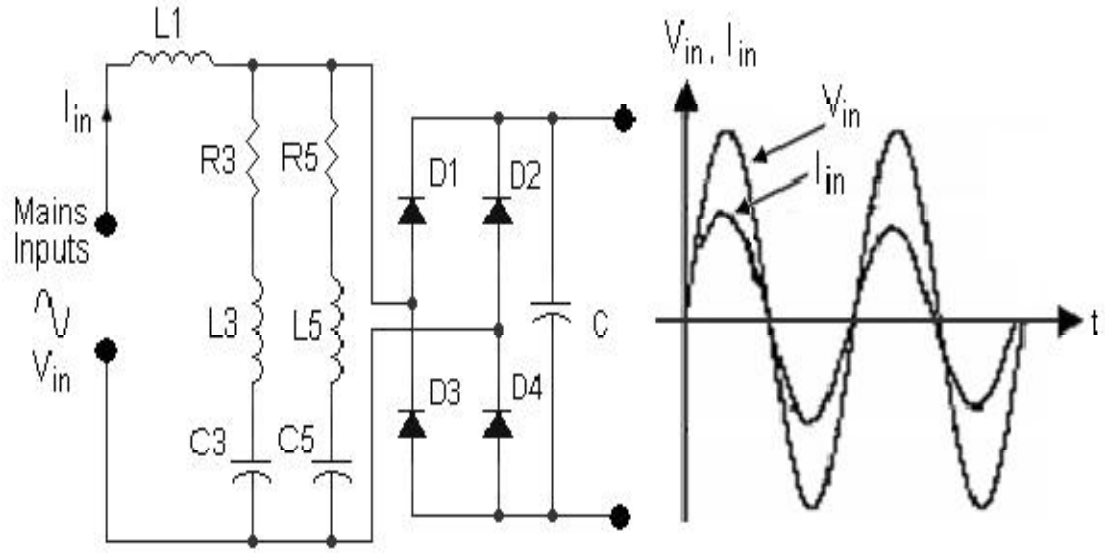
(a) Parallel BSF rectifier (b) Inputs waveforms

Figure 2.7: Rectifier with parallel-resonant BSF and waveforms [35].

The advantages of this circuit are lower value of capacitance element used and improve better the shape of line current. However, the maximum power factor that can be obtained is 0.90 [35]. This circuit requires a heavy and bulky inductor and must handle the rated full load current. This circuit can only supply nonlinear loads.

2.4.1.4 Rectifier with Harmonic Trap Filter

Another possibility is to use a harmonic trap filter. The harmonic trap consists of a series resonant network, connected in parallel to the AC source and tuned at a harmonic that must be attenuated [13, 35]. For example, the filter shown in Figure 2.8 has two harmonic traps, which are tuned at the 3rd and 5th harmonic respectively.



(a) Harmonic trap filter rectifier (b) Inputs waveforms

Figure 2.8: Rectifier with harmonic trap filter and waveforms [35].

Some of the advantages of this circuit are no high frequency losses, provides low impedance to tuned frequency and greatly improves the shape of line current. However, the maximum power factor that can be obtained is 0.95 [35]. It only filters a single (tuned) harmonic frequency. Therefore, multiple filters are required to satisfy typical desired harmonic limits. This resonant circuit is very sensitive to line frequency and it can import harmonics from other nonlinear loads. The voltage regulation is also low.

PPFC have certain advantages, such as simplicity, reliability and ruggedness, insensitive to noise and surges, no generation of high-frequency Electromagnetic Interference (EMI) and no high

frequency switching losses. On the other hand, they also have several drawbacks. Solutions based on filters are heavy and bulky, because line-frequency reactive components are used [27, 34].

They also have poor dynamic response, lack voltage regulation and the shape of their input current depends on the load. Even though line current harmonics are reduced, the fundamental component may show an excessive phase shift that reduces the power factor. Moreover, circuits based on resonant networks are sensitive to the line-frequency. In harmonic trap filters, series-resonance is used to attenuate a specific harmonic [11, 35]. However, parallel-resonance at different frequencies occurs too, which can amplify other harmonics. Better characteristics are obtained with APFC circuits, which are reviewed in the following section.

2.4.2 Active PFC

An active power factor correction (APFC) performs much better and is significantly smaller and lighter than the PPFC circuits. An APFC refers to the use of a power electronic converter, switching at higher frequency than line frequency, to shape the input current to be sinusoidal and in-phase with the input utility voltage. Using APFC techniques, it is possible to achieve a power factor near unity and current THD less than 5% [17, 35].

Despite of active wave shaping, APFC includes feedback sensing of the source current for waveform control and feedback control to regulate the output voltage even when the input voltage varies over a wide range. Compared with passive solutions, they are less bulky and can easily meet the standards of harmonic distortion. Figure 2.9 shows the block diagram of an APFC circuit.

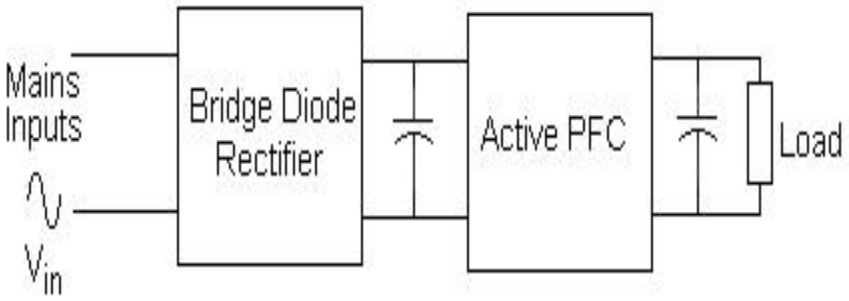


Figure 2.9: Block diagram of a rectifier with APFC [35].

For single phase PFC, a AC-DC converter is placed in between the input voltage and the load. In principle, any AC-DC converter can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties. For this reason, the basic Buck, Boost and Buck-Boost converters were considered and analyzed. These converters may operate in Continuous Conduction Mode (CCM), where the inductor current never reaches zero during one switching cycle or Discontinuous Conduction Mode (DCM), where the inductor current is zero during intervals of the switching cycle [35].

The result is a large current ripple in DCM and a smaller current ripple in CCM. The choice of CCM or DCM depends on which SMPS is used and the necessary current and power rating required. DCM is often implemented in low power design where the current ripple is lower. CCM is often preferred at high power levels.

2.4.2.1 Buck Converter

The Buck converter has a lower output voltage than input voltage, and it has pulsating input current generating high harmonics into the power line. This circuit is not practical for low-line input because it does not draw the input current when input voltage is lower than the output voltage. The line current of a PFC based on a Buck converter has distortions and the input current of the converter is discontinuous [34, 35]. Therefore, it has relatively low power factor. The conventional buck converter is shown in figure 2.10 [30].

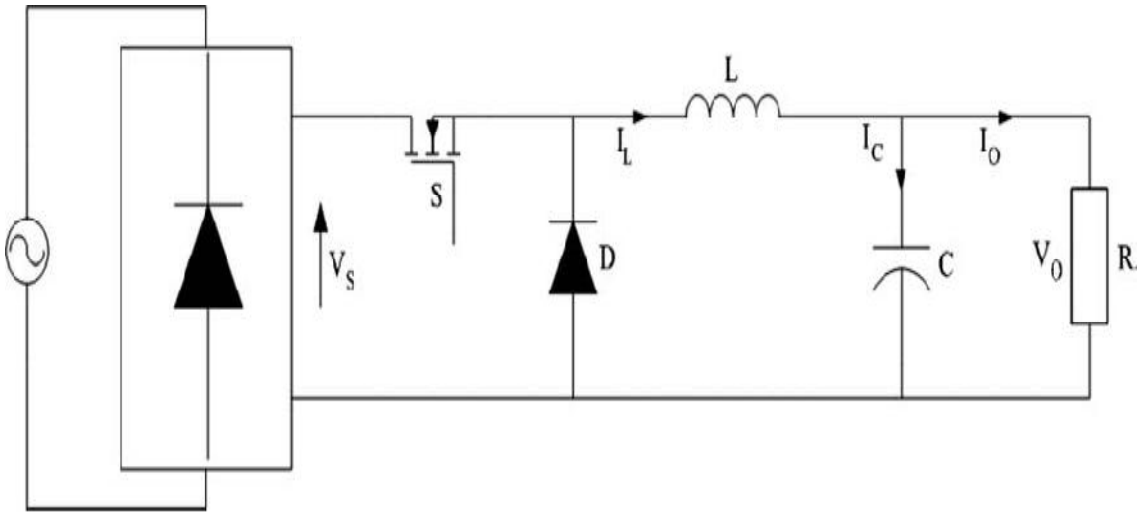


Figure 2.10: Buck converter [30].

2.4.2.2 Boost Converter

The Boost converter is shown in Figure 2.11, it has step-up conversion ratio. Therefore the output voltage is always higher than the input voltage. The converter will operate throughout the entire line cycle, so the input current does not have distortions and continuous. It has a smooth input current because an inductor is connected in series with the power source. In addition, the switch is source-grounded, therefore it is easy to drive. This topology is a universal solution for off-line power supplies and SMPS applications [35].

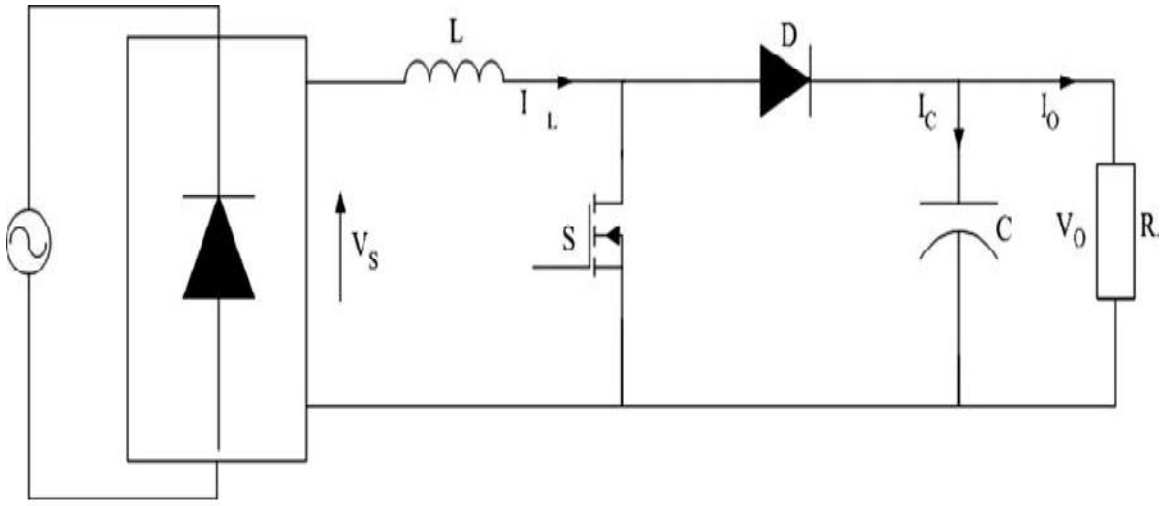


Figure 2.11: Boost converter [30].

2.4.2.3 Buck-Boost Converter

The buckï boost converter regulates the average output DC voltage both lower and higher than the input voltage [35]. The circuit diagram of the buckï boost converter is shown in Figure 2.12.

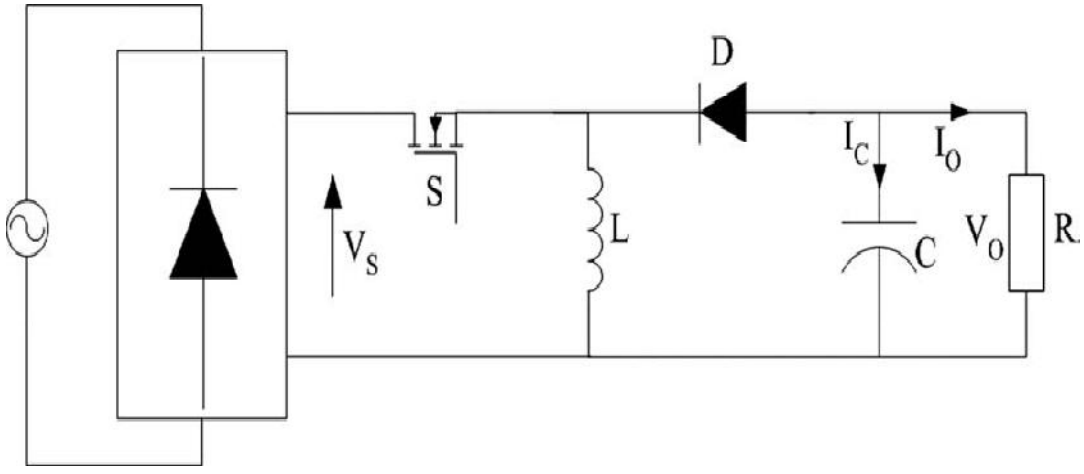


Figure 2.12: Buck-boost converter [30].

2.5 Control Structure of Boost PFC Converter

Among the three basic power converters buck, boost and buck-boost the boost converter is the most suitable for use in implementing PFC. Because the boost inductor is in series with the line input terminal, the inductor will achieve smaller current ripple and it is easier to implement average current mode control [18, 33]. Whereas, Buck converter has discontinuous input current and would lose control when input voltage is lower than the output voltage. The buck-boost converter can achieve average input line current, but it has higher voltage and current stress, so it is usually used for low-power application. The power stage adopted in this thesis is boost converter operating in continuous conduction mode. Figure 2.13 shows the circuit diagram of the boost PFC converter.

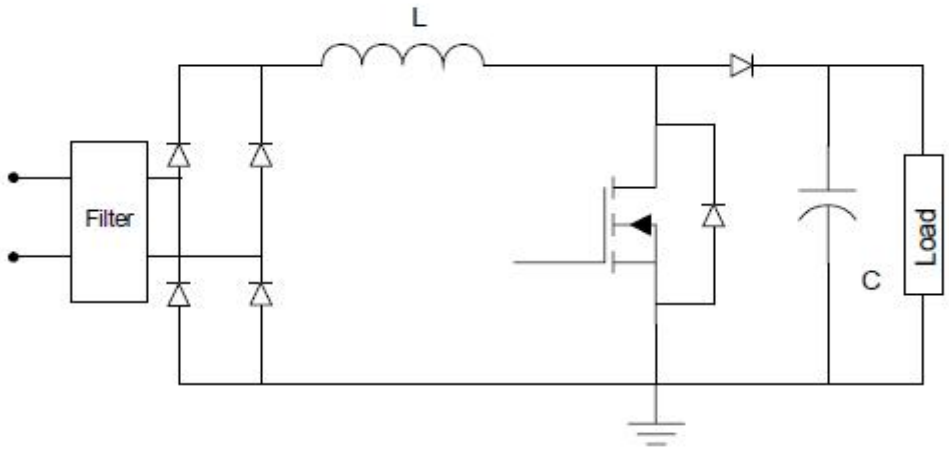
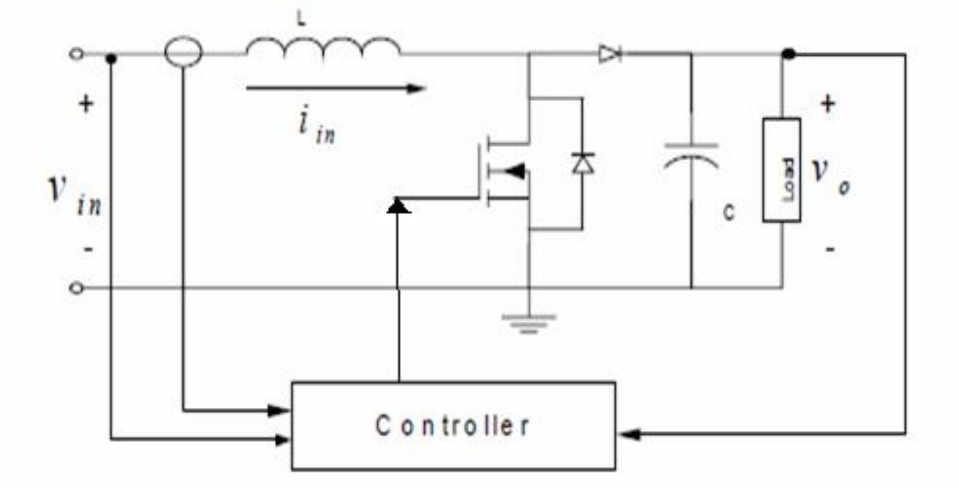


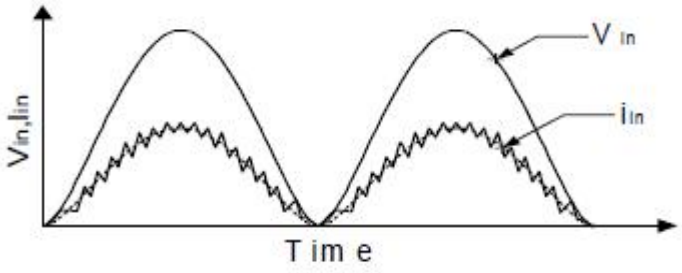
Figure 2.13: Boost Power Factor Correction converter [33].

As shown in Figure 2.14, the digital controller for the boost PFC has two tasks which are:

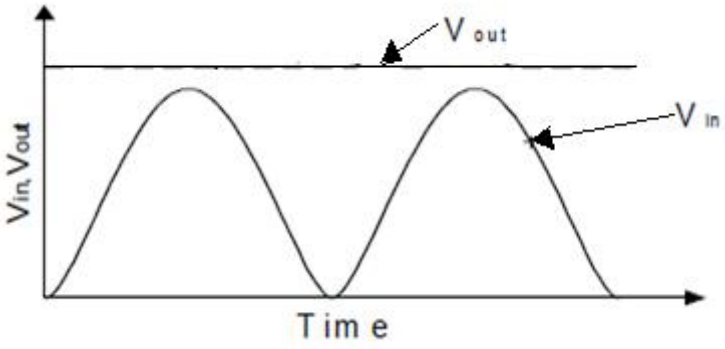
- Current tracking forces the average inductor current to track the current reference so that it has the same shape as the input voltage, as shown in Figure 2.14 (b). This task gives the input a unity PF.
- Voltage regulation regulates the output voltage keeping the output voltage equal to some predefined level, which is higher than the input voltage as shown in Figure 2.14 (c).



(a)



(b)



(c)

Figure 2.14: Boost PFC converter controller [33]: (a) Boost PFC with controller, (b) Waveforms of input voltage and inductor current, (c) Waveforms of input voltage and output voltage.

The analog control structure for a single switch CCM PFC boost converter is illustrated in Figure 2.15. The PFC converter has a three-loop control structure. The fast current loop keeps the input current the shape of the input voltage, which renders the unity PF. The input voltage feed forward loop is to compensate the input voltage variation. The voltage loop keeps the output voltage at some higher level than the input voltage. The voltage loop is very slow to avoid introducing 2nd harmonic ripple into the current reference [33]. Figure 2.16 shows the control structure of the digital controller for a single-switch PFC converter.

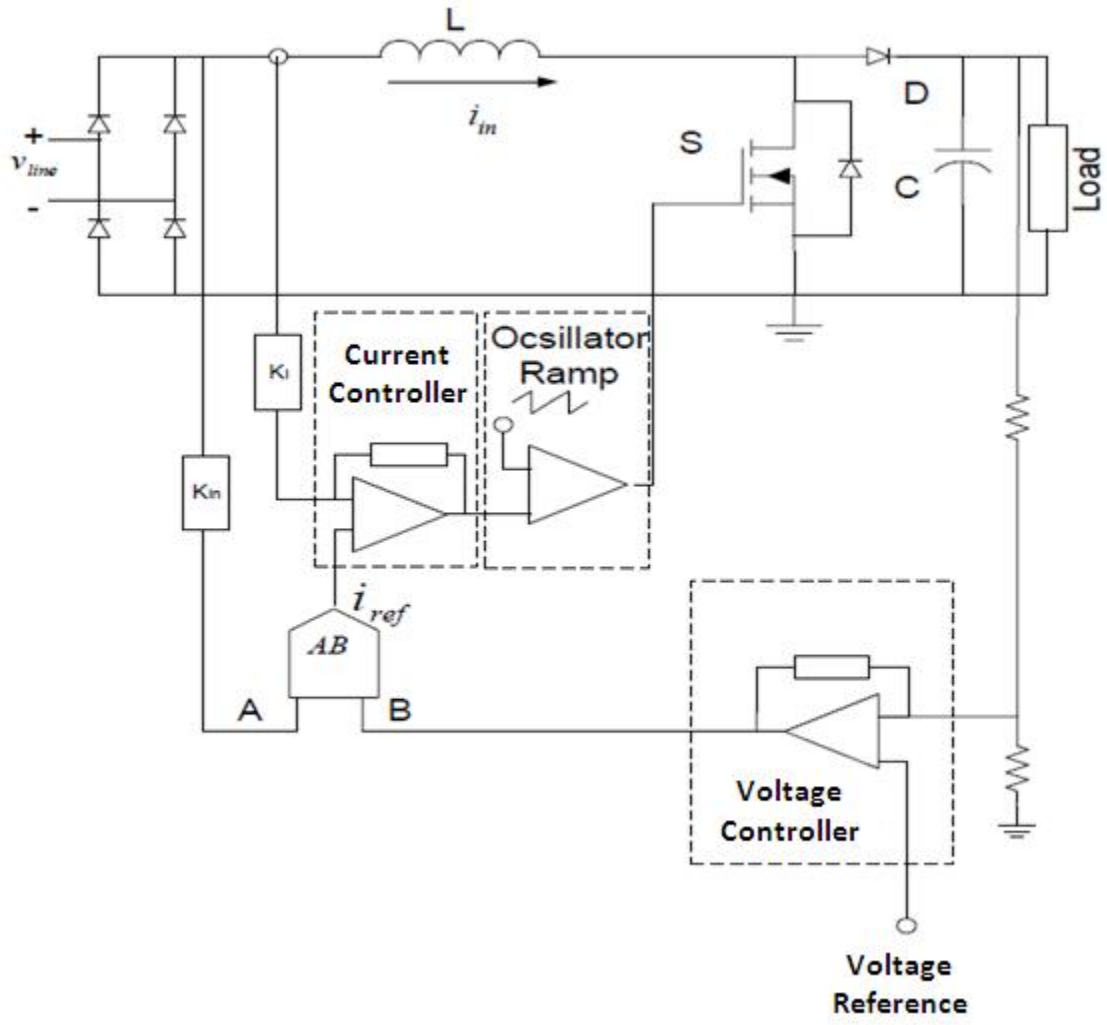


Figure 2.15: Analog average current control for boost-type PFC [33].

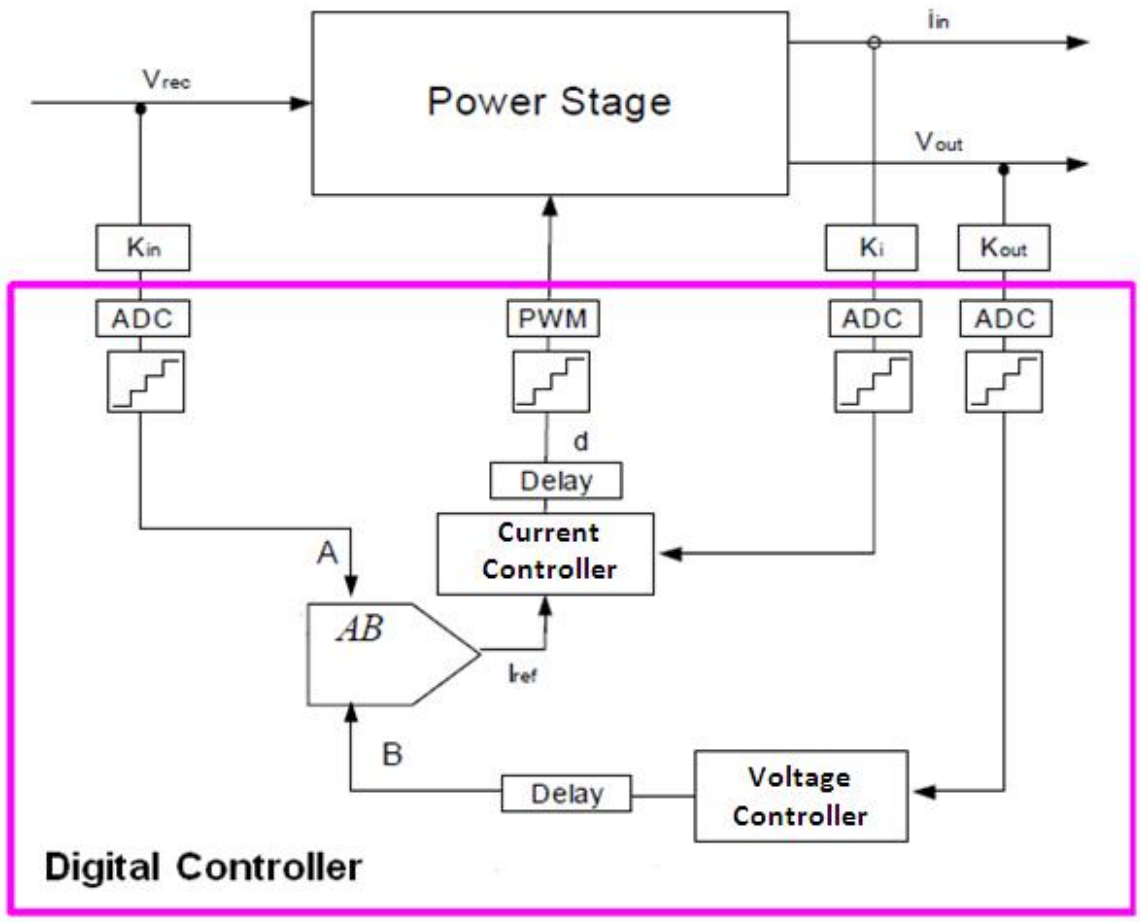


Figure 2.16: Digital control structure of single-switch PFC [33].

CHAPTER 3

DESIGN AND MODELING OF PFC CONVERTER

3.1 Fundamental AC-DC Converter Circuits

ACï DC conversion technology is a major research area in the field of power electronics and has been under development for decades. ACï DC converters are commonly used in applications requiring regulated DC power such as computers, communication devices, battery chargers, switched mode power supplies, and DC machine drive applications. Generally, unregulated DC voltage obtained from rectifying the line voltage is used at the input of these converters. Therefore, step down and step up are occurring at the input of these converters as a result of changing the line voltage [23, 30]. These converters are being used for converting AC voltage level to needed regulated DC voltage. A standard ACï DC converter system is shown in Figure 3.1 [30].

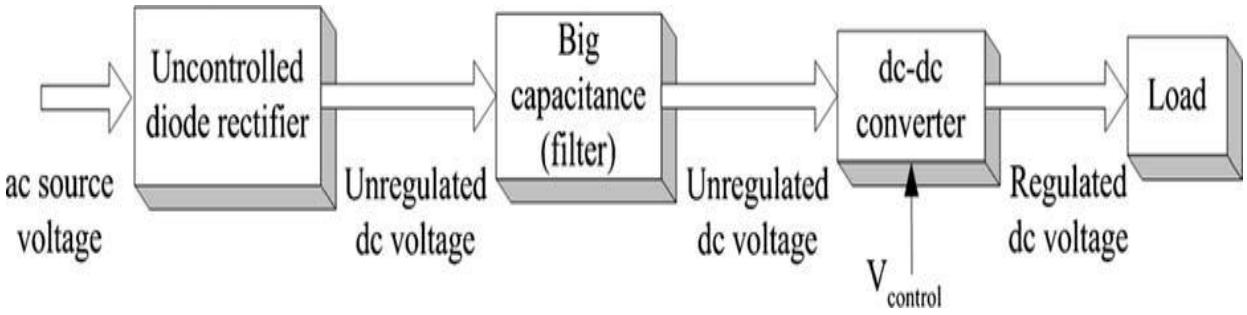


Figure 3.1: An ACï DC converter system structure [30].

ACï DC converters can be divided under two categories which are non-isolated and isolated AC-DC converters [30]. The classifications of these converters are shown as follows:

Non-isolated fundamental AC–DC converters:

(1) Buck converter.

(2) Boost converter.

(3) Buckï boost converter.

(4) C´uk converter.

(5) SEPIC converter.

Isolated fundamental AC–DC converters:

(1) Flyback converter.

(2) Forward converter.

(3) ZETA converter.

Buck, boost, and buckï boost converters are the main structures of ACï DC converter circuits. When these three main converters are investigated, operating principles, basic functions, circuit structures of these circuits, and the topologies coming along the developing duration of these can be understood. The state-space representation of the fundamental non-isolated ACï DC converter circuits is briefly discussed below.

3.1.1 Modeling of AC-DC Converters

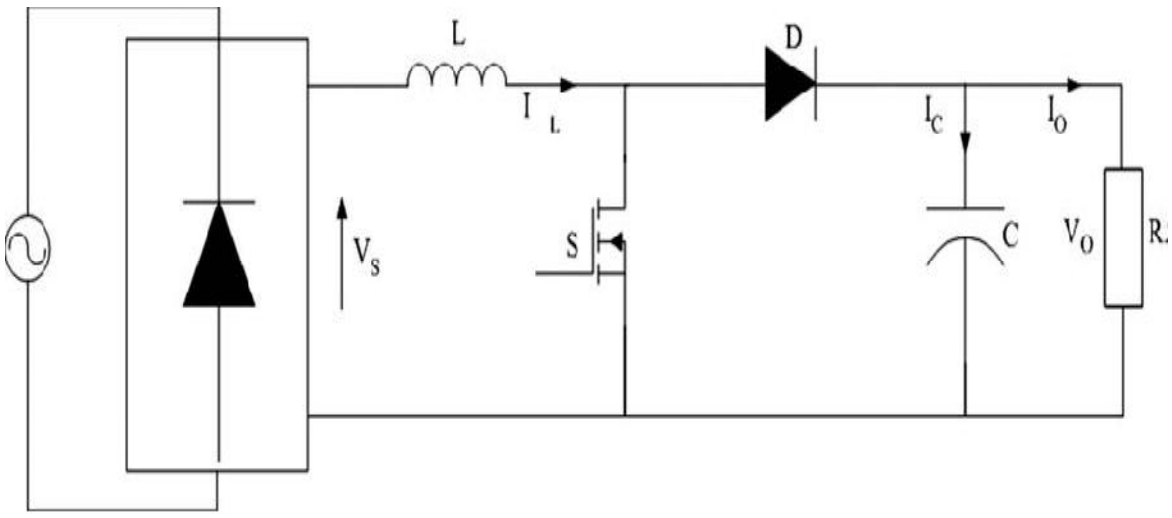


Figure 3.2: Circuit diagram of boost converter [30].

The boost converter regulates a higher DC voltage than input voltage. Circuit diagram of the boost converter is shown Figure 3.2.

The circuit operation can be divided into two modes. Mode 1 begins when switch is turned-on at t=0. The input current, which rises, flows through inductor L and switch S. Mode 2 begins when switch is turned-off at t=t1. The current flowing through the switch would now flow through L, C, load, and diode. The inductor current falls until switch is turned on again in the next cycle [30, 34]. The energy stored in inductor L is transferred to the load. During the turn-on time of switch S (S-on, D-off), characteristic equations of the circuit can be defined as follows [30]:

$$V_L = V_S \tag{3.1}$$

$$L\frac{dI_L}{dt} = V_S \tag{3.2}$$

$$\frac{dI_L}{dt} = \frac{V_S}{L} \tag{3.3}$$

$$I_C = -I_O \tag{3.4}$$

$$\frac{dV_C}{dt} = -\frac{V_C}{RC} \tag{3.5}$$

Where V_L, V_S are inductance voltage and rectified AC line voltage, respectively. Equation (3.3) shows the slope of the current as positive. In the same way, during the turn-off time of switch S (S-off, D-on) following equations are validated [30]:

$$V_L = V_S - V_C \tag{3.6}$$

$$\frac{dI_L}{dt} = \frac{V_S - V_C}{L} \tag{3.7}$$

$$I_C = I_L - \frac{V_C}{R} \tag{3.8}$$

$$\frac{dV_C}{dt} = \frac{I_L}{C} - \frac{V_C}{RC} \tag{3.9}$$

Where V_C is equal to the output voltage. Equation (3.4) shows the slope of the current as negative because the output voltage is bigger than rectified source voltage ($V_O > V_S$). The following equation determining the characteristic of inductance current is found by using equations (3.3) and (3.7) [30]:

$$\frac{dI_L}{dt} = \frac{V_S}{L} - (1-\beta)\frac{V_C}{L} \tag{3.10}$$

Where ɓ ∈ {0,1} and when the switch is turned-on (ɓ=1), equation (3.10) is equal to equation (3.3). At the other state of switch (ɓ=0), it is equal to equation (3.7). If the same operation is performed for equations (3.5) and (3.9), equation (3.11) determining the characteristic of capacitance voltage is found as follows [30]:

$$\frac{dV_C}{dt} = (1-\beta)\frac{I_L}{C} - \frac{V_C}{RC} \tag{3.11}$$

If equations (3.10) and (3.11) are written with the matrix form, the state space equation of the circuit is found as given in equation (3.12) [30].

$$\begin{bmatrix} \frac{dI_L(t)}{dt} \\ \frac{dV_C(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-\beta}{L} \\ \frac{1-\beta}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L(t) \\ V_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_S \tag{3.12}$$

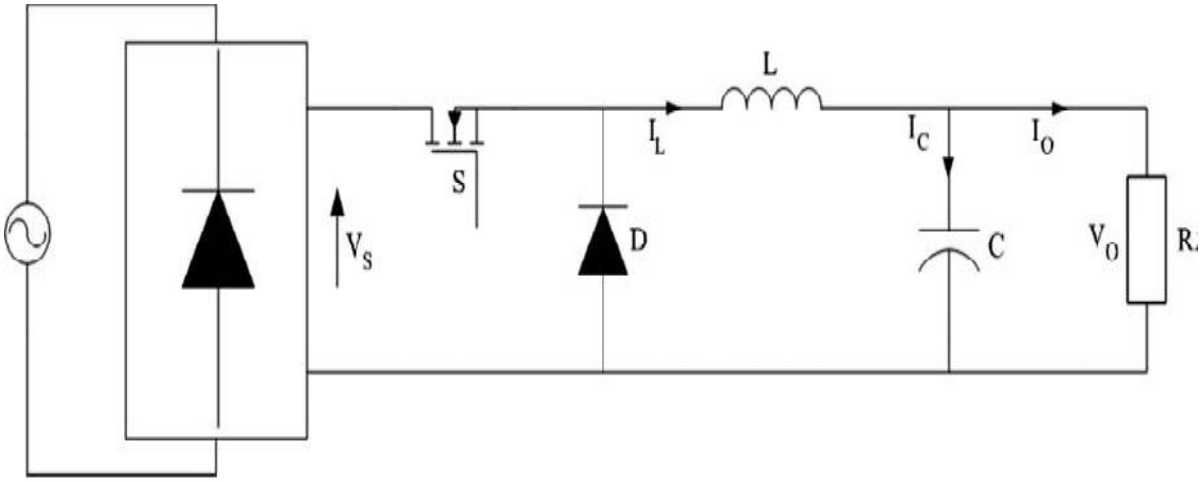


Figure 3.3: Circuit diagram of buck converter [30].

The buck or step-down converter regulates the average DC output voltage at a level lower than the input voltage [30, 34]. The circuit diagram of the buck converter is shown in Figure 3.3. After obtaining the current and voltage equations according to the S switchôs onï off position, state space equations of buck converter at matrix form are obtained as in the equation (3.13) [30].

$$\begin{bmatrix} \frac{dI_L(t)}{dt} \\ \frac{dV_C(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{1}{C} & \frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L(t) \\ V_C(t) \end{bmatrix} + \begin{bmatrix} \frac{\beta}{L} \\ 0 \end{bmatrix} V_S \qquad (3.13)$$

Where ß is defining the state of switch (ß {0,1}); *R*, *L*, *C* represents ohmic load, inductor, and capacitor values of the circuit, respectively. I_L is the inductor current and V_C is the capacitor voltage.

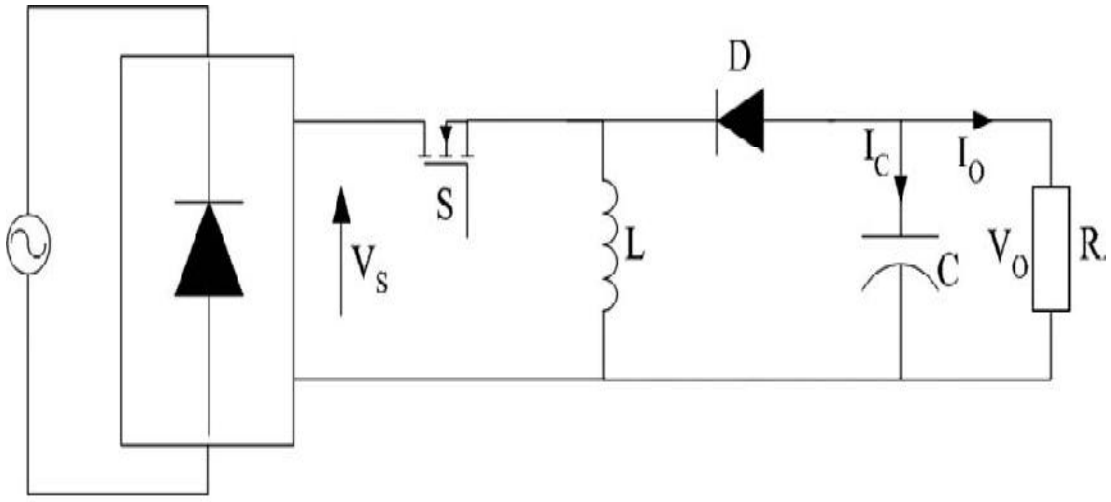


Figure 3.4: Circuit diagram of buckï boost converter [30].

The buckï boost converter regulates the average output DC voltage both lower and higher than the input voltage. The circuit diagram of the buckï boost converter is shown in Figure 3.4. In equation (3.14) the current and voltage state equations of buckï boost converter at matrix form are given [30].

$$\begin{bmatrix} \frac{dI_L(t)}{dt} \\ \frac{dV_C(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-\beta}{L} \\ \frac{1-\beta}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L(t) \\ V_C(t) \end{bmatrix} + \begin{bmatrix} \frac{\beta}{L} \\ 0 \end{bmatrix} V_S \qquad (3.14)$$

3.1.2 Modeling of the Open Loop System

The thyristor for PFC converter with different firing angles will give less output power, more harmonics and poor power factor as compared with Diode rectifier [13, 15, 22]. Hence, the diode rectifier is used as a dc input source to the Boost converter. The conventional boost converter circuit is shown in figure 3.5 [13].

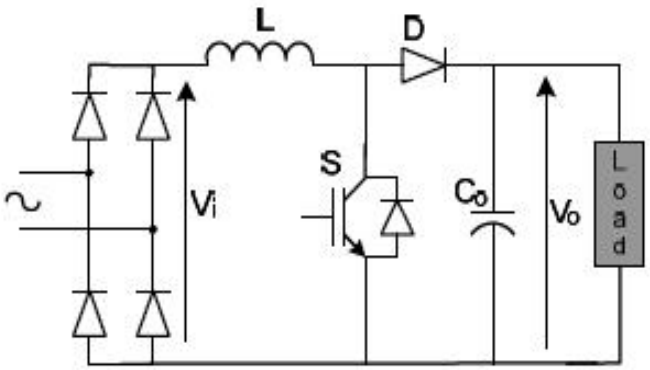


Figure 3.5: The conventional Boost Converter circuit [13].

The boost converter has Vi as the input voltage and Vo as the output voltage. Here, output voltage is greater than the input voltage. A large inductor L in series with the source voltage is essential. When the switch is on, the input current flows through the inductor and switch and the inductor stores the energy during this period. When the switch is off, the inductor current cannot die down instantaneously, this current is forced to flow through the diode and the load during this off period. As the current tends to decrease, polarity of the emf induced in L is reversed. As a result, a voltage across the load is the sum of supply voltage and inductor voltage and it is greater than the supply voltage. The voltage impressed across the inductor during on period is Vi. During this period, the current rises linearly from a minimum level I_1 to a maximum level I_2. Therefore the voltage across inductor is given in equation 1 [10, 36].

$$V_L = V_i \tag{3.15}$$

$$V_L = \frac{L(I_2 - I_1)}{T_{on}} = \frac{L(\Delta I)}{T_{on}} \tag{3.16}$$

From equations (3.15) and (3.16), equation (3.17) is derived [10].

$$T_{on} = \frac{L(\Delta I)}{V_i} \tag{3.17}$$

The voltage impressed across the inductor during off period is (Vo ï Vi) and the current drops linearly from the maximum level I_2 to the minimum level I_1. Therefore the voltage across the inductor is given in equation (3.18) [10].

$$V_L = V_O - V_i \tag{3.18}$$

$$V_L = \frac{L(I_2 - I_1)}{T_{off}} = \frac{L(\Delta I)}{T_{off}} \tag{3.19}$$

From equations (3.18) and (3.19), equation (3.20) is resulted [10].

$$T_{off} = \frac{L(\Delta I)}{(V_O - V_i)} \tag{3.20}$$

From equation (3.17), equation (3.21) is derived [10].

$$L(\Delta I) = T_{on} \cdot V_i \tag{3.21}$$

From equation (3.20), equation (3.22) is obtained [10].

$$L(\Delta I) = T_{off} \cdot (V_O - V_i) \tag{3.22}$$

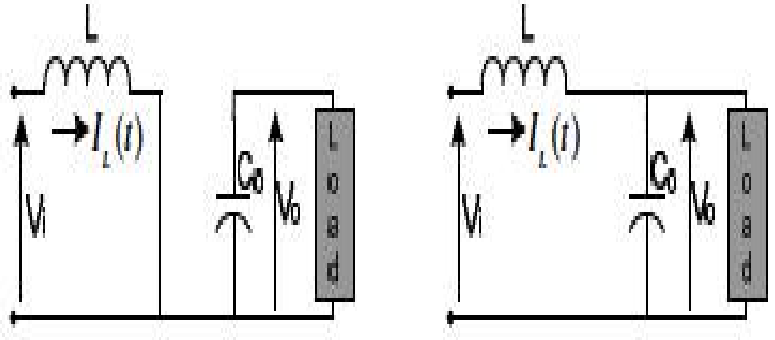
From equations (3.21) and (3.22), the following equations are derived [10, 36].

$$T_{on} \cdot V_i = T_{off} \cdot (V_O - V_i) \tag{3.23}$$

$$V_O = \frac{(T_{on} + T_{off}) \cdot V_i}{T_{off}} = \frac{T \cdot V_i}{T_{off}} = \frac{V_i}{(1-\alpha)} \qquad (3.24)$$

Where Ŭ=Ton/T is delay angle or the duty cycle of the boost converter. As firing angle increase from 0 to 1, the output voltage ideally increases from Vi to infinity. Hence, the output voltage is boosted [10, 36].

The boost converter, operating in the continuous conduction mode (CCM), depending on the position of the switch S has two operating mode as shown in figure 3.6 (a) and (b) [13].



(a) (b)

Figure 3.6: Boost converter operating modes [13] (a) switch is on and (b) switch is off

The open loop mathematical model for simulation studies can be easily derived by applying Kirchhoffôs voltage law, including the parasitic elements R_L and R_C , for these two operating modes as shown below [13]. When the switch is in on position, shown in figure 3.6 (a), the dynamics of the circuit are given below:

$$\frac{dI_L(t)}{dt} = \frac{1}{L}(V_i - I_L(t)R_L) \qquad (3.25)$$

$$\frac{dV_C(t)}{dt} = -\frac{V_O}{CR_C} \tag{3.26}$$

When the switch is in off position, shown in figure 3.6 (b), the dynamics of the circuit are given below [13]:

$$\frac{dI_L(t)}{dt} = \frac{1}{L}(V_i - I_L(t)R_L - V_O) \tag{3.27}$$

$$\frac{dV_C(t)}{dt} = \frac{1}{C}(I_L(t) - \frac{V_O}{R_C}) \tag{3.28}$$

Using the above equations capacitor voltage Vc(t) and output voltage Vo(t) are related via the following equation [13]:

$$V_O(t) = R_C C\frac{dV_C(t)}{dt} + V_C(t) \tag{3.29}$$

Due to inherent switching operation, AC-DC converters periodically switch between the subsystems, each subsystem described by the separate set of equations as given above. Therefore, it is difficult to obtain accurate model of the converters for the transient analysis and control design. The technique called average-value model, wherein the effects of fast switching are neglected, provides a solution to this problem. The transfer function is obtained from small signal model around the nominal operating point [13, 32]. When the switch is in on position, dynamics of the inductance current is given below [13]:

$$\frac{dI_L(t)}{dt} = \frac{V_i}{L} - \frac{R_L I_L(t)}{L} \tag{3.30}$$

And its Laplace form is given as follows [13]:

$$I_L(s) = \frac{V_i(s)}{sL + R_L} \tag{3.31}$$

The average value of the inductance current for the switch in off position is given below [13]:

$$I_{Lave}(t) = \frac{T_{off}}{T} I_L(t) = \frac{T(1-d)}{T} I_L(t) = (1-d) I_L(t) \tag{3.32}$$

$$I_{Lave}(t) = (1-d) \frac{V_i(s)}{sL + R_L} \tag{3.33}$$

The output voltage is given as follows [13]:

$$V_O(t) = \frac{1}{C} \int I_{Lave}(t) dt \tag{3.34}$$

$$V_O(s) = \frac{1}{sC} I_{Lave}(s) \tag{3.35}$$

When the equation (3.33) written in equation (3.35) the transfer function of the system can be derived as given below [13].

$$G(s) = \frac{V_O(s)}{(1-d)} = \frac{V_i(s)}{sC(sL + R_L)} \tag{3.36}$$

The open-loop block diagram of the system is shown below in figure 3.7 [13].

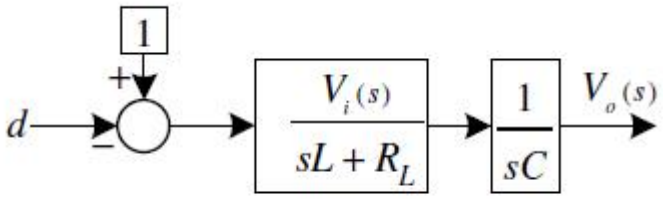


Figure 3.7: The open loop block diagram of boost PFC converter [13].

3.2 Boost PFC Converter Design

A 4 KW Boost PFC converter is designed with the following power stage specifications:

- Input voltage: 220 V ac single phase
- Output voltage: 400V
- Output power: 4000 W
- ɖ(efficiency of the converter)=0.95

For boost PFC converter PF is assumed to be 0.99 or greater. Maximum input power can be calculated assuming a nominal efficiency of the converter to be 0.95 [37].

$$P_{IN(MAX)} = \frac{P_{O(MAX)}}{\eta} = \frac{4000W}{0.95} = 4210.53W \qquad (3.37)$$

The maximum rms AC line current is calculated as [37]:

$$I_{IN(RMS)MAX} = \frac{P_{O(MAX)}}{\eta \cdot V_{IN(RMS)} \cdot PF} \qquad (3.38)$$

$$I_{IN(RMS)MAX} = \frac{4000W}{0.95 \cdot 220V \cdot 0.998} = 19.18A \tag{3.39}$$

Assuming sinusoidal AC current, the peak value of the AC current can be calculated as follows [37]:

$$I_{IN(PK)MAX} = \frac{\sqrt{2} \cdot P_{IN(MAX)}}{V_{IN(RMS)}} \tag{3.40}$$

$$I_{IN(PK)MAX} = \frac{\sqrt{2} \cdot 4210.53W}{220V} = 27.07A \tag{3.41}$$

Power switch duty cycle (D) must be determined using input rms voltage. The peak input voltage is used for boost inductor calculation [37].

$$V_{IN(PK)} = \sqrt{2} \cdot V_{IN(RMS)} = \sqrt{2} \cdot 220V = 311V \tag{3.42}$$

$$D = \frac{V_O - V_{IN(RMS)}}{V_O} = \frac{400V - 220V}{400V} = 0.45 \tag{3.43}$$

The ripple current (æI_L) is assumed to 20% of the peak input current. The ripple current and the peak inductor current are given as follows [37]:

$$\Delta I_L = 0.2 \times I_{IN(PK)MAX} = 0.2 \times 27.07A = 5.41A \tag{3.44}$$

$$I_{L(PK)MAX} = I_{IN(PK)MAX} + \frac{\Delta I_L}{2} = 27.07A + \frac{5.41A}{2} = 29.78A \tag{3.45}$$

Finally the boost inductor is designed as follows (assuming the switching frequency is about 20 kHz) [37]:

$$L_{BST} = \frac{8 \times V_{IN(PK)} \times D}{f_{SW} \times \Delta I_L} = \frac{8 \times 311V \times 0.45}{20kHz \times 5.41} = 10.34mH \quad (3.46)$$

So the boost inductor is chosen to be 10mH.

Output Capacitor design in PFC converters is typically based on hold up time requirements. For such applications the holdup time (æt) can be taken to be around 30ms [24, 37]. Taking the minimum input rms voltage to be 190V (13% deviation) the minimum output capacitance is given below [37]:

$$C_{OUT} \geq \frac{\frac{1}{2} \cdot P_O \cdot \Delta t}{V_{IN(RMS)}^2 - V_{IN(RMS)MIN}^2} \quad (3.47)$$

$$C_{OUT} \geq \frac{\frac{1}{2} \cdot 4000W \cdot 30ms}{220V^2 - 190V^2} \quad (3.48)$$

$$C_{OUT} \geq 4878\,\mu F \quad (3.49)$$

Hence the output capacitance can be taken to be 5000εF. The boost converter design is complete with L=10mH and C=5000εF. The design of the boost PFC converter is summarized in the following table (table 3.1).

Input rms voltage $V_{IN(RMS)}$	220V
Input peak voltage $V_{IN(PK)}$	311V
Maximum input rms current $I_{IN(RMS)MAX}$	19.18A
Maximum input peak current $I_{IN(PK)MAX}$	27.07A
Ripple current æI_L	5.41A
Maximum inductor peak current $I_{L(PK)MAX}$	29.78A
Maximum input power $P_{IN(MAX)}$	4210.53W
Output voltage V_O	400V
Output power P_O	4000W
Boost inductor L_{BST}	10mH
Output capacitor C_{OUT}	5000ε F

Table 3.1: Design summary of the boost PFC converter

CHAPTER 4

DESIGN OF AVERAGE CURRENT MODE DIGITAL CONTROLLER

4.1 Average Current Mode Control

Digital control of a boost PFC converter based on average current mode control is illustrated in Fig 4.1. In the outer voltage loop, the output voltage is sensed and compared with the voltage reference. The error becomes the input to the voltage proportional-integral (PI) controller. The output of this PI controller is the scaling factor for the rectified voltage that is used as one of the inputs to the multiplier. The product of the scaling factor and the rectified voltage is the current reference, i_{ref}. The inner current loop implements average current mode control to force the average inductor current to follow the reference current [12, 24, 33].

In digital implementation for average current mode control, multiplication and division operations are implemented by the software. Because all the calculations, including multiplication and division, are executed in every switching period, the implementation requires a high speed digital controller.

The processes in a digital control PFC based on average current mode control include: output voltage samples, voltage error calculation, voltage PI controller, reference current controller (including multiplication), current error calculation, current PI controller and duty cycle calculations. Because this process is iteratively running in every switching cycle, a high performance digital controller is needed [24].

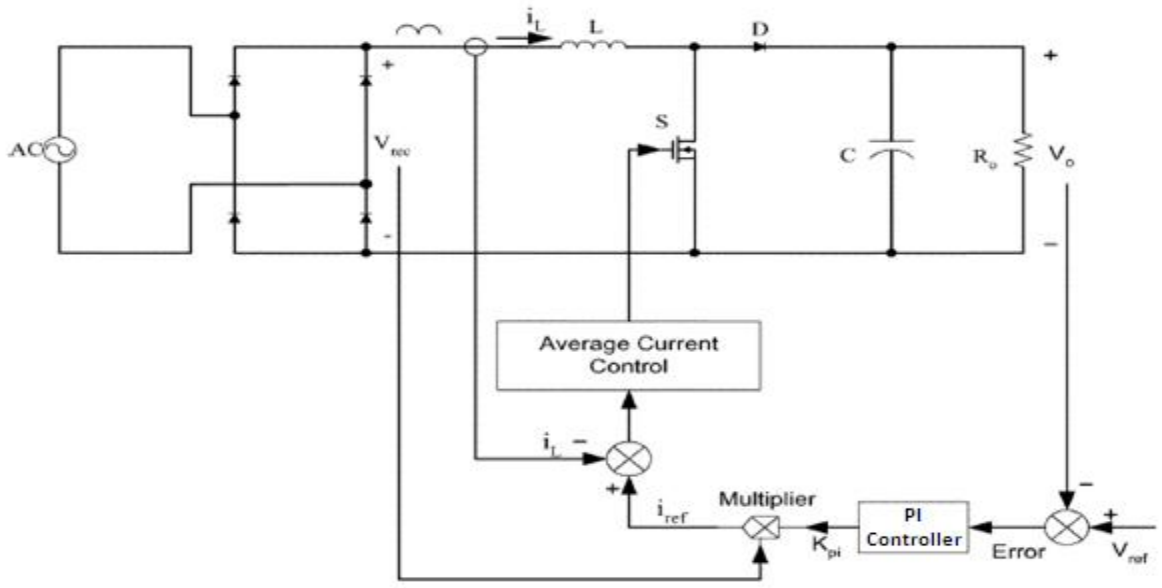


Figure 4.1: Average current mode control of Boost PFC Converter [16].

4.2 Modeling of the Digital Controller

Figure 4.2 shows the digital control structure (average current mode control) with various sensor gains [33].

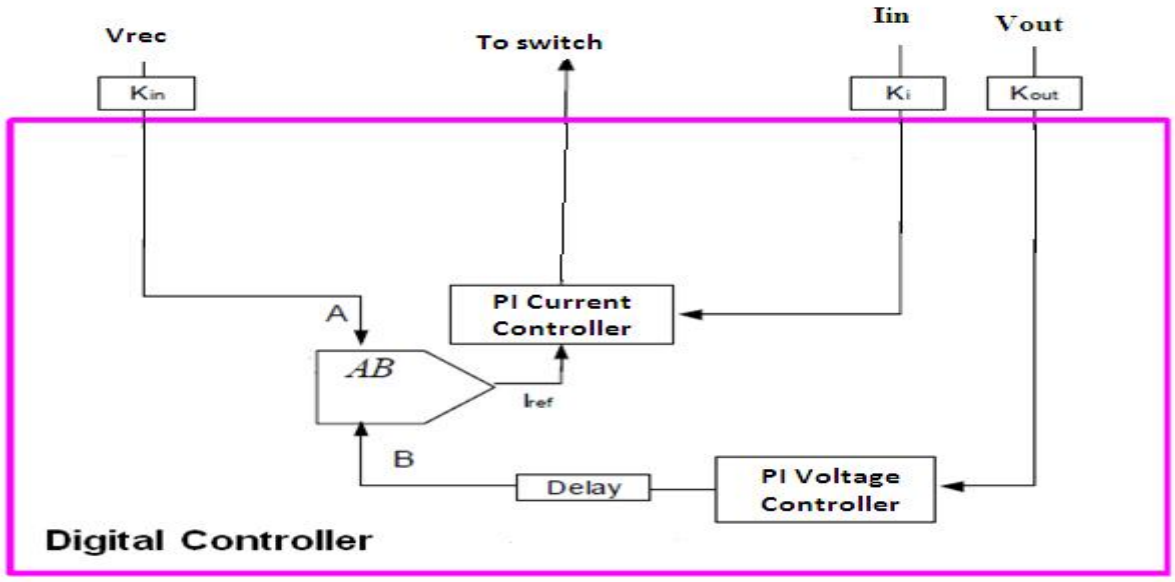


Figure 4.2: Digital control structure of boost PFC converters [33].

4.2.1 Current Loop Modeling

The function of the current controller is to force the current to track the current reference that is given by the multiplier and which has the same shape as the input voltage. So the current loop bandwidth must be higher than the reference bandwidth. For faithfully tracking a semi-sinusoidal waveform of 100Hz, the bandwidth of the current loop is usually set to 2-10KHz [19, 33]. A small-signal equivalent circuit of the current loop is shown in Figure 4.3.

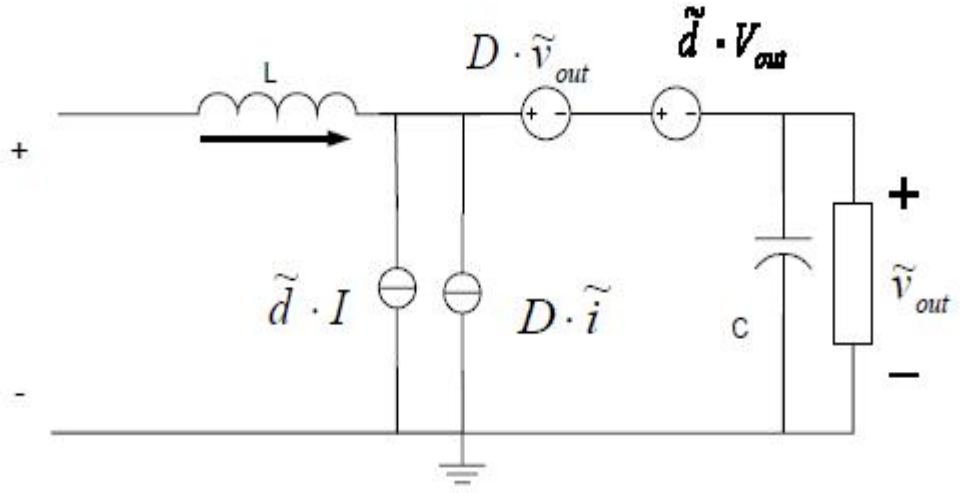


Figure 4.3: Small-signal model of current loop [33].

The power stage small-signal duty-to-current transfer function is derived to be as follows [33]:

$$G_{id}(s) = \frac{\tilde{i}}{\tilde{d}} = \frac{2V_{out}}{R_L(1-D)^2} \cdot \frac{1+\frac{sR_LC}{2}}{1+\frac{sL}{R_L(1-D)^2}+\frac{s^2LC}{(1-D)^2}} \qquad (4.1)$$

For s=jɤ , when ɤ is large enough, the high frequency approximation can be derived as follows [33]:

$$G_{id}(s) = \frac{\tilde{i}}{\tilde{d}} \approx \frac{V_{out}}{Ls} \qquad (4.2)$$

Where L is boost inductance, C is output capacitor, R_L is load resistor, D is duty cycle and V_{out} is the output voltage.

4.2.2 Feed-forward Loop Modeling

The current reference is given by equation (4.3) [33].

$i_{ref} = A*B$ (4.3)

Where $A=K_{in}*V_{in}$ (K_{in} is the input voltage gain) and $B=V_c$ (V_c is the voltage controller output).

Assume the inductor current tracks the reference perfectly. The input current is proportional to the input voltage, which means the voltage loop can be affected by input voltage variation. The feed-forward loop is inserted to compensate the line voltage variation [11, 33].

4.2.3 Voltage Loop Modeling

Assume the input current is perfectly controlled and tracks the input voltage. Then the following equation can be written [33].

$I_{in}=K*V_{in}*V_c$ (4.4)

$$K = \frac{K_{in}}{(K_{ff}V_{in\_rms})^2} \qquad (4.5)$$

Where K_{in} is the input voltage gain, K_{ff} is the feed-forward gain and V_c is voltage controller output. For P_{in} being approximately equal to P_{out} the following equations are written [33].

$$i_{in}v_{in} = i_o v_{out} \tag{4.6}$$

$$Kv_{in}^{2}v_c = i_o v_{out} \tag{4.7}$$

Using small-signal perturbation method, the following linearized equation is obtained [33].

$$\tilde{i}_o = \frac{2KV_C V_{in}}{V_{out}}\tilde{v}_{in} + \frac{KV_{in}^{2}}{V_{out}}\tilde{v}_c - \frac{KV_{in}^{2}V_C}{V_{out}^{2}}\tilde{v}_{out} \tag{4.8}$$

Where V_c, V_{in}, V_{out} are steady state values, and $\tilde{v}c$, $\tilde{v}in$, $\tilde{v}out$, are small signal perturbations. A low-frequency small-signal model is developed to design voltage controller, as shown in Figure 4.4.

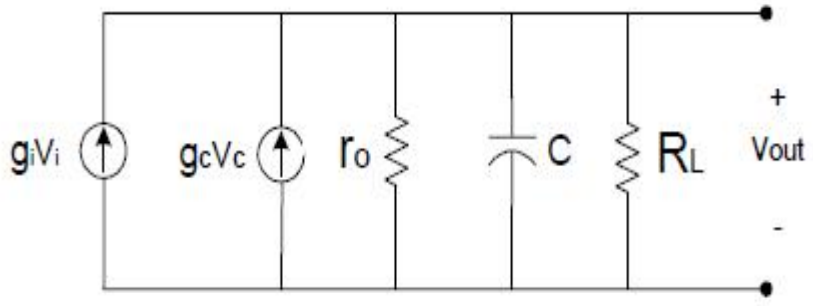


Figure 4.4: Low-frequency Small-Signal Model for voltage loop [33].

In Figure 4.4, the constants are given as follows [19, 33].

$$g_c = K\frac{V_{in\_rms}^{\ 2}}{V_{out}} \tag{4.9}$$

$$g_i = K\frac{2V_{in}V_C}{V_{out}} \tag{4.10}$$

$$r_o = \frac{V_{out}}{I_{out}} \tag{4.11}$$

Finally, from the small-signal model, the control to output voltage transfer function is derived to be as follows [33].

$$G_V = \frac{\tilde{v}_{out}}{\tilde{v}_C} = \frac{g_C}{Cs} \tag{4.12}$$

4.3 Digital Controller Design in Z-domain

The simplest method to implement digital control is to convert an analog controller into a digital controller. There are many conversion methods, such as ñbackward integral,ò ñTustinò and ñzero and pole matchingò. However, it is difficult to model sample and hold, $G_H(s)$ and computation delay $e^{-Tdelay}$ in s domain [20].

Designing an analog controller may not be accurate. Even with an accurate analog controller, converting it into a discrete form may compromise its performance. Alternatively, the digital controller is designed directly in z-domain employing the relation of z variable and s variable [33]:

$$z = e^{sT_s} \tag{4.13}$$

Where T_S is the sampling cycle. The frequency response of a digital system G(z) can be represented as shown in equation (4.15). The magnitude response and the phase response are given in equations (4.16) and (4.17) respectively [33].

$$G(z) = k\frac{(z-\xi_1)\cdots(z-\xi_m)}{(z-\rho_1)\cdots(z-\rho_n)} \tag{4.14}$$

$$G(e^{j\omega T_s}) = k\frac{(e^{j\omega T_s}-\xi_1)\cdots(e^{j\omega T_s}-\xi_m)}{(e^{j\omega T_s}-\rho_1)\cdots(e^{j\omega T_s}-\rho_n)} \tag{4.15}$$

$$\left|G(e^{j\omega T_s})\right| = k\frac{\prod_{i=1}^{m}\left|e^{j\omega T_s}-\xi_i\right|}{\prod_{j=1}^{n}\left|e^{j\omega T_s}-\rho_j\right|} \tag{4.16}$$

$$\angle G(e^{j\omega T_s}) = \sum_{i=1}^{m}\angle(e^{j\omega T_s}-\xi_i) - \sum_{j=1}^{n}\angle(e^{j\omega T_s}-\rho_j) \tag{4.17}$$

These responses are directly related to the position of zeros and poles on the z-plain as shown in Figure 4.5. Particularly, the computation delay $e^{-TdelayS}$ can be mapped into the origin as $Z^{-Tdelay/Ts}$.

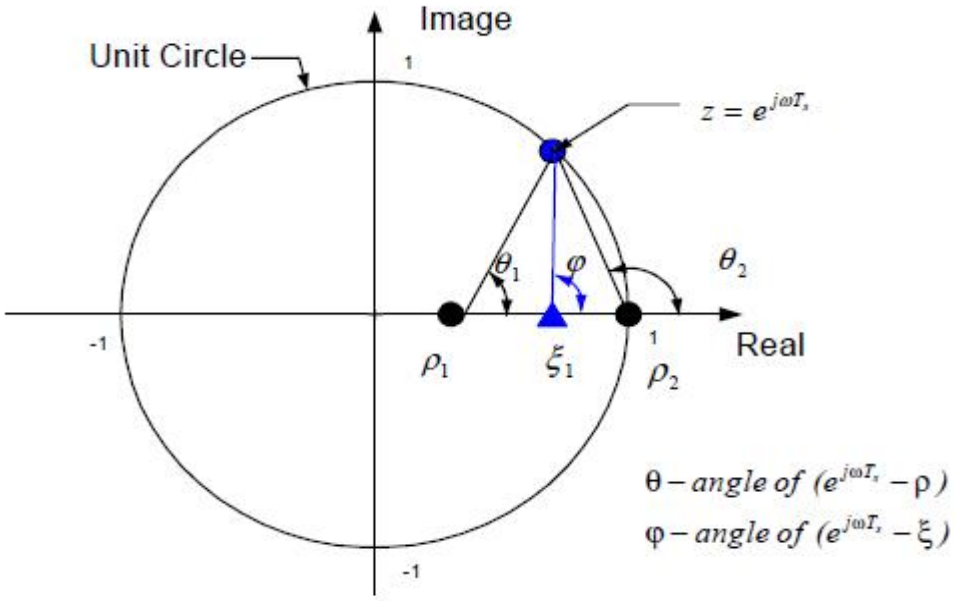


Figure 4.5: Poles and zeros in the z-plane [33].

In this approach the controller is designed by placing the poles and zeros in z-plane to stabilize the converter and achieve the power factor correction. Before the controller is designed, proper model of power stage must be obtained.

4.3.1 Discrete Time Model of Power Stage with Sample-and-Hold

If e(*t*) is the impulse response of system G, the Laplace transformation of a sampled signal, e*(*t*), is given as follows [33].

$$E^*(s) = \sum_{n=0}^{\infty} e(nT)e^{-nT_s} = \sum_{poles}[residue\ of\ E(\lambda)\frac{1}{1-e^{-T_s(s-\lambda)}}] \qquad (4.18)$$

Where E*(*s*) is the Laplace transformation of e* (*t*). Combined with the sample-and-hold function the following relation is obtained [9, 33].

$$E^*(s) = [\sum_{n=0}^{\infty} e(nT)e^{-nT_s}]\frac{1-e^{-T_s s}}{s}$$
$$= \sum_{poles}[residue\ of\ E(\lambda)\frac{1}{1-e^{-T_s(s-\lambda)}}\cdot\frac{(1-e^{-T_s\lambda})}{\lambda}] \qquad (4.19)$$

The power stage can be digitized using the zero-order-hold method with assumed sampling frequency of 20 KHz, as shown in Figure 4.6.

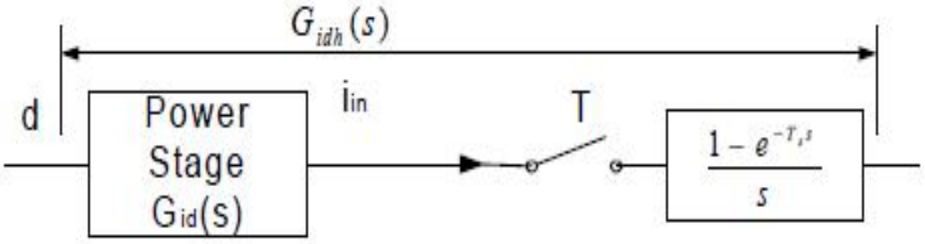


Figure 4.6 Power stage with sample and hold [33].

From Figure 4.6 and from equation (4.2) the discrete duty to current transfer function is derived to be as given in equation (4.20) [9, 33].

$$G_{idz}(z) = \frac{V_{out}}{L}\cdot\frac{T_S}{(z-1)} \qquad (4.20)$$

Where the sampling period is Ts= 50εs. Figure 4.7 shows the duty to current discrete transfer function in the z-plane.

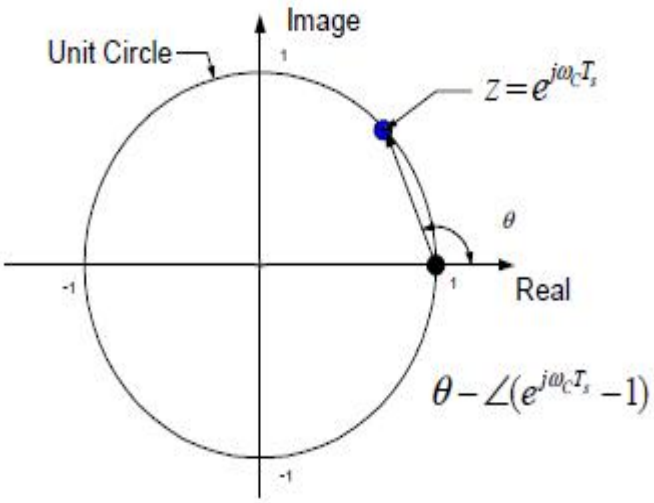


Figure 4.7: Duty to current transfer function mapped into z-plane [33].

Using the same method and equation (4.12) the discrete control to output transfer function is derived as given in equation (4.21) [9, 33].

$$G_{vz}(z) = \frac{g_C}{C} \cdot \frac{T_S}{(z-1)} \tag{4.21}$$

4.3.2 Current Controller Design

The current loop with digital controller is illustrated in Figure 4.8 [33].

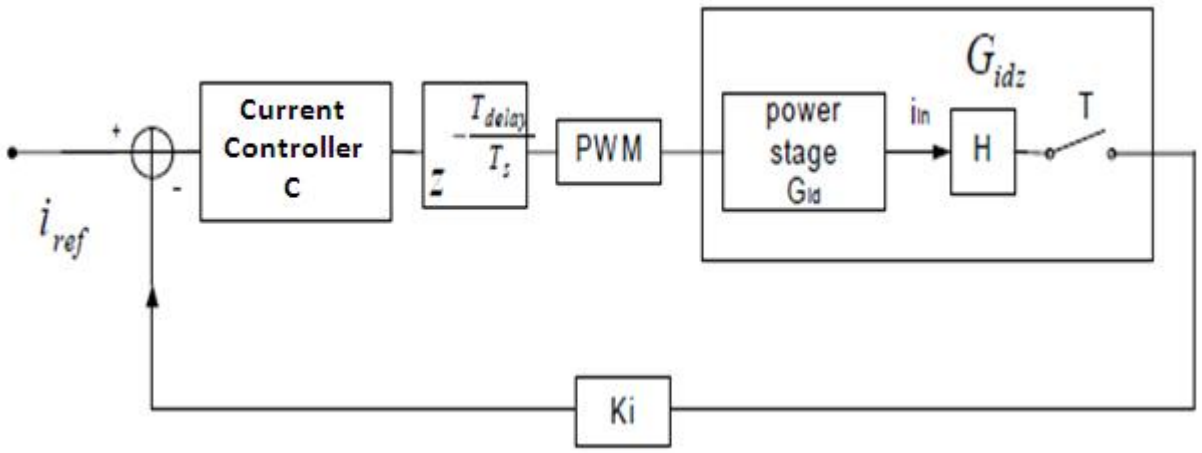


Figure 4.8 Current loop with digital compensator [33].

In the above figure the value Ki is the current feedback gain. The design target is so that, the phase margin is set to 45^o and for a faithful tracking of the semi sinusoidal waveform, the bandwidth is 8 KHz [10, 33]. The value of 45^o for the phase margin is a benchmark value for stability of the digital controller. The current controller is given in equation 4.22.

$$C(z) = K_P \frac{(z-\xi)}{(z-1)} \tag{4.22}$$

The current loop gain is given as follows [33].

$$\begin{aligned} T_C(z) &= G_{idz}(z) \cdot C(z) \cdot Ki \cdot z^{-\frac{T_{delay}}{T_s}} \\ &= \frac{V_{out} \cdot T_s}{L(z-1)} \cdot \frac{K_P(z-\xi)}{z-1} \cdot K_i \cdot z^{-\frac{T_{delay}}{T_s}} \end{aligned} \tag{4.23}$$

The two design targets, magnitude of the current loop gain and phase margin are used to determine two unknown variables, gain *Kp* and zero ξ, as shown below.

$$\begin{cases} \left|T_C(e^{j\omega_c T_s})\right| = 1 \\ \angle T_C(e^{j\omega_c T_s}) = -180^0 + 45^0 \end{cases} \quad (4.24)$$

Where $\omega_c = 2\pi f_c = 2\pi * 8$krad/sec, Vout=400V, L=10mH, Ki(current feedback gain)=0.0725, T_{delay}=10εs and Ts=50μs. Solving equation (4.24) the value of gain *Kp* and zero ξ are determined as given below.

$$\begin{cases} Kp = 50 \\ \xi = 0.8 \end{cases} \quad (4.25)$$

Hence, the controller transfer function is given in equation (4.26). Changing this into continuous s-domain (using d2c function of MATLAB) equation (4.27) is resulted.

$$C(z) = \frac{50(z-0.8)}{z-1} \quad (4.26)$$

$$C(s) = \frac{50s+100}{s} \quad (4.27)$$

Hence a PI current controller is designed with the gains Kp=50 and Ki=100 based on the design target.

4.3.3 Voltage Controller Design

The voltage loop is shown in Figure 4.9 [33].

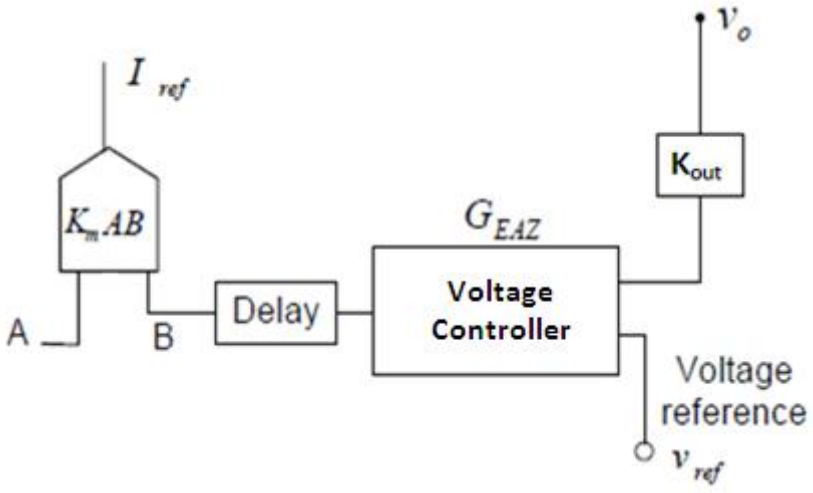


Figure 4.9: Outer voltage loop [33].

The discrete transfer function of the voltage controller is given in equation (4.28). The voltage open loop gain is given in equation (4.29) [10, 33].

$$G_{EAZ}(z) = \frac{K_P(z-\xi)}{z-1} \tag{4.28}$$

$$T_V = G_{VZ} \cdot k_{out} \cdot G_{EAZ} \cdot z^{-\frac{Tdelay}{Ts}} \tag{4.29}$$

The two design targets, the magnitude of the current loop gain and phase margin are used to determine two unknown variables gain *Kp* and zero ξ as shown below [33].

$$\begin{cases} \angle T_v(e^{-j\omega_c T_s}) = -180^\circ + 45^\circ \\ \left|T_v(e^{-j\omega_c T_s})\right| = 1 \end{cases} \tag{4.30}$$

Where T_{delay}=10µs, T_s=50µs, K_{out}=0.002(output voltage sensing gain), C=5000µF. The voltage controller parameters are found to be as given in equation (4.31). The voltage controller is given in equation (4.32).

$$\begin{cases} Kp = 0.002 \\ \xi = -99 \end{cases} \tag{4.31}$$

$$G_{EAZ}(z) = \frac{0.002\,(z+99)}{z-1} \tag{4.32}$$

Changing this discrete function in to continuous s-domain (using d2c MATLAB function) the following result is obtained.

$$G_{EA}(s) = \frac{0.002\,s + 2}{s} \tag{4.33}$$

Hence a PI voltage controller is designed with the gains Kp=0.002 and Ki=2 based on the design targets.

CHAPTER 5

SIMULATION OF DIGITALLY CONTROLLED PFC CONVERTER

A PFC converter must provide a regulated DC output voltage under load variation and input voltage fluctuation. The control of the output voltage should be performed in a closed-loop manner using negative feedback. The three most common closed-loop control methods for PWM PFC converters are the voltage-mode control, the current-mode control and PFC control [30].

5.1 Voltage-Mode Control

Voltage-mode control is probably the most common way to control a power supply. In essence, an error voltage obtained from the difference between a reference voltage and a portion of the output voltage is continuously compared to a fixed frequency and amplitude saw-tooth. The crossing point between these two signals generates a transition on the comparatorôs output. When the output voltage deviates from its natural target, the error voltage *e* (error) increases [13, 30].

The voltage-mode control scheme is shown in Figure 5.1. The error amplifier produces a control voltage that is compared to a saw-tooth waveform. The comparator produces a pulse width modulation (PWM) signal fed to drivers of controllable switches in the PFC converter [31].

The duty ratio of the PWM signal depends on the value of the control voltage. The frequency of the PWM signal is the same as the frequency of the saw-tooth waveform. An important advantage of the voltage-mode control is in its simplicity and flexibility [26, 31].

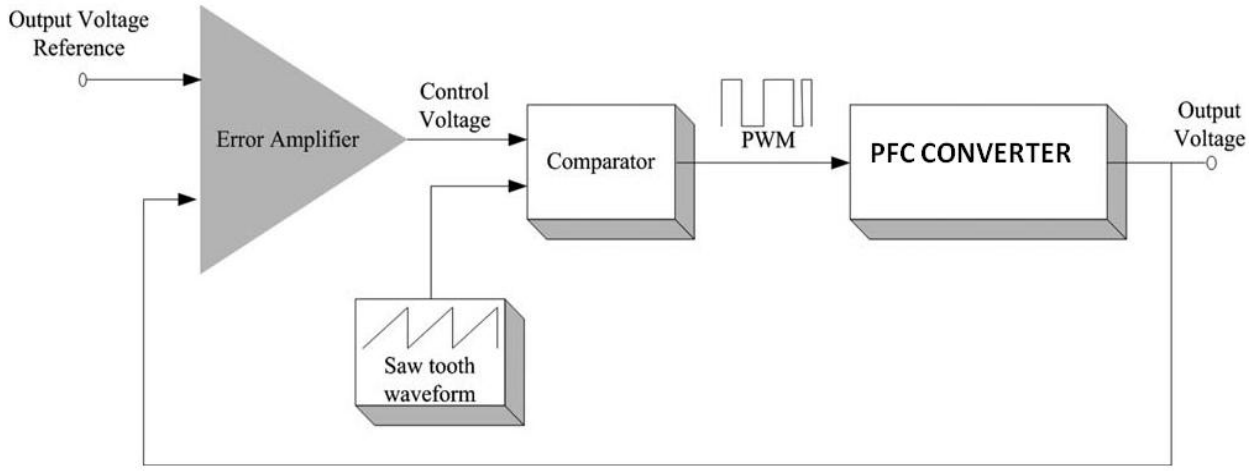


Figure 5.1: Voltage-mode control scheme [30].

The advantages of voltage-mode control are given as follows [30]:

(1) A single feedback loop is easier to design and analyze.

(2) A large-amplitude ramp waveform provides good noise margin for a stable modulation process.

(3) A low impedance power output provides better cross regulation for multiple output supplies.

Voltage-modeôs disadvantages can be listed as [30]:

(1) Any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slow response.

(2) The output filter adds two poles to the control loop requiring either a dominant-pole low frequency roll-off at the error amplifier or an added zero in the compensation.

(3) Compensation is further complicated by the fact that the loop gain varies with input voltage.

The voltage mode controller for boost PFC converter is simulated using MATLAB-Simulink. The circuit parameters are given below:

Vs(peak)=311V, Vs(rms)=220V, f(line)=50Hz, L=10mH, C=5000ε F, R-load=40Ý, Vout=400V, Pout=4000W.

For voltage PI controller Kp=0.0007 and Ki=0.09. (For this controller Kp and Ki are obtained using the trial and error method.)

Figure 5.2 shows the MATLAB simulink model for the boost converter with the voltage mode controller. Figure 5.3 and figure 5.4 shows the MATLAB simulink model of the boost converter and the voltage mode controller respectively.

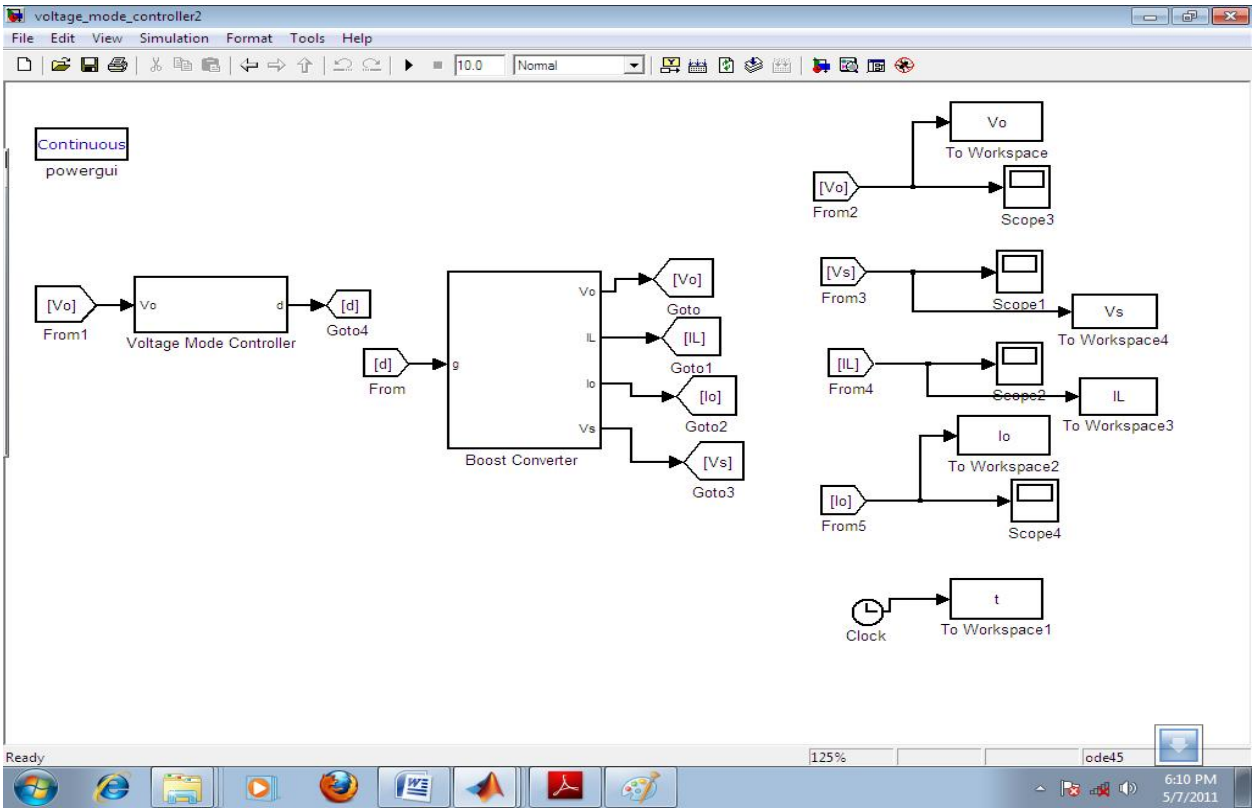


Figure 5.2: MATLAB model of the PFC converter with voltage mode controller

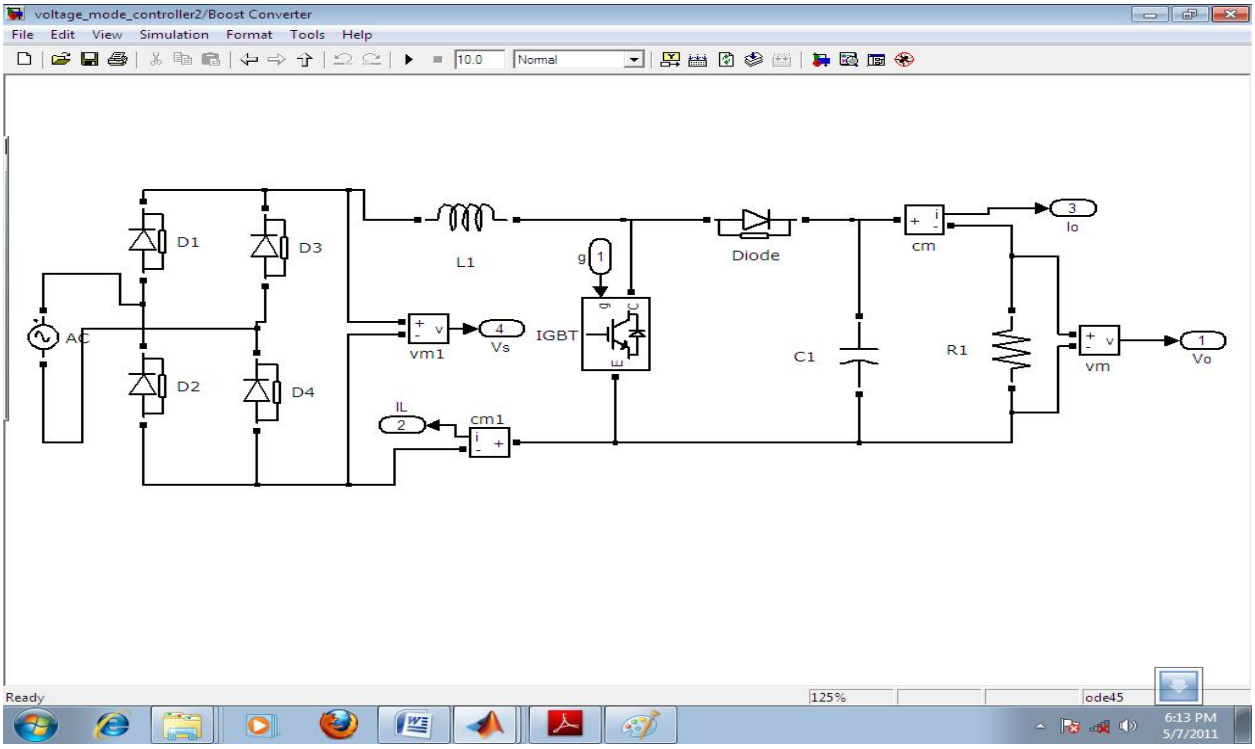


Figure 5.3: MATLAB model of the boost converter

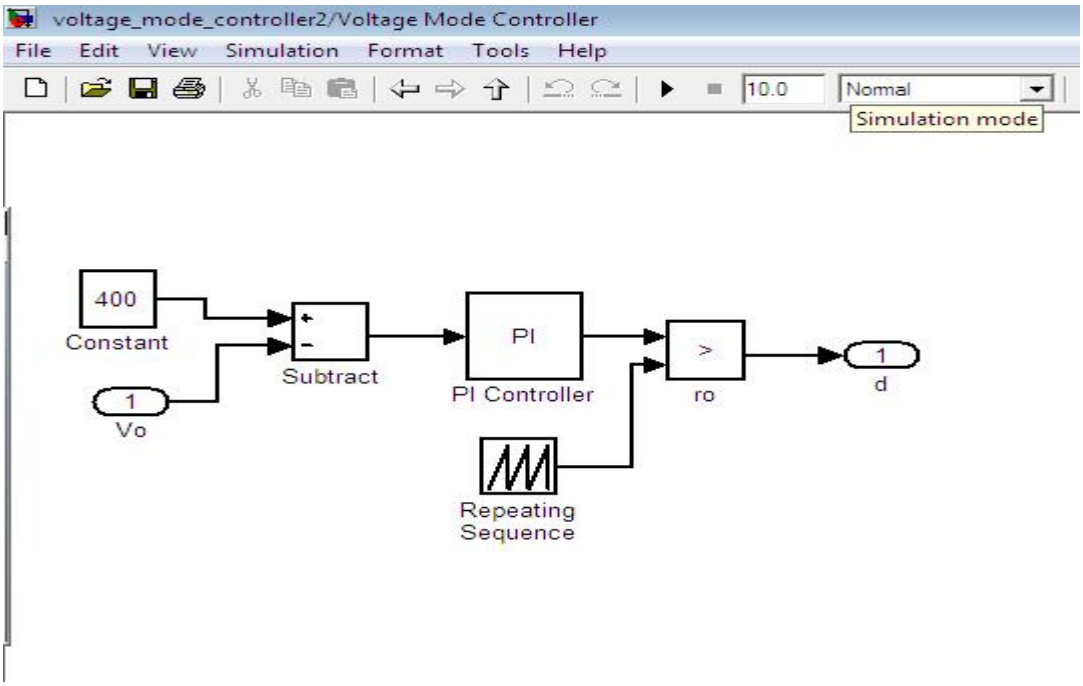


Figure 5.4: MATLAB model of the voltage mode controller

The following figures show the results of simulation. Figure 5.5 and 5.6 show the output voltage and the output current respectively. Figure 5.7 shows the rectified input voltage and the inductor (input) current on the same plot.

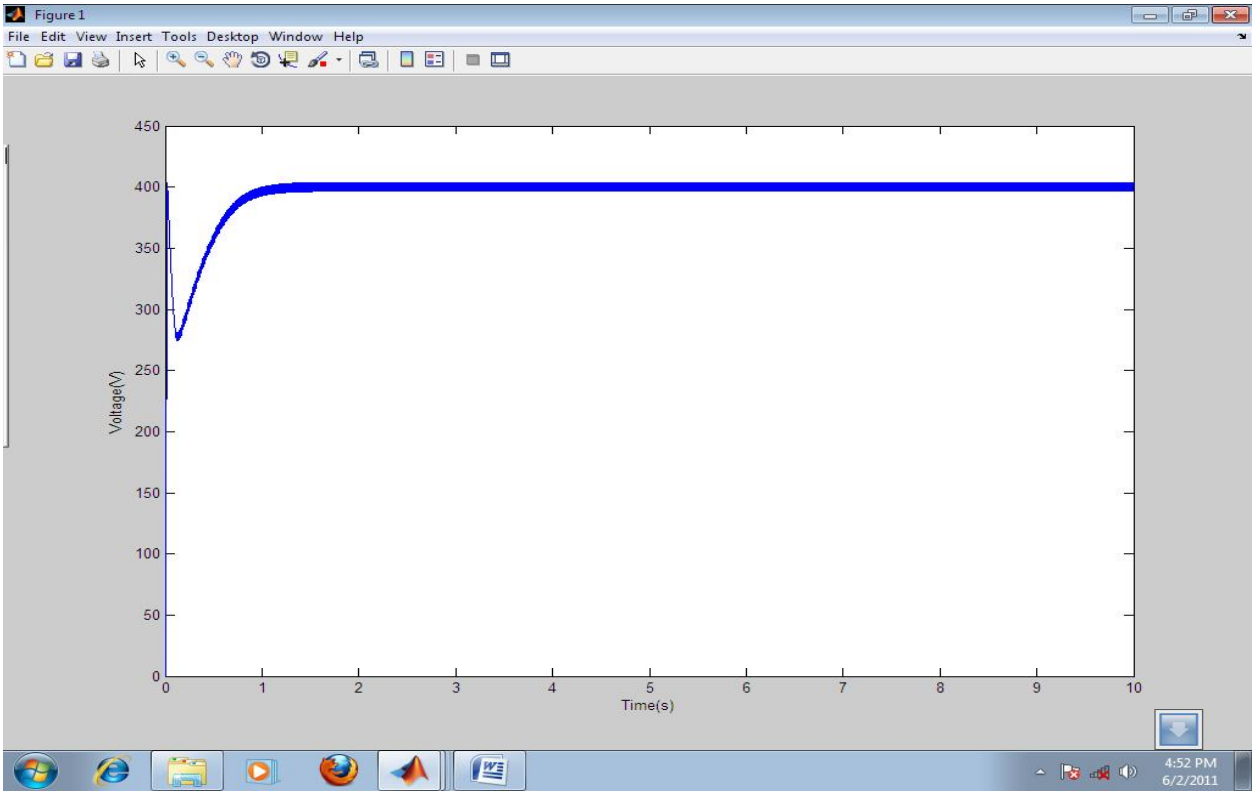


Figure 5.5: The output voltage of the voltage mode controlled converter

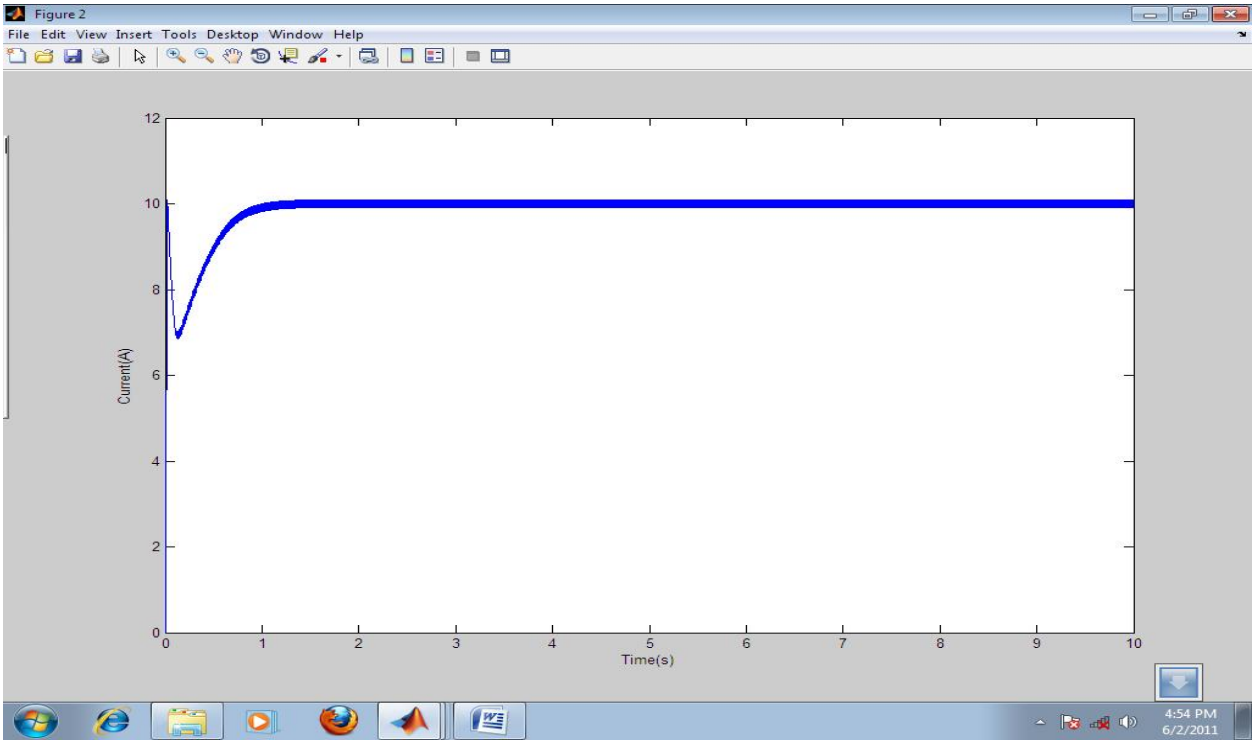


Figure 5.6: The output current of the voltage mode controlled converter

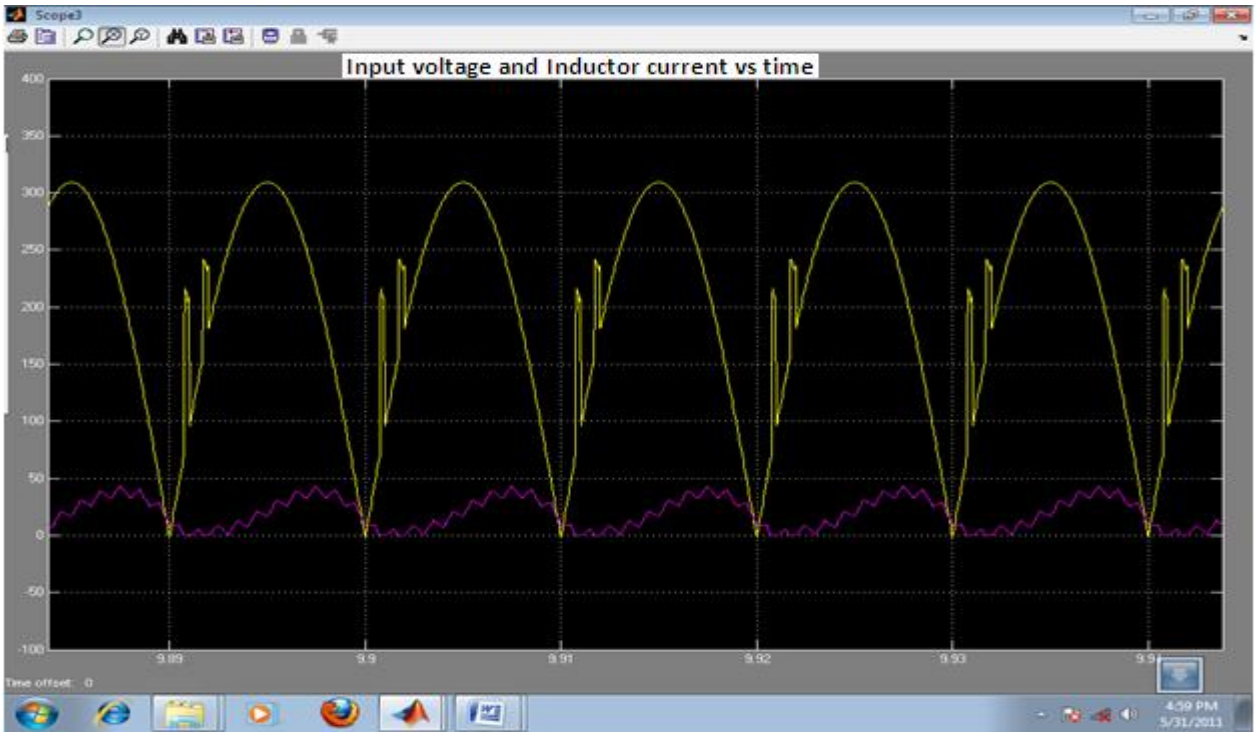


Figure 5.7: The rectified input voltage (upper) and inductor current (lower) of the voltage mode controlled converter

The output voltage and output current are obtained as desired. The output voltage is controlled to the 400V level. The output power is 4KW as desired. The inductor current is in phase with the input voltage waveform but it contains significant amount of ripple. This is the major disadvantage of the voltage mode controller.

5.2 Current-Mode Control

The current-mode control scheme is presented in Figure 5.8. Note that the peak inductor (switch) current is proportional to the input voltage. Hence, the inner loop of the current-mode control naturally accomplishes the input voltage-feed forward technique. The inner control loop feedbacks an inductor current signal. After then, a voltage converted from this current signal is compared to the control voltage. This modification of replacing the triangular waveform of the voltage-mode control scheme by a converter current signal significantly alters the dynamic behavior of the converter which takes on some characteristics of a current source [26, 28, 30].

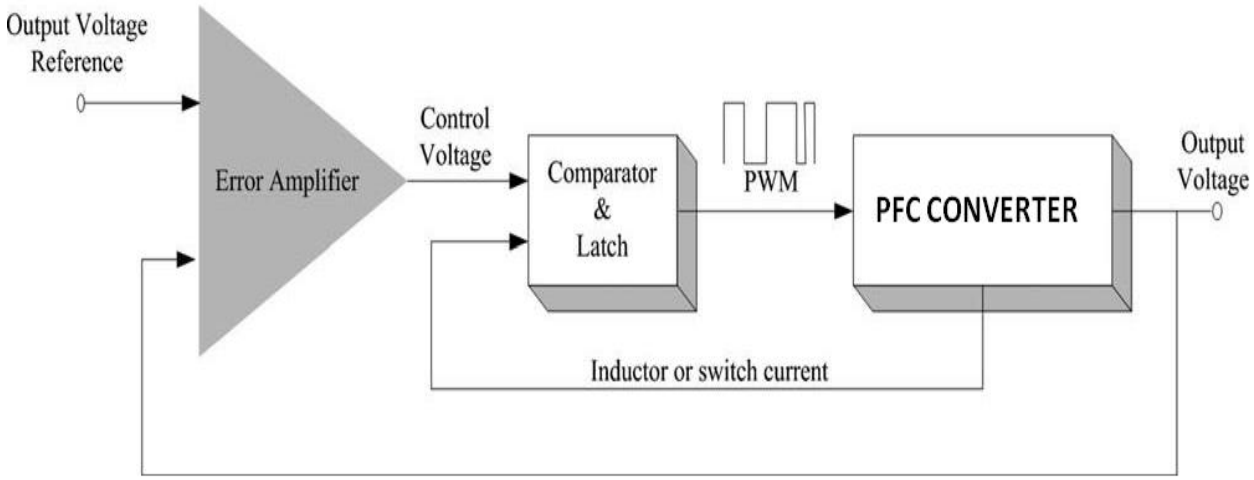


Figure 5.8: Current-mode control scheme [30].

The advantages which the control technique offers include the following [30]:
(1) Since inductor current rises with a slope determined by *V*sï *V*o, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage.
(2) Since the error amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop. This allows both simpler compensation and a higher gain bandwidth over a comparable voltage-mode circuit.
(3) Additional benefits with current-mode circuits include inherent pulse-by-pulse current limiting by merely clamping the command from the error amplifier, and the ease of providing load sharing when multiple power units are paralleled.

While the improvements offered by current mode are impressive, it has its own unique set of problems which must be solved in the design process. A list of some of these is outlined below [30]:
(1) There are now two feedback loops, making circuit analysis more difficult.
(2) The control loop becomes unstable at duty cycles above 50% unless slope compensation is added.
(3) Since the control modulation is based on a signal derived from output current, resonances in the power stage can insert noise into the control loop.
(4) A particularly troublesome noise source is the leading edge current spike typically caused by transformer winding capacitance and output rectifier recovery current.
(5) With the control loop forcing a current drive, load regulation is worse and coupled inductors are required to get acceptable cross regulation with multiple outputs.

The current mode controller for boost PFC converter is simulated using MATLAB-Simulink. The circuit parameters are given below:

Vs(peak)=311V, Vs(rms)=220V, f(line)=50Hz, L=10mH, C=5000ε F, R-load=40Ý, Vout=400V, Pout=4000W.

For voltage controller Kp=0.2 and Ki=20. For current controller Kp=5 and Ki=1000. (For this controller Kp and Ki are obtained using the trial and error method.)

Figure 5.9 shows the MATLAB simulink model for the boost converter with the current mode controller. Figure 5.10 and figure 5.11 shows the MATLAB simulink model of the boost converter and the current mode controller respectively.

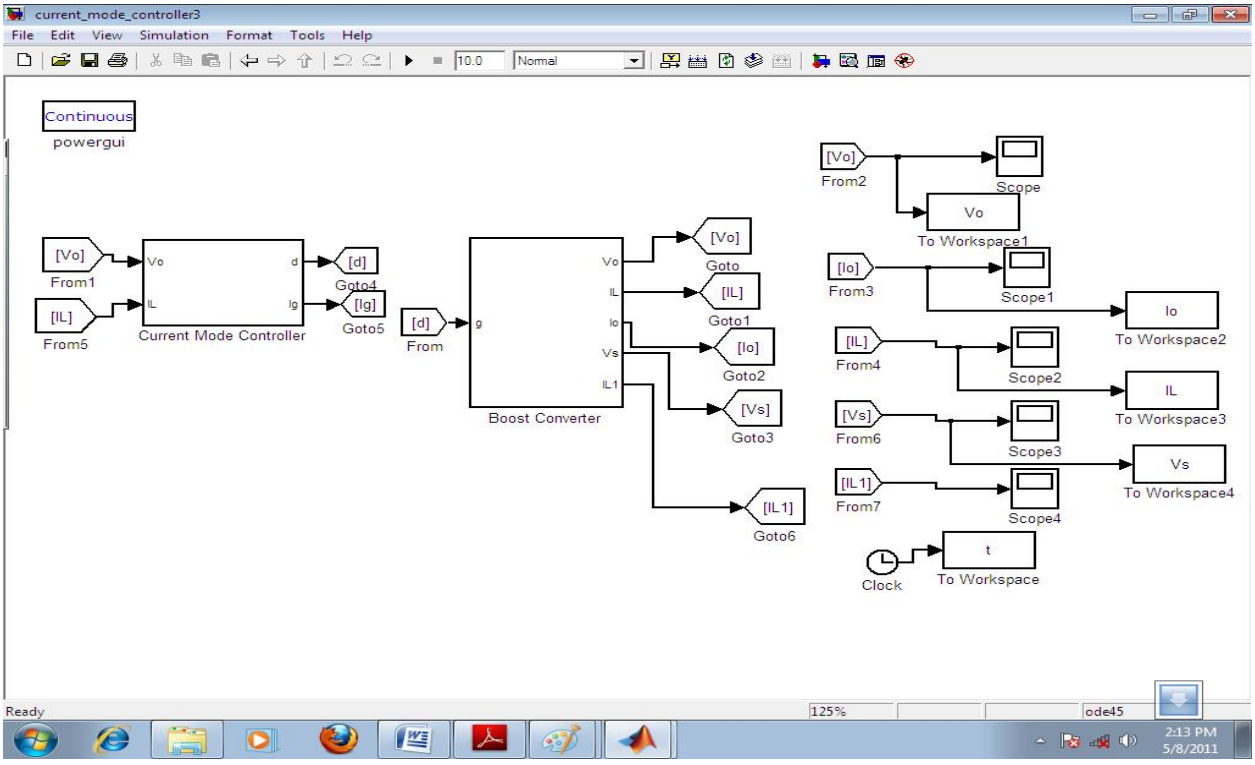


Figure 5.9: MATLAB model of the boost converter with the current mode controller

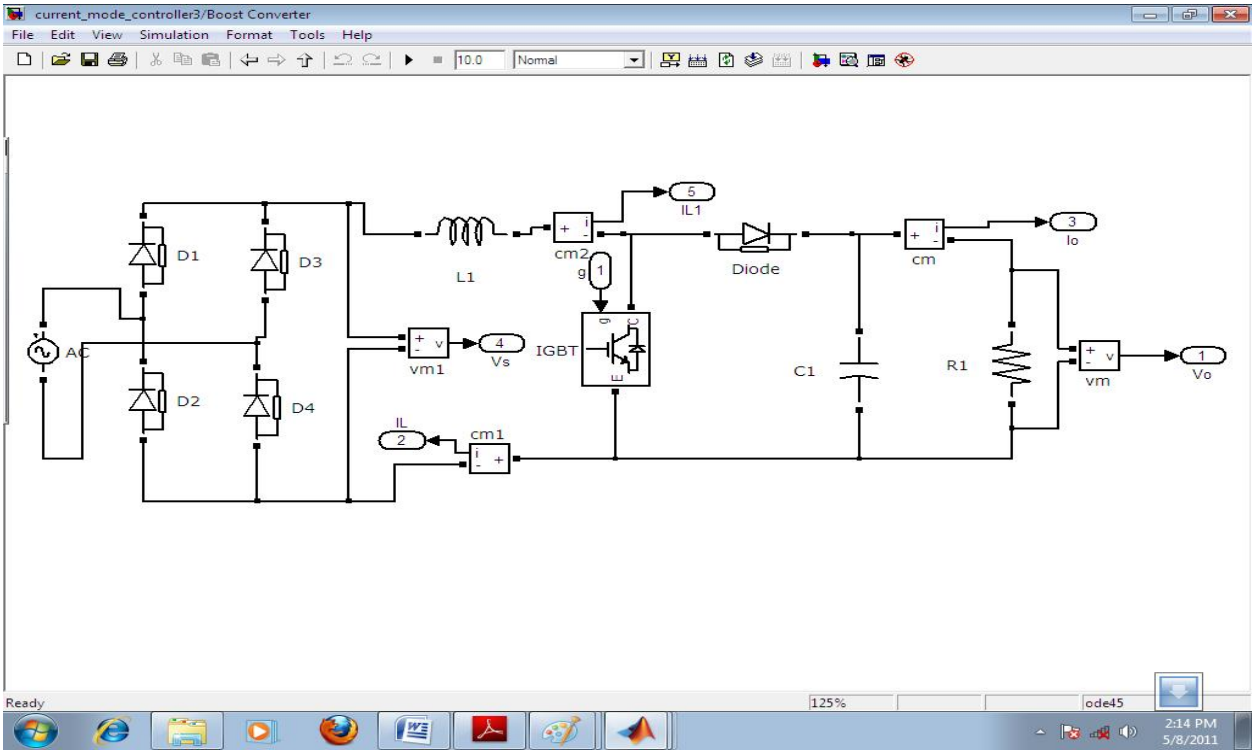


Figure 5.10: MATLAB model of the boost PFC converter

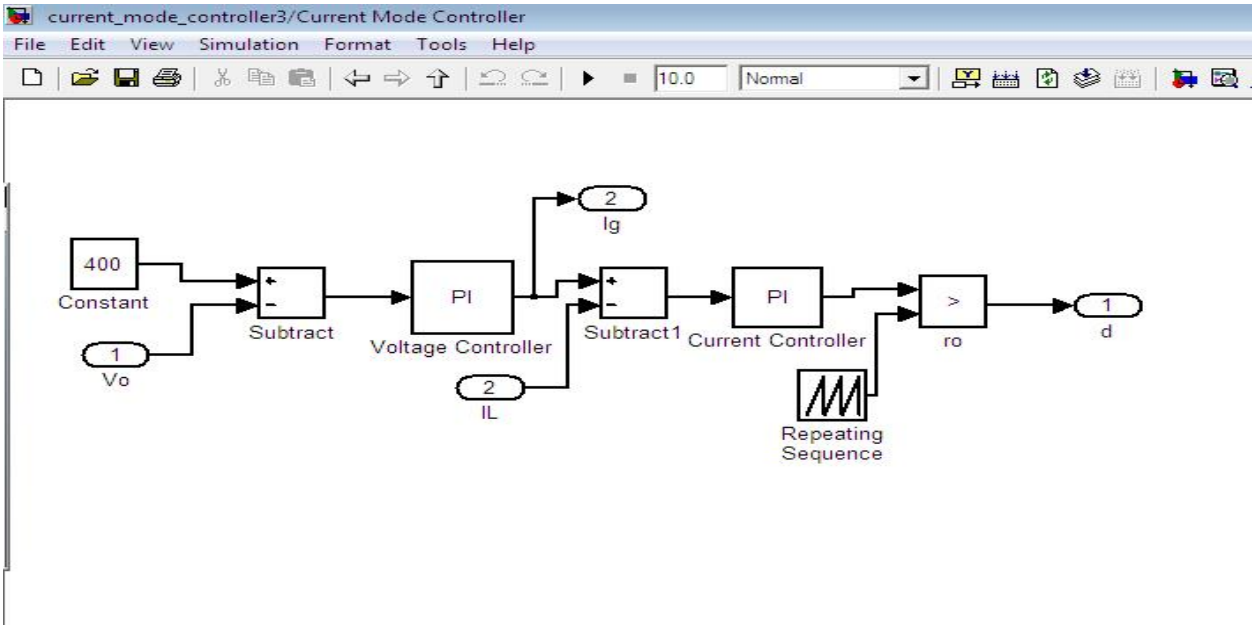


Figure 5.11: MATLAB model of the current mode controller

The following figures show the results of simulation. Figure 5.12 and 5.13 show the output voltage and the output current respectively. Figure 5.14 shows the rectified input voltage and the inductor (input) current.

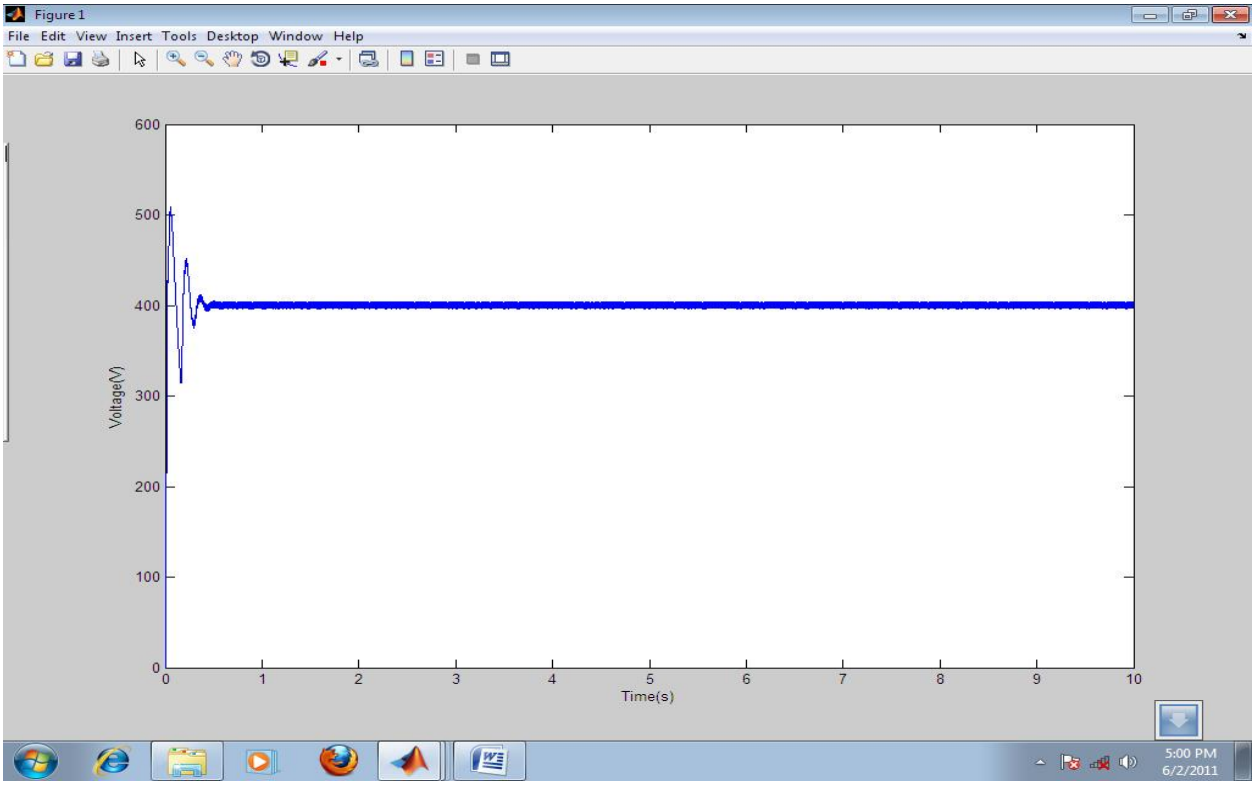


Figure 5.12: The output voltage of the current mode controlled converter

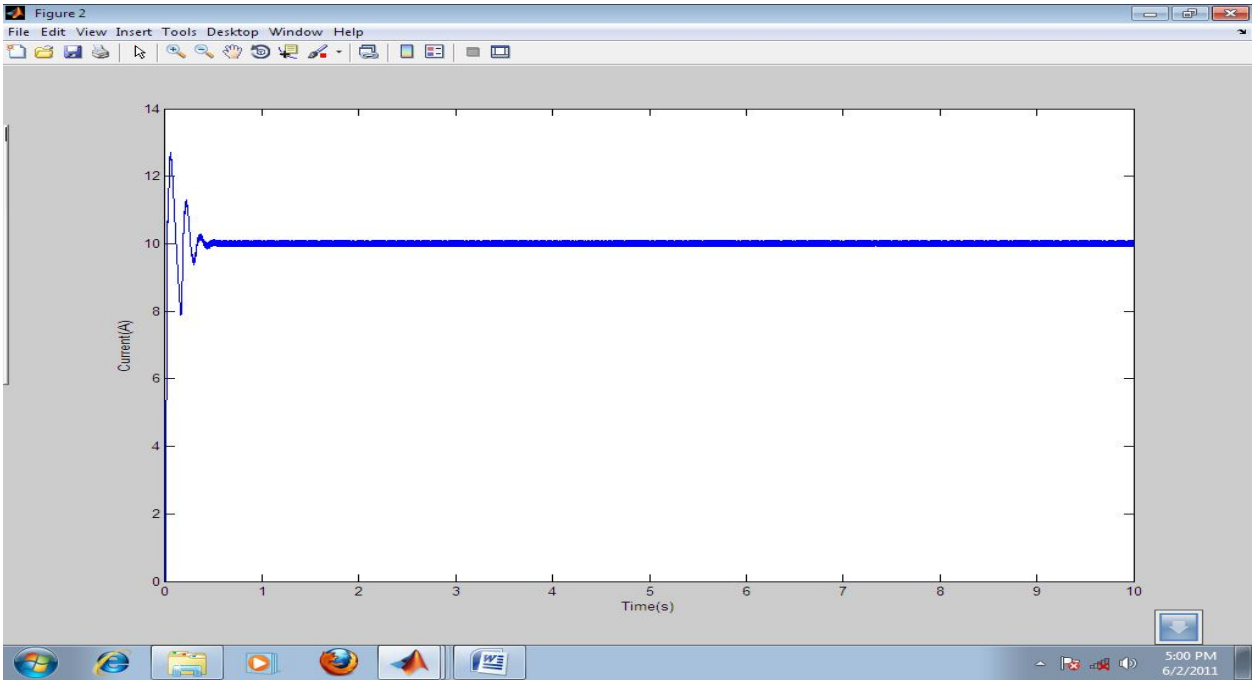


Figure 5.13: The output current of the current mode controlled converter

Figure 5.14: The rectified input voltage (upper) and inductor current (lower) of the current mode controlled converter

The output voltage and output current are obtained as desired. The output voltage is controlled to the 400V level. The output power is 4KW as desired. The inductor current is in phase with the input voltage waveform and it has a better shape than that was obtained using voltage mode controller. Hence the current mode controller is better than the voltage mode controller. But the best result (a near unity power factor) is obtained when the PFC mode controller is used.

5.3 PFC-Mode Control

The PFC controller generally has two control loops. The first loop of these is a voltage control loop for regulated output voltage (outer loop). The second loop is a current control loop for high PF value and active shaping the input current (inner loop). This structure is named as average current mode controller [28, 30].

A PFC mode controller with boost converter is shown in Figure 5.15. In basic form, a switch controls the boost converter circuit. When the switch is closed, current flows through the inductance. After then, the switch is opened and the current is forced to flow through the diode to the output. Multiple cycles of this switching cause the output capacitor voltage to build due to the charge it stores from the inductor current. The result is a higher output voltage than the source voltage [30]. Generally, voltage and current control of boost converter can be fulfilled via traditional control methods such as PI controller.

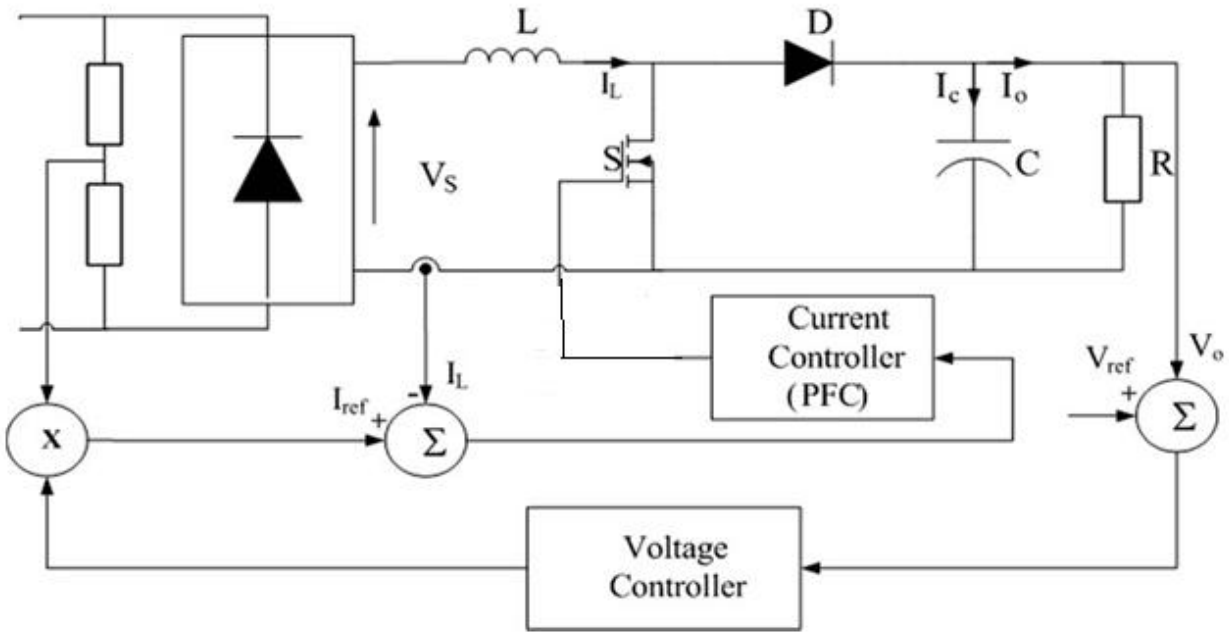


Figure 5.15: Boost converter circuit with PFC mode controller [30].

The advantages of average current-mode control can be stated as follows [30]:

(1) Constant switching frequency,

(2) No need of compensation ramp,

(3) Control is less sensitive to commutation noises, due to current filtering,

(4) Better input current waveforms than for the peak current control since, near the zero crossing of the line voltage, the duty cycle is close to one, so reducing the dead angle in the input current.

Disadvantages of average current-mode control are stated as follows [30]:

(1) Inductor current must be sensed,

(2) A current error amplifier is needed and its compensation network design must take into account the different converter operating points during the line cycle.

The PFC mode controller for boost PFC converter is simulated using MATLAB-Simulink. The circuit parameters are given below:

Vs(peak)=311V, Vs(rms)=220V, f(line)=50Hz, L=10mH, C=5000ε F, R-load=40Ý, Vout=400V, Pout=4000W.

For voltage PI controller Kp=0.002 and Ki=2 as determined in equation (4.33). For current PI controller Kp=50 and Ki=100 as obtained from equation (4.27). These values of Kp and Ki are determined previously in the design stage of the current loop and voltage loop compensator.

Figure 5.16 shows the MATLAB simulink model for the boost converter with the PFC mode controller. Figure 5.17 and figure 5.18 shows the MATLAB simulink model of the boost converter and the PFC mode controller respectively.

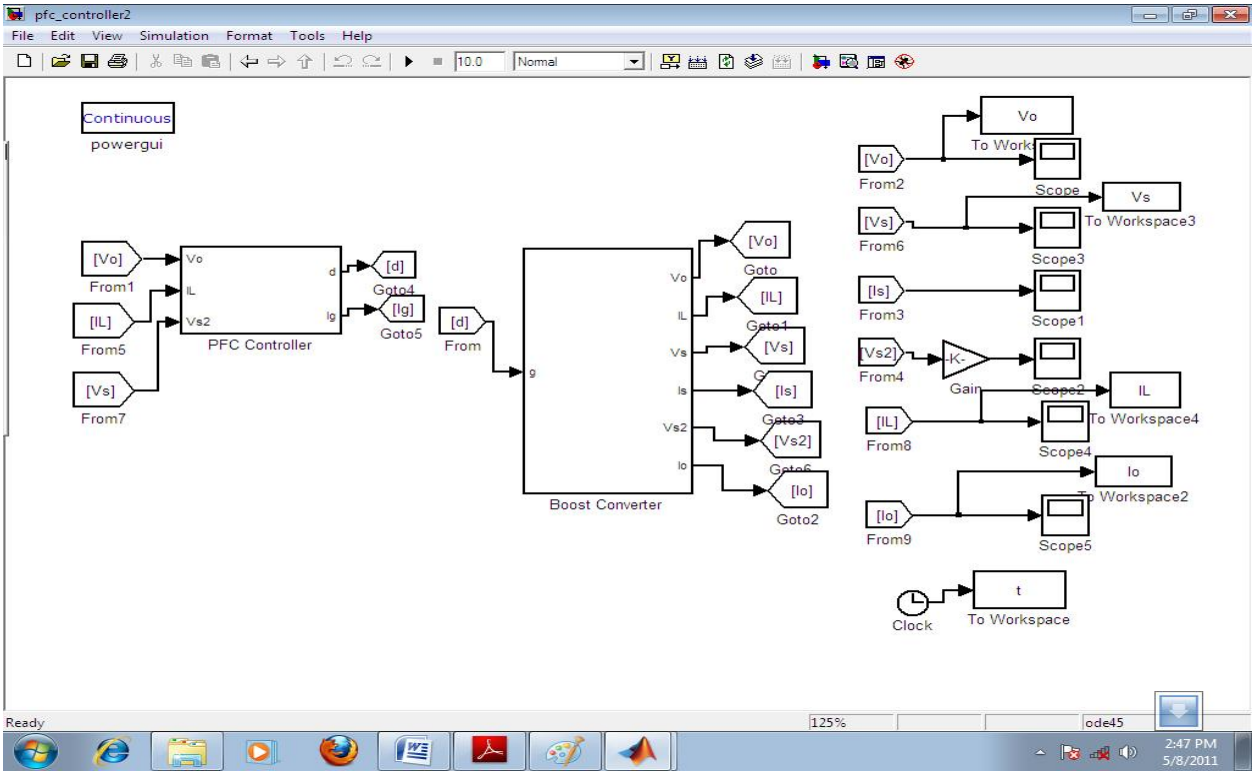


Figure 5.16: MATLAB model of the boost converter with the PFC mode controller

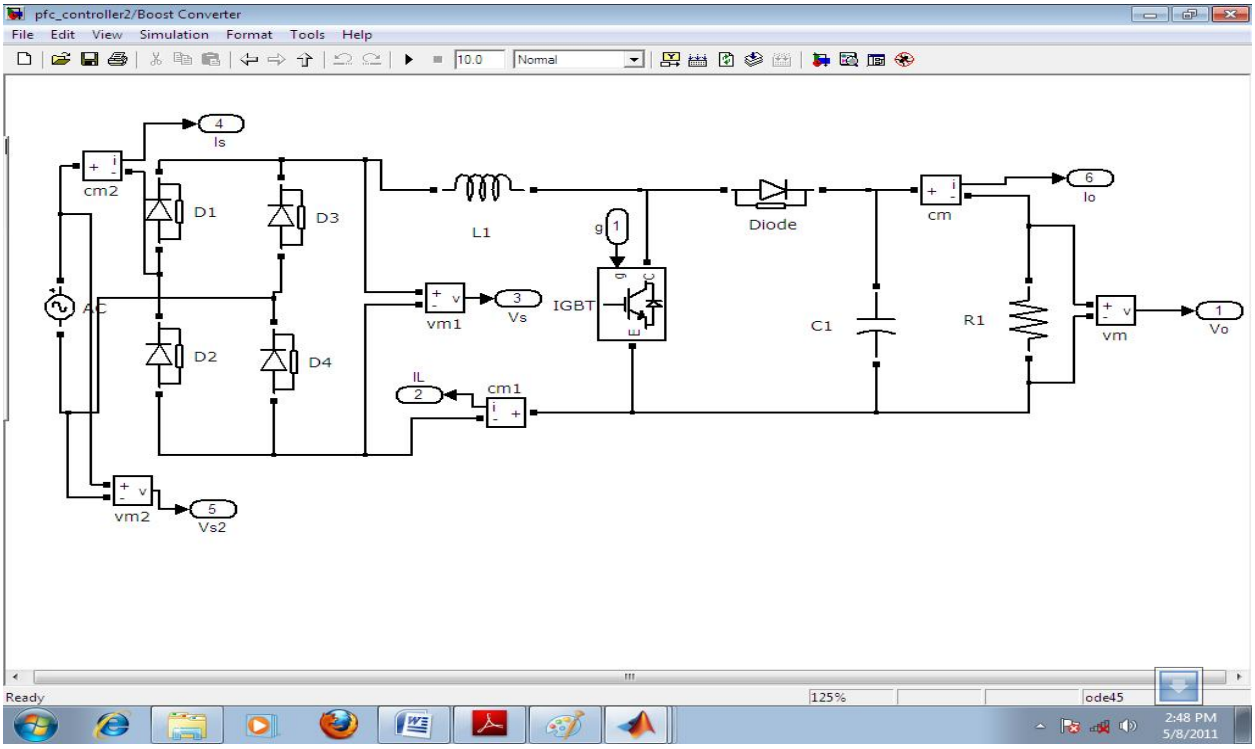


Figure 5.17: MATLAB model of the boost converter

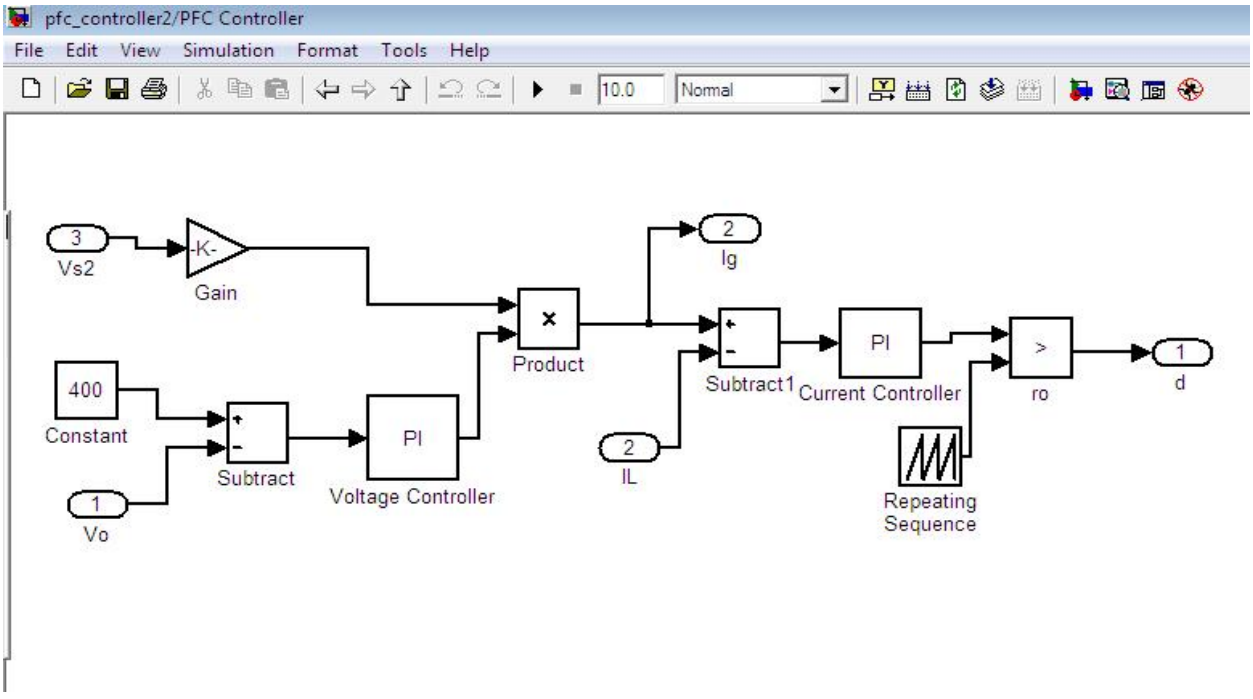


Figure 5.18: MATLAB model of the PFC mode (average current mode) controller

The following figures show the results of simulation. Figure 5.19 and 5.20 show the output voltage and the output current respectively. Figure 5.21 shows the rectified input voltage and the inductor (input) current.

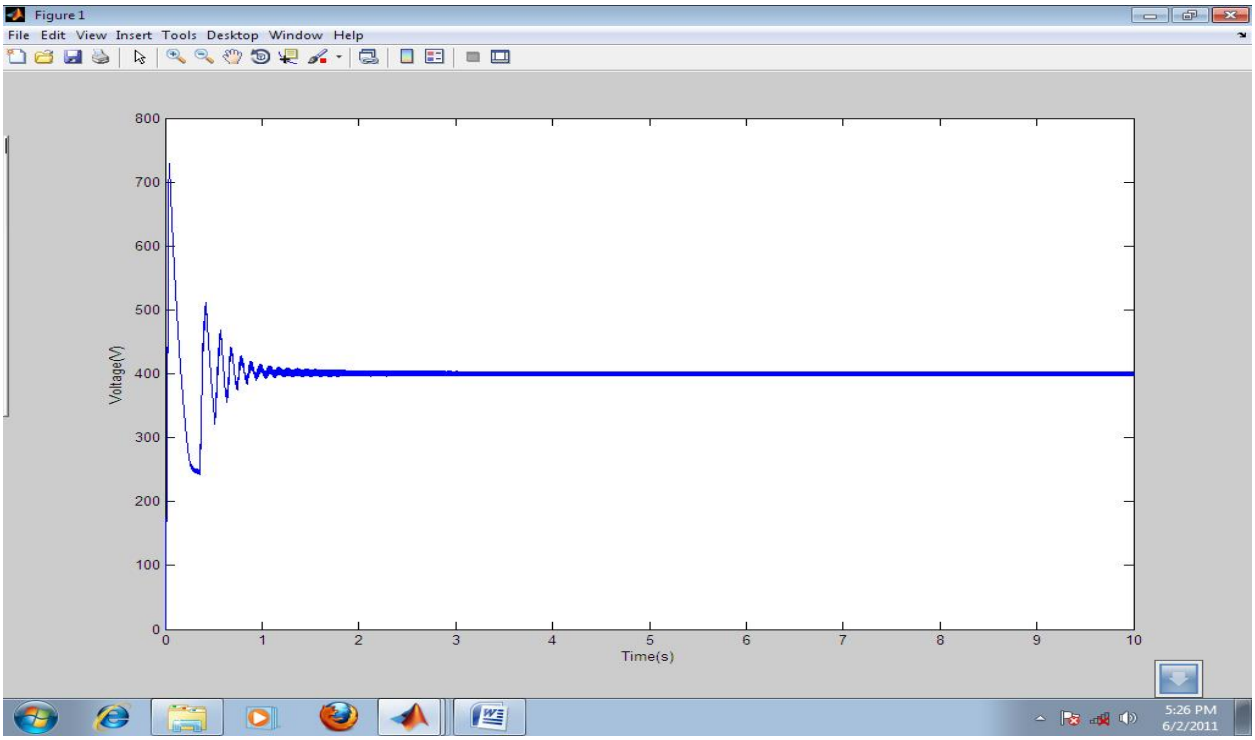


Figure 5.19: The output voltage of the PFC mode controlled converter

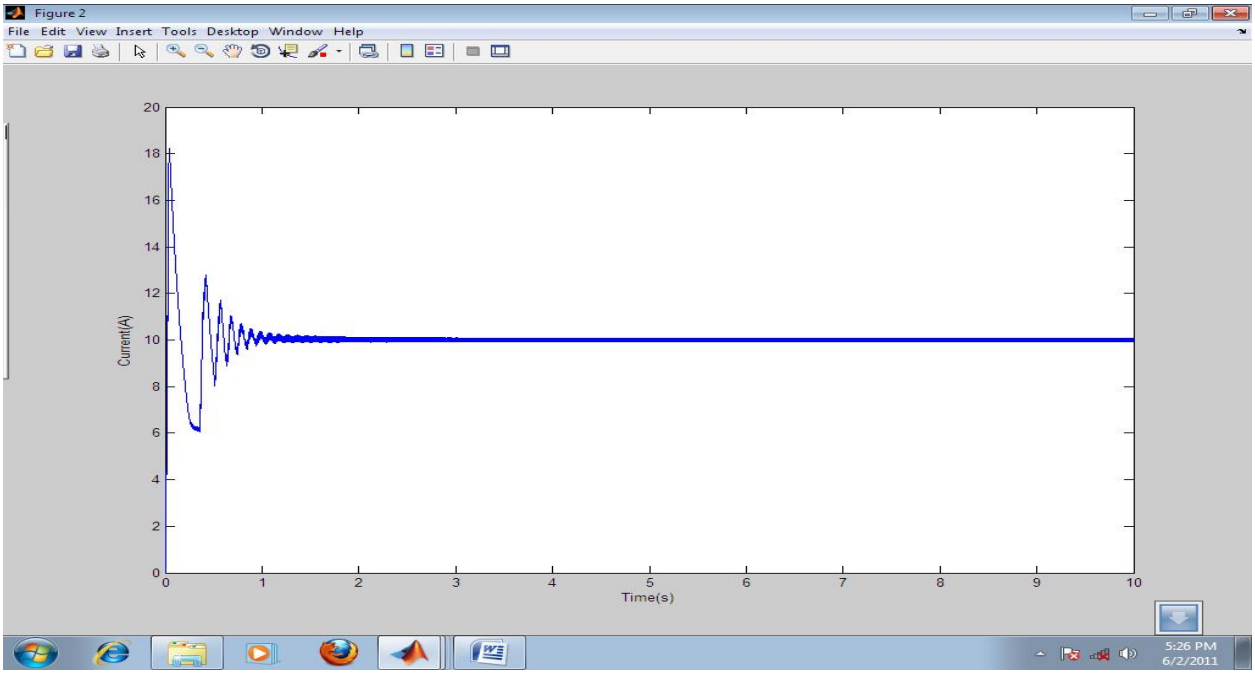


Figure 5.20: The output current of the PFC mode controlled converter

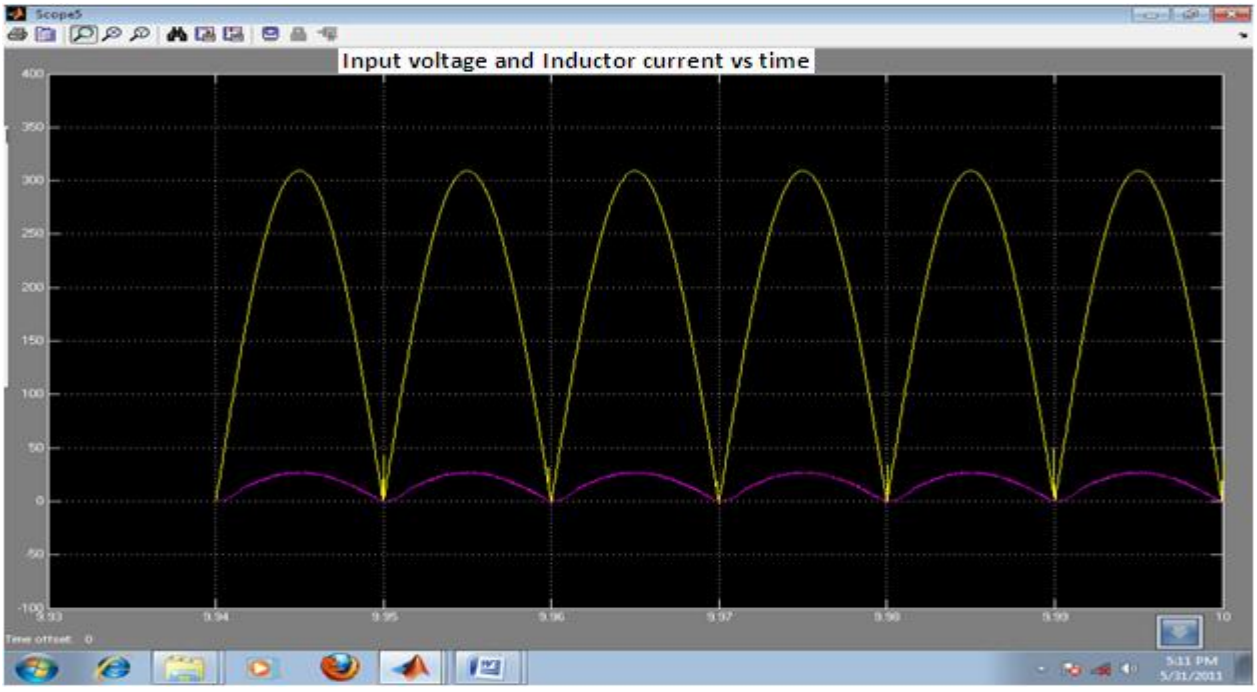


Figure 5.21: The rectified input voltage (upper) and inductor current (lower) of the PFC mode controlled converter

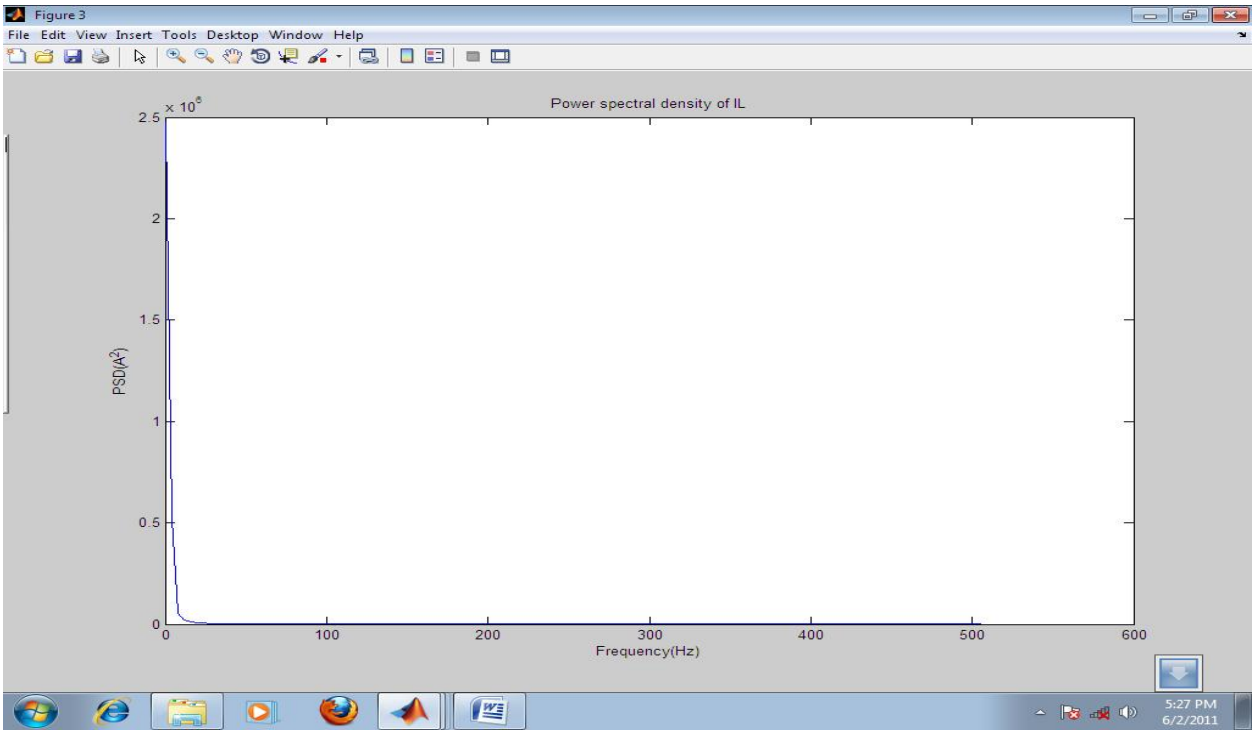


Figure 5.22: Power spectral density of the inductor (input) current

Figure 5.22 shows the power spectral density of the inductor current. This was used to approximate the total harmonic distortion (THD) and power factor (PF) of the input current as shown in table 5.1. Harmonics beyond n = 7 are negligible.

Harmonic	PSD
3	0.02
5	0.01
7	0.001

Table 5.1: Power spectral density up to seventh harmonics

The total harmonic distortion (THD) and the distortion factor (DF) are given in the following equations [30].

$$THD = \sqrt{\sum_{n=3}^{7} I_n^{\,2}} = \sqrt{(0.02)^2 + (0.01)^2 + (0.001)^2} = 0.0223 \tag{5.1}$$

$$DistortionFactor = \frac{1}{\sqrt{1+THD^2}} = \frac{1}{\sqrt{1+(0.0223)^2}} = 0.99975 \tag{5.2}$$

Hence the THD is 2.23% and the DF is 0.99975. Since there is negligible phase difference between the input voltage and inductor (input) current the power factor (PF) is given as follows [30].

$$PF = \frac{1}{\sqrt{1+THD^2}}\cos(\theta) \approx \frac{1}{\sqrt{1+THD^2}} = 0.99975 \tag{5.3}$$

Hence near unity power factor (PF) is obtained by using the designed PFC controller. The output voltage and output current are obtained as desired. The output voltage is controlled to the 400V level. The output power is 4KW as desired. The inductor current is in phase with the input voltage waveform and it has the best semi-sinusoidal shape as compared to that obtained by using the other two control modes (voltage mode and current mode control). Hence the best result (a near unity power factor) is obtained when the PFC mode controller is used.

Once the PFC controller is designed, it should be checked that it works properly even if there is deviation in the input voltage and the load. Figures 5.23 to 5.25 show the simulation results when the peak input voltage is changed from 311V to 270V, that is about 15% of input voltage variation. Similarly figures 5.26 to 5.28 show the simulation results when the peak input voltage is changed to 350V (about 15% of variation). Figures 5.29 to 5.31 show the simulation results

when the load is changed from 40Ý to 20Ý which is around 50% of load variation. These simulation results show that the designed PFC controller works properly for these input voltage and load variations (deviations).

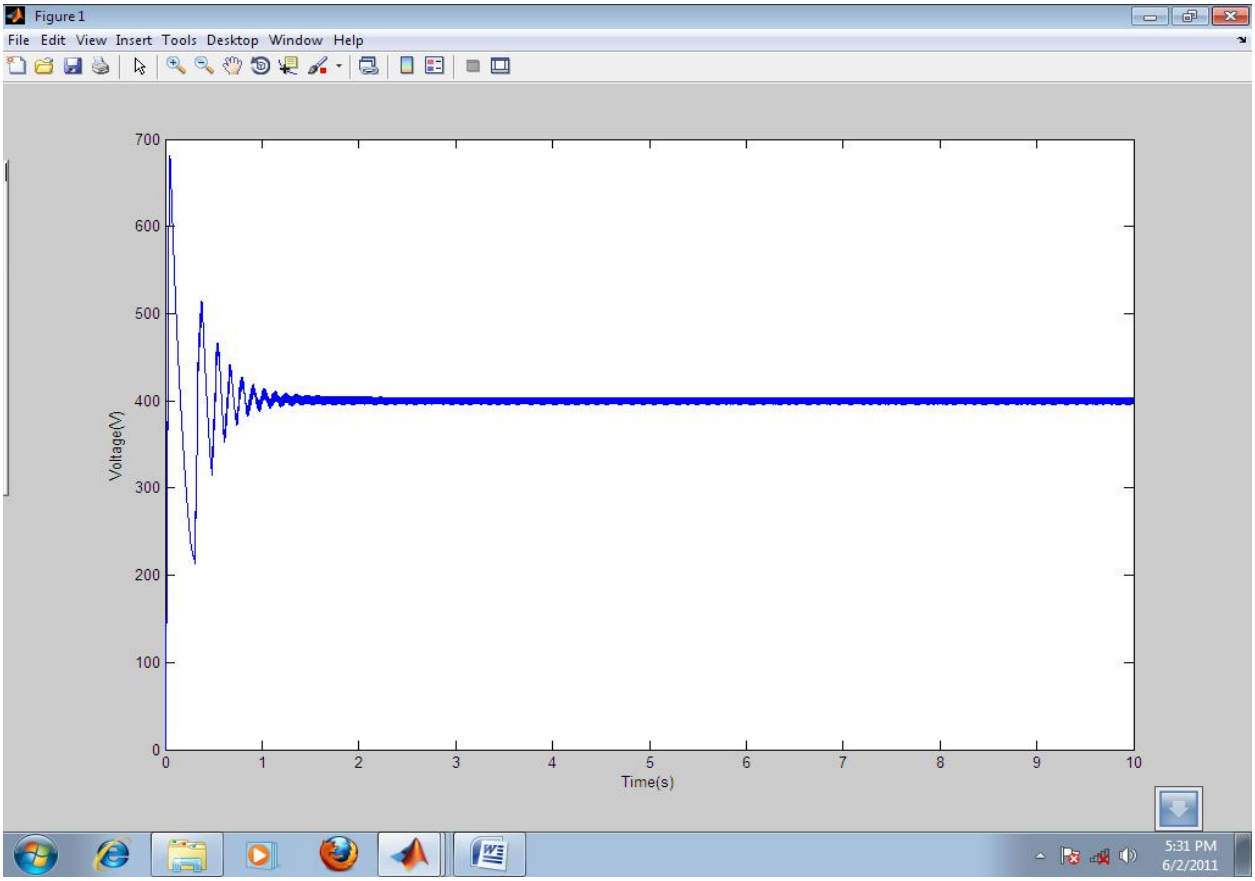


Figure 5.23: Output voltage waveform for Vin(peak)=270V

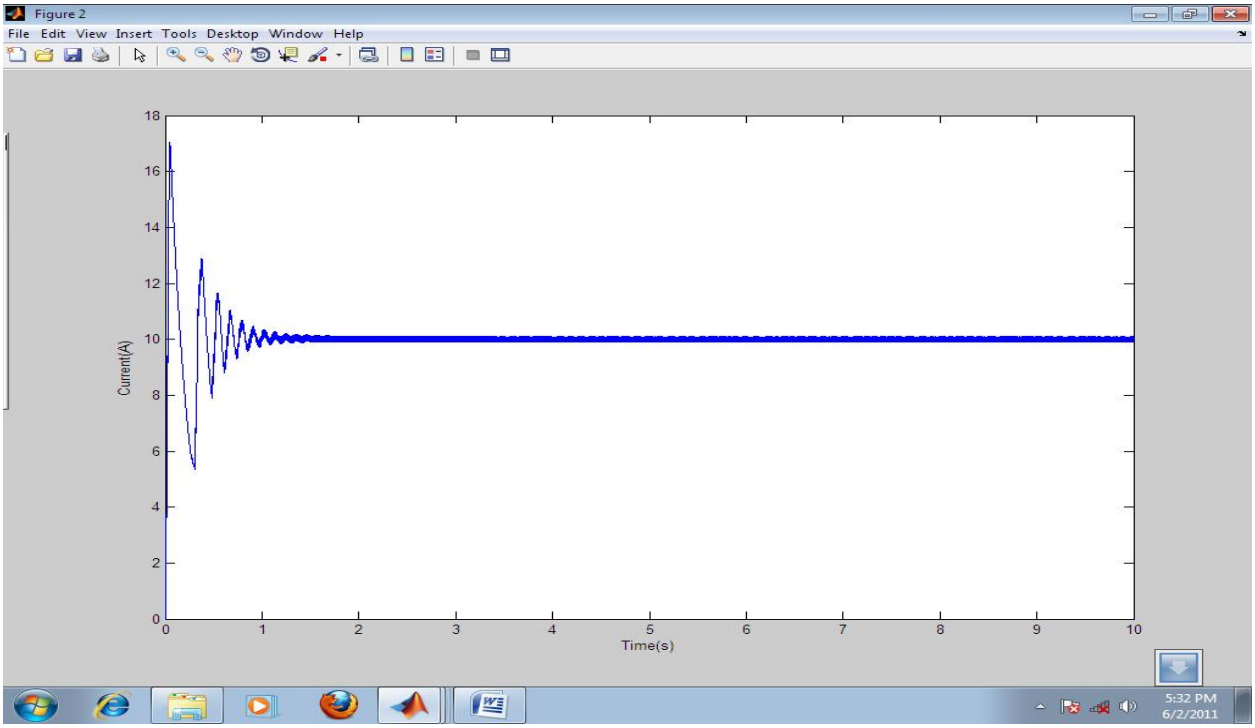


Figure 5.24: Output current for Vin(peak)=270V

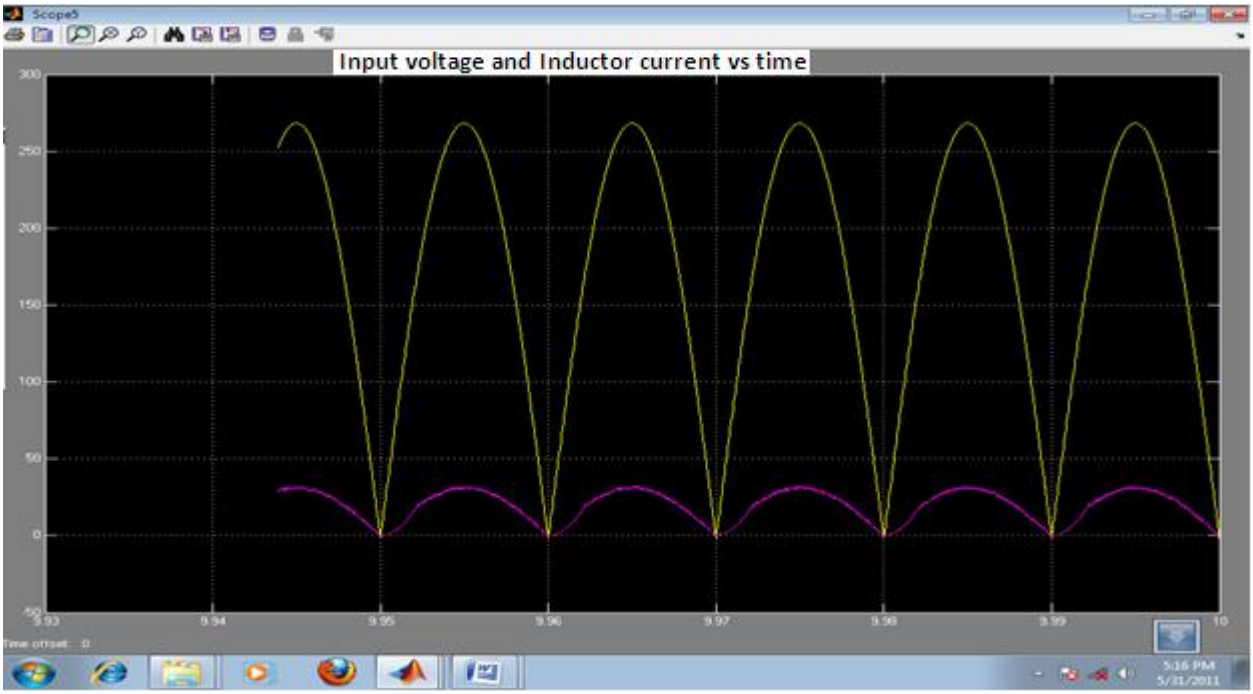


Figure 5.25: The rectified input voltage (upper) and inductor current (lower) for Vin(peak)=270V

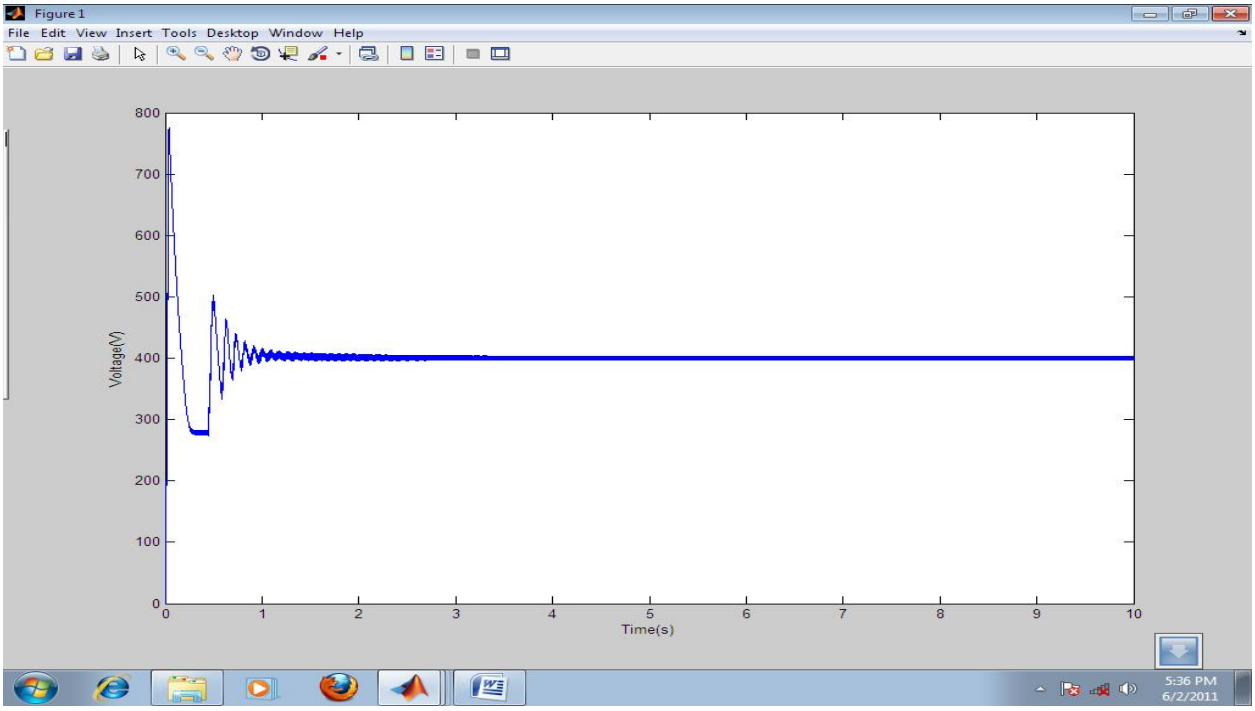


Figure 5.26: The output voltage waveform for Vin(peak)=350V

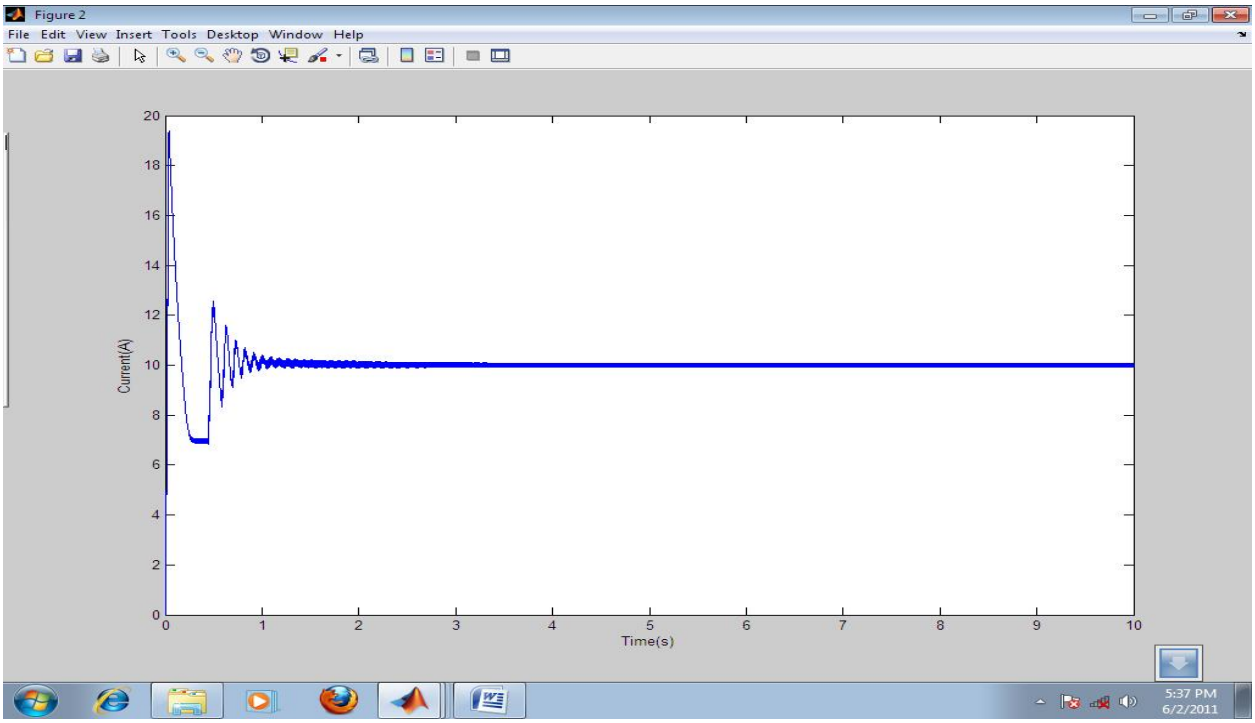


Figure 5.27: The output current waveform for Vin(peak)=350V

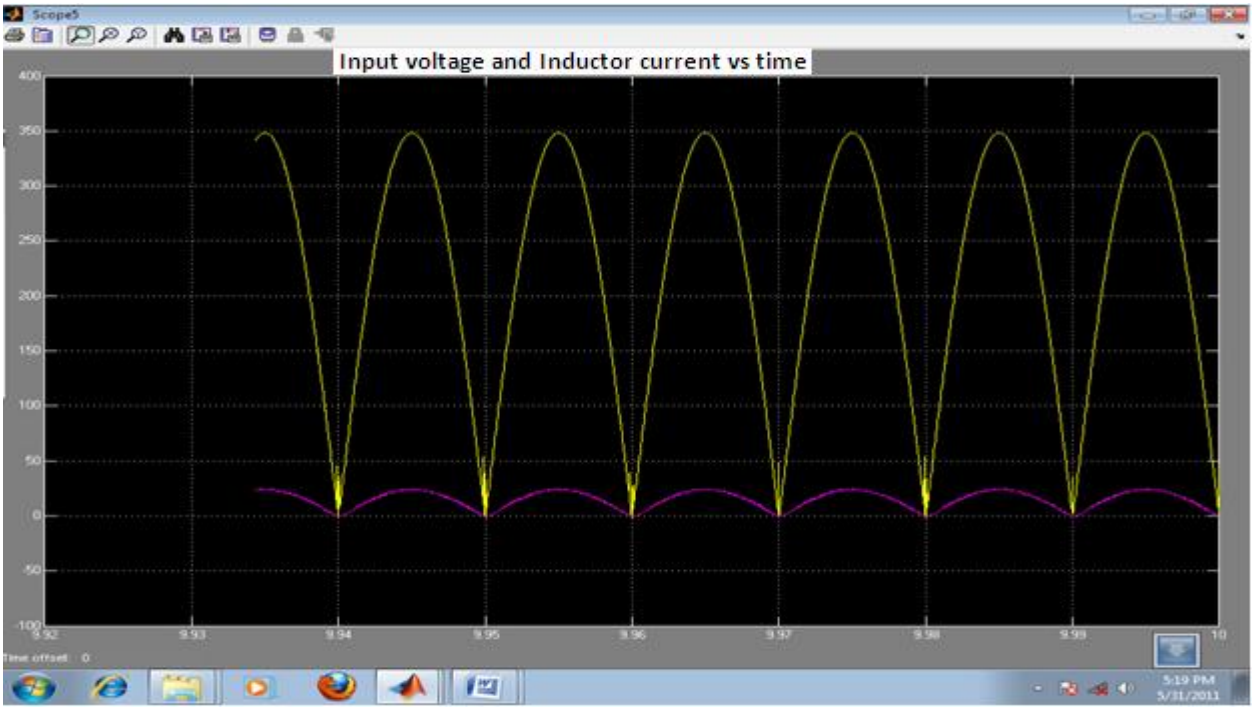


Figure 5.28: The rectified input voltage (upper) and inductor current (lower) for Vin(peak)=350V

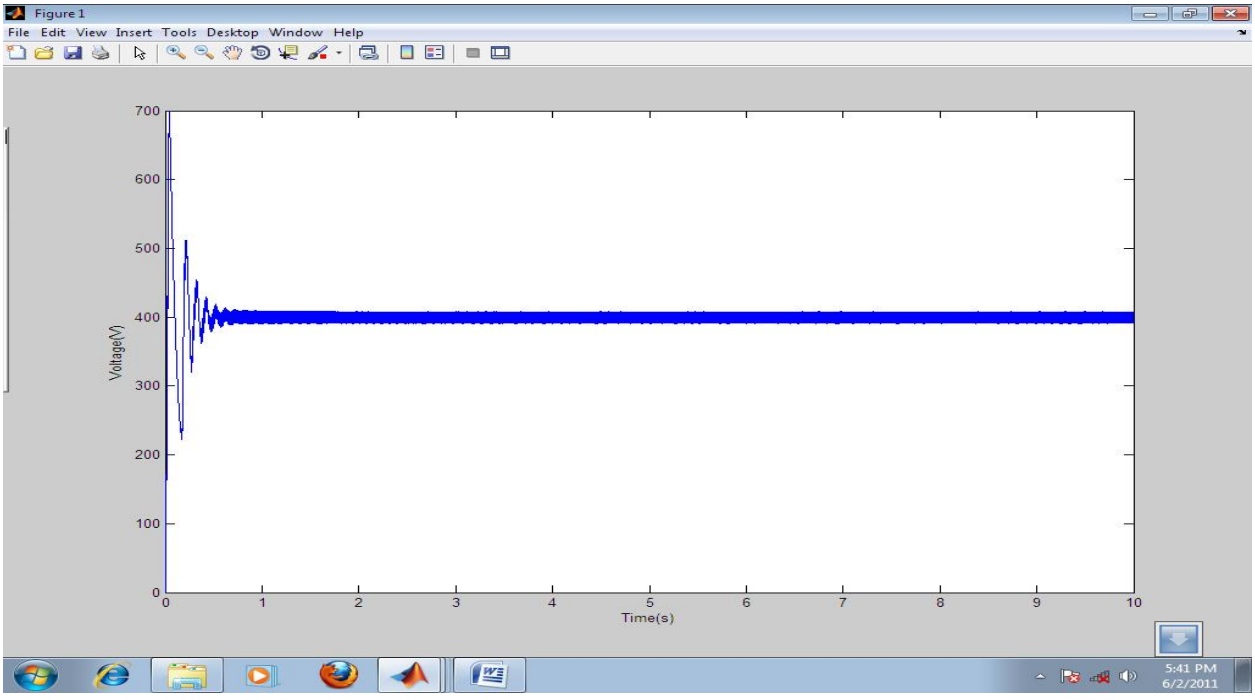


Figure 5.29: The output voltage waveform for R(load)=20Ý

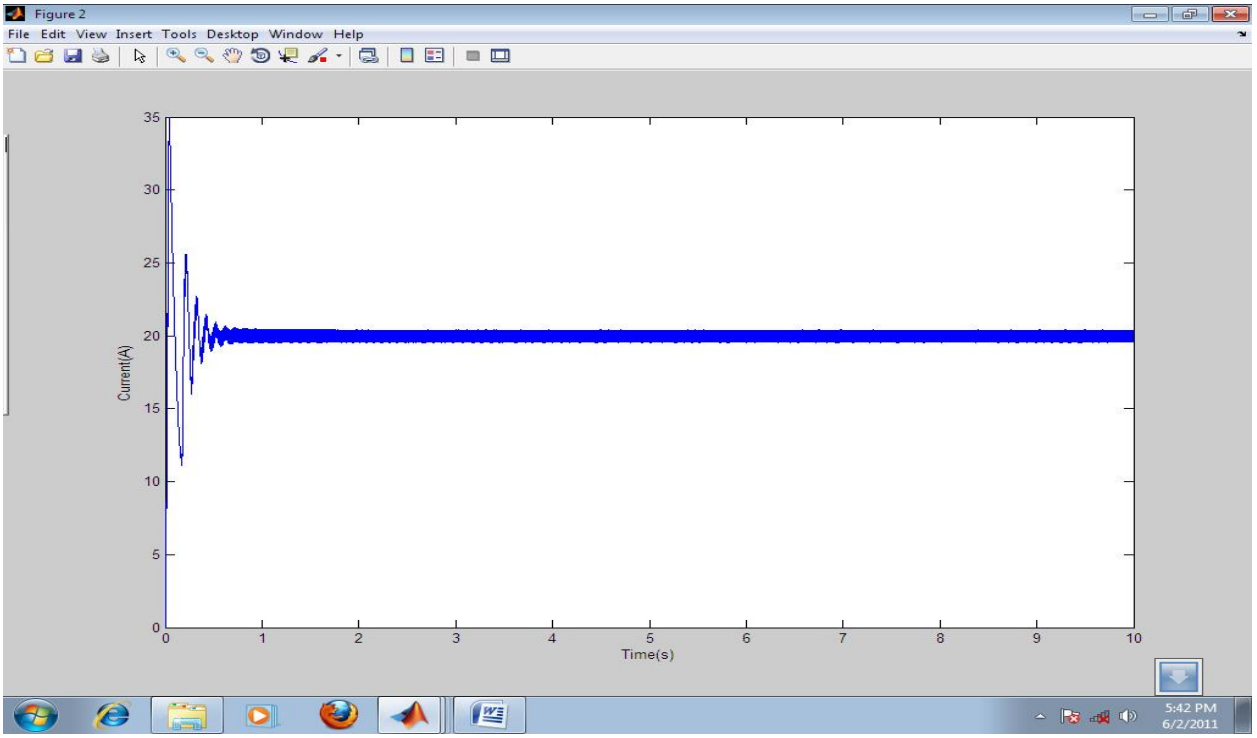


Figure 5.30: The output current waveform for R(load)=20Ý

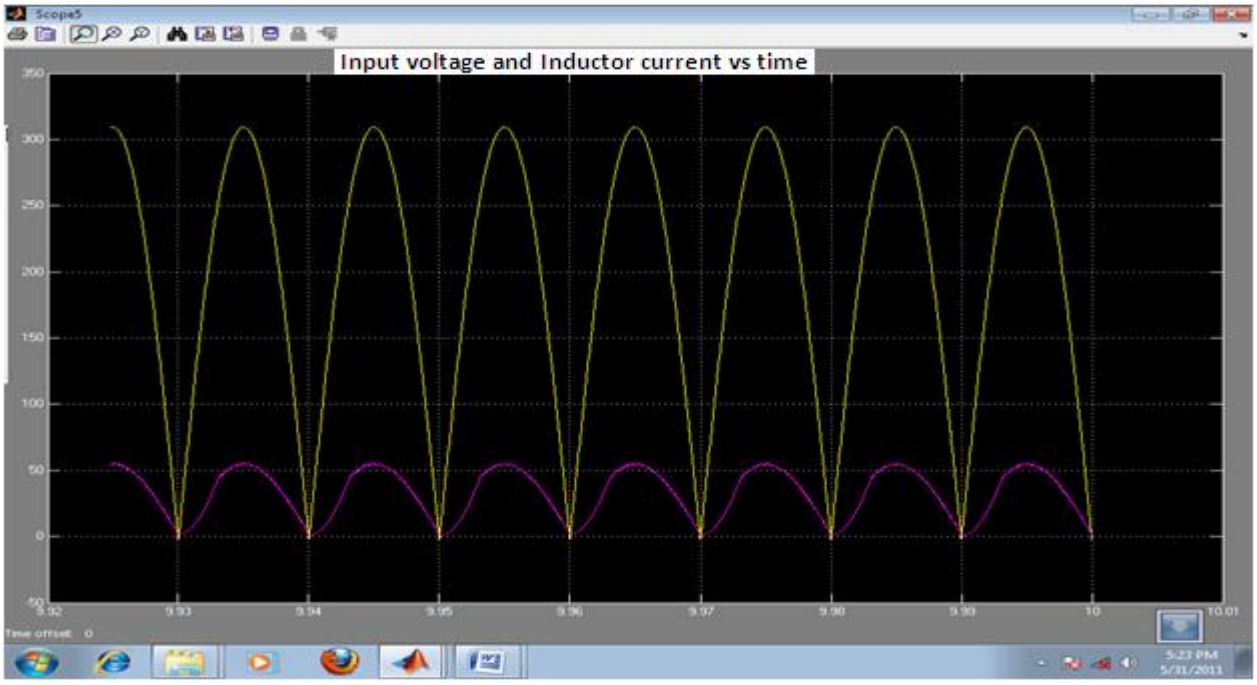


Figure 5.31: The rectified input voltage (upper) and inductor current (lower) for R(load)=20Ý

The main target of the PFC controller is to make the input current(inductor current) in phase with the input voltage, and as seen from the simulation results this task is accomplished with PF= 0. 99975 (unity PF).

The designed PFC controller (with voltage PI controller Kp=0.002 and Ki=2, current PI controller Kp=50 and Ki=100) works well for 15% input voltage variation, and for 50% load variation. The PFC controller works well for up to 10% loading (90% load variation) whose performance is shown in the next section.

The PFC controller renders an input current in phase with input voltage more effectively than the other two methods (i.e. the voltage mode and current mode controllers).

5.4 Comparison of Performance at Different Loads

Figures 5.32 to 5.36 show the inductor (input) current with the input (rectified) voltage for the three control modes (i.e. current mode, voltage mode and PFC mode) under 100%, 75%, 50%, 25% and 10% load. For 100% load the load resistance is 40Ý. For 75%, 50%, 25% and 10% load the load resistance is set to 53Ý, 80Ý, 160Ý and 400Ý respectively. In the figures, the yellow line shows the input (rectified) voltage. The red line, green line and purple line represent inductor current for the voltage mode controller, current mode controller and PFC mode controller respectively.

The output voltage and output current are found to be 400V and 10A as desired for the different loadings. Hence the desired level of output power is obtained which is 4KW for these loadings with the exception of the current mode controller for 25% and 10% load. At 25% and 10% load the current mode controlled converter fails to operate properly since at this loading the inductor current dies down to zero.

For 100% loading, the power spectral density of inductor current for the three control modes is determined using the FFT analysis tool of MATLAB. The power spectral densities for harmonics beyond the seventh are negligible and hence are neglected. This is shown in table 5.2.

Power spectral density of inductor current			
Harmonics	3	5	7
Voltage mode controller	0.1	0.08	0.01
Current mode controller	0.09	0.07	0.001
PFC mode controller	0.02	0.01	0.001

Table 5.2: Power spectral density of inductor current for the three control methods (100% loading)

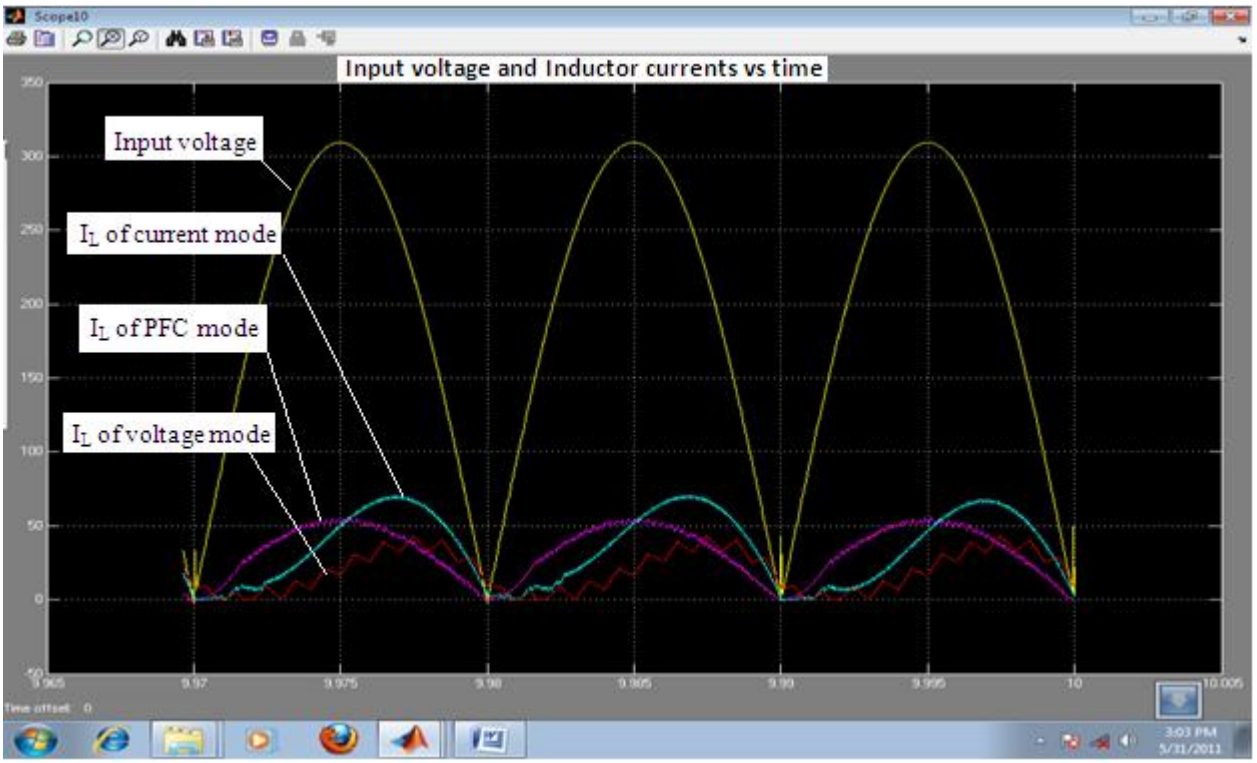


Figure 5.32: The rectified input voltage and inductor current for the three modes (100% load)

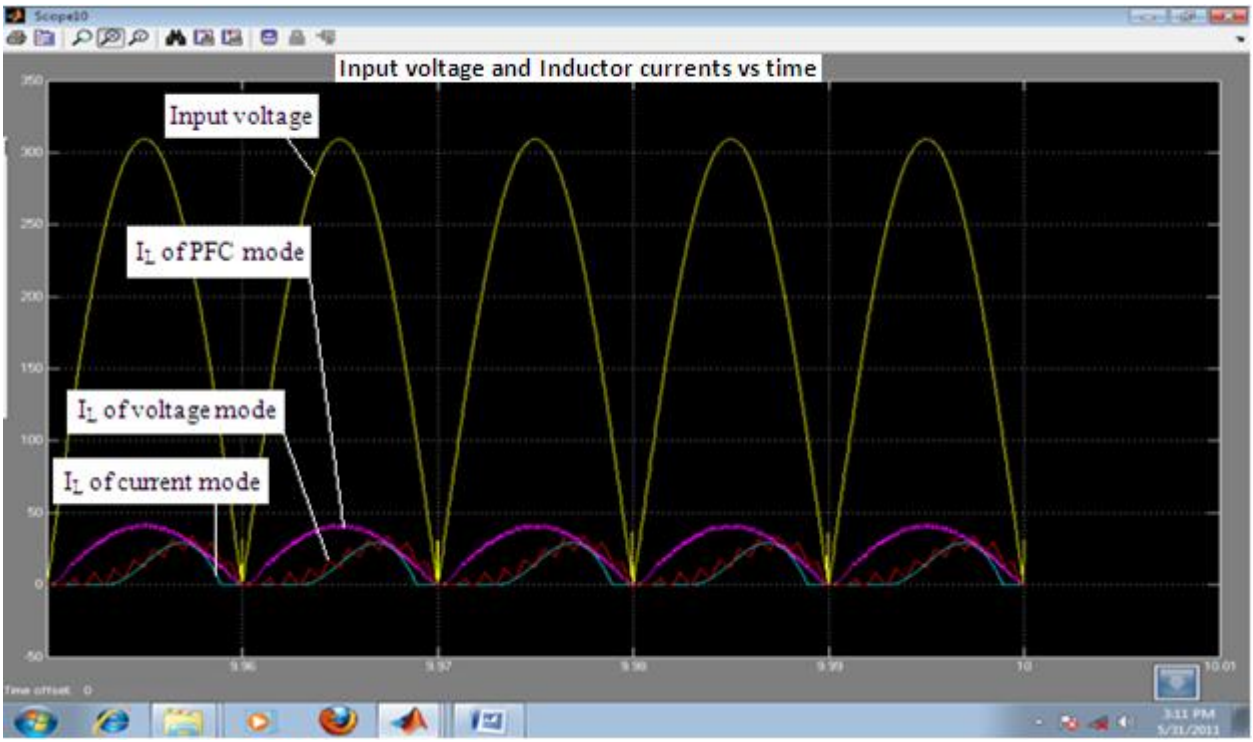


Figure 5.33: The rectified input voltage and inductor current for the three modes (75% load)

Figure 5.34: The rectified input voltage and inductor current for the three modes (50% load)

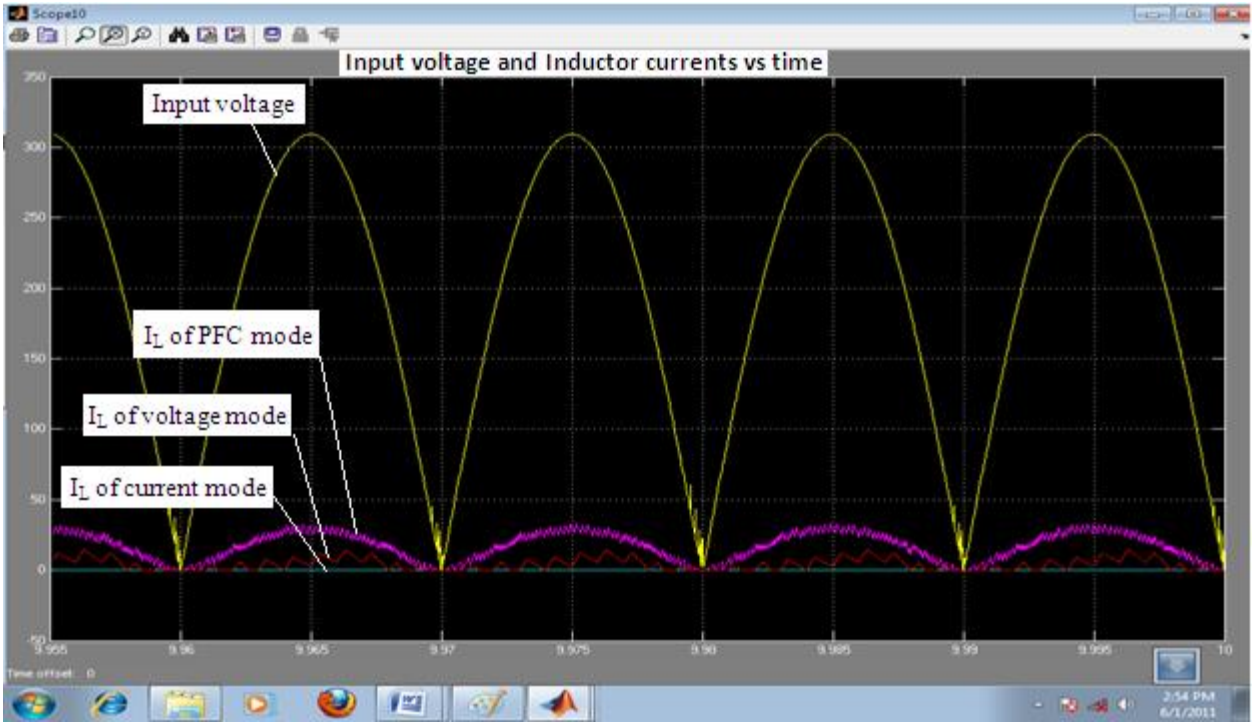


Figure 5.35: The rectified input voltage and inductor current for the three modes (25% load)

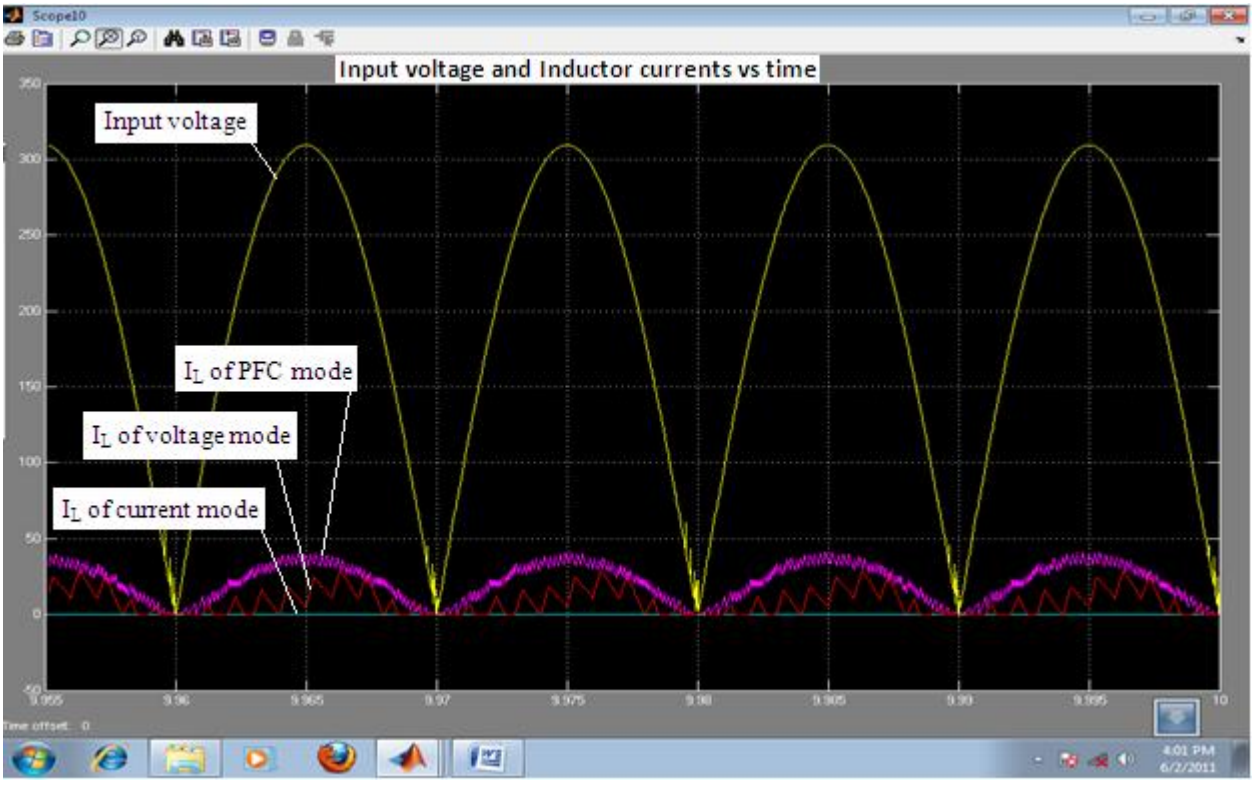


Figure 5.36: The rectified input voltage and inductor current for the three modes (10% load)

For the voltage mode controller, the THD (total harmonic distortion), DF (distortion factor) and PF (power factor) are determined as follows by using the data from table 5.2.

$$THD = \sqrt{\sum_{n=3}^{7} I_n^{\,2}} = \sqrt{(0.1)^2 + (0.08)^2 + (0.01)^2} = 0.128 \tag{5.4}$$

$$DistortionFactor = \frac{1}{\sqrt{1 + THD^2}} = \frac{1}{\sqrt{1 + (0.128)^2}} = 0.99191 \tag{5.5}$$

For the voltage mode controller the inductor current is about one tenth of a half cycle (10% of 180^o) out of phase from the input (rectified) voltage. The phase difference is about 18^o. Hence the power factor is given as follows in equation (5.6).

$$PF = \frac{1}{\sqrt{1 + THD^2}} \cos(\theta) = \frac{1}{\sqrt{1 + (0.128)^2}} \cos(18^o) = 0.943 \tag{5.6}$$

For the current mode controller the THD, DF and PF (for phase difference of 18^o) are determined using the data given in table 5.2 as shown in equations (5.7), (5.8) and (5.9).

$$THD = \sqrt{\sum_{n=3}^{7} I_n^{\,2}} = \sqrt{(0.09)^2 + (0.07)^2 + (0.001)^2} = 0.114 \tag{5.7}$$

$$DistortionFactor = \frac{1}{\sqrt{1 + THD^2}} = \frac{1}{\sqrt{1 + (0.114)^2}} = 0.99356 \tag{5.8}$$

$$PF = \frac{1}{\sqrt{1 + THD^2}} \cos(\theta) = \frac{1}{\sqrt{1 + (0.114)^2}} \cos(18^o) = 0.945 \tag{5.9}$$

Similarly, for the PFC mode controller the THD, DF and PF are determined as shown below.

$$THD = \sqrt{\sum_{n=3}^{7} I_n^{\,2}} = \sqrt{(0.02)^2 + (0.01)^2 + (0.001)^2} = 0.0223 \qquad (5.10)$$

$$DistortionFactor = \frac{1}{\sqrt{1+THD^2}} = \frac{1}{\sqrt{1+(0.0223)^2}} = 0.99975 \qquad (5.11)$$

Hence the THD is 2.23% and the DF is 0.99975. Since there is negligible phase difference between the input voltage and inductor (input) current the power factor (PF) is given in equation (5.12).

$$PF = \frac{1}{\sqrt{1+THD^2}}\cos(\theta) \approx \frac{1}{\sqrt{1+THD^2}} = 0.99975 \qquad (5.12)$$

For the three modes the reactive power absorbed from the source is determined as shown below. Here the assumption is that the input power to the converter is equal to the output power of the converter (4000W). For the voltage mode controller the reactive power is obtained in equation (5.14).

$$Apparent\ Power = \frac{Active\ Power}{PF} = \frac{4000\,W}{0.943} = 4241.78\,VA \qquad (5.13)$$

$$\mathrm{Re}active\ Power = \sqrt{Apparent\ Power^2 - Active\ Power^2} = \sqrt{4241.78^2 - 4000^2} = 1411.63\,VAR \qquad (5.14)$$

Similarly, for the current mode controller the reactive power is obtained as given in equation (5.16).

$$Apparent\ Power = \frac{Active\ Power}{PF} = \frac{4000\,W}{0.945} = 4232.8\,VA \tag{5.15}$$

$$\text{Re}active\ Power = \sqrt{Apparent\ Power^2 - Active\ Power^2} = \sqrt{4232.8^2 - 4000^2} = 1384.41\,VAR \tag{5.16}$$

For the PFC mode controller, a small amount of reactive power is absorbed. It is calculated in equation (5.18).

$$Apparent\ Power = \frac{Active\ Power}{PF} = \frac{4000\,W}{0.99975} = 4001\,VA \tag{5.17}$$

$$\text{Re}active\ Power = \sqrt{Apparent\ Power^2 - Active\ Power^2} = \sqrt{4001^2 - 4000^2} = 89.45\,VAR \tag{5.18}$$

Hence for 100% loading (full load), the reactive power drawn by the PFC converter with the PFC mode controller is only 89.45 VAR whereas the reactive power drawn by the other control mode converter is considerably high. Additionally, the highest PF and the lowest THD are obtained for the PFC control mode. Therefore the best control method with near unity power factor is the PFC control mode. For the 100% load (full load) the performance parameters of the three control modes is summarized in the following table (table 5.3).

	THD	DF	PF	Reactive Power (VAR)
Voltage mode controller	12.8%	0.99191	0.943	1411.63
Current mode controller	11.4%	0.99356	0.945	1384.41
PFC mode controller	2.23%	0.99975	0.99975	89.45

Table 5.3: Performance parameters for the three control modes (100% loading)

By using FFT analysis tool of MATLAB, the power spectral density of inductor current for 75%, 50%, 25% and 10% loading is determined to be as shown in table 5.3. Harmonics beyond the seventh are neglected.

Power spectral density of inductor current												
Loading	75%			50%			25%			10%		
Harmonics	3	5	7	3	5	7	3	5	7	3	5	7
Voltage mode controller	0.2	0.18	0.1	0.25	0.2	0.15	0.2	0.15	0.05	0.25	0.18	0.1
Current mode controller	0.19	0.17	0.01	0.23	0.2	0.01	-	-	-	-	-	-
PFC mode controller	0.03	0.02	0.003	0.04	0.02	0.005	0.04	0.01	0.006	0.04	0.02	0.01

Table 5.4: Power spectral density of inductor current for the three modes (for different loadings)

For the current mode controller at 25% and 10% loading, the current dies down to zero hence the converter cannot operate at these conditions. But the voltage mode controller and PFC mode controller operate well for the different level of loadings.

The THD, DF, PF and reactive power for the three control modes and for the different loadings (75%, 50%, 25% and 10%) are determined using the same methods used previously for full load(100% load). The results for 75%, 50%, 25% and 10% load are shown in the following tables.

	THD	DF	PF	Reactive Power (VAR)
Voltage mode controller	28.7%	0.9612	0.832	2667.19
Current mode controller	25.5%	0.969	0.839	2594.19
PFC mode controller	3.62%	0.99935	0.99935	144.25

Table 5.5: Performance parameters for the three control modes (75% loading)

	THD	DF	PF	Reactive Power (VAR)
Voltage mode controller	35.4%	0.9427	0.816	2833.59
Current mode controller	30.5%	0.9565	0.828	2708.84
PFC mode controller	4.5%	0.999	0.999	178.93

Table 5.6: Performance parameters for the three control modes (50% loading)

	THD	DF	PF	Reactive Power (VAR)
Voltage mode controller	25.5%	0.969	0.839	2594.19
Current mode controller	-	-	-	-
PFC mode controller	4.17%	0.99913	0.99913	166.89

Table 5.7: Performance parameters for the three control modes (25% loading)

	THD	DF	PF	Reactive Power (VAR)
Voltage mode controller	32.4%	0.951	0.824	2750.44
Current mode controller	-	-	-	-
PFC mode controller	4.58%	0.999	0.999	178.93

Table 5.8: Performance parameters for the three control modes (10% loading)

As seen from the tables, the best performance (the lowest THD and the highest near unity PF) is obtained from the PFC mode controller for all levels of loading. The acceptable level of THD is below 5%. For the PFC mode controller the THD obtained is as desired (below 5%) whereas for the voltage mode and current mode controller the THD is well above the limit. In addition the lowest level of drawn reactive power is obtained using the PFC mode controller. Hence, PFC mode control is the preferred control method as compared to the voltage mode and current mode control schemes.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this thesis, a digitally controlled switched mode PFC (power factor correction) converter has been designed, modeled and simulated. Of the three major control modes (i.e. voltage mode, current mode and PFC mode) PFC mode controller implementation is the target of this study. The three control modes have been simulated using the MATLAB Simulink for different loadings. From the simulation results it can be deduced that the PFC mode controller for the switched mode converters has the best performance.

One of the ways of evaluating the performance of a digital controller is to determine how the controller responds to input voltage variation and load variation. It has been found that the PFC mode controller performs well even if there is an input voltage variation up to 15% and load variation up to 10% load. The results of the simulation show that the required level of output voltage and output power are obtained with the power factor being improved to near unity. In addition, the performance of the three common control modes (i.e. current mode, voltage mode and PFC mode control) is assessed for 100%, 75%, 50%, 25% and 10% loading. The performance parameters are THD, DF, PF and reactive power drawn from the source. For the 100% load the PFC mode controller achieves a near unity input power factor with power factor of 0.99975. At full load, the voltage mode and current mode controller have a lower power factor of 0.943 and 0.945 respectively. For the other loadings, the PFC mode controller has a near unity power factor greater than 0.99. The voltage mode and current mode controller have a relatively lower power factor for the different loadings (about 0.8). It is found that the lowest total harmonic distortion (THD) and reactive power, and the highest power factor (PF) are obtained using the PFC mode control. Since a near unity PF is the main objective, based on this criteria the PFC mode control is the best control mode as compared to the voltage mode and current modes of control.

This work is a significant contribution to the field of researches made on power factor correction. Power factor correction is an important field of study since it can be used to reduce the harmonics in the line current, increase the efficiency of power systems, and reduce customersô utility bills.

6.2 Future Work

In the future, the performance of the single phase two-channel interleaved boost PFC converter with a digital controller can be investigated. In addition, a digitally controlled cuk converter performance can be studied. These two can provide an improved power factor with low total harmonic distortion.

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DECLARATION

I, the undersigned, declare that this thesis is my original work, has not been presented for a degree in this or other universities, all sources of materials used for this thesis work have been fully acknowledged.

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This thesis has been submitted for examination with my approval as a university advisor.

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