Addis Ababa University
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School of Electrical and Computer Engineering

Performance Analysis of GaN Based Class D Amplifiers in Comparison to Conventional Si Based Amplifiers

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Performance Analysis of GaN based Class D Amplifiers in Comparison to Conventional Si Based Amplifiers

is solely my own work and that if any text, passage or diagrams from books, papers, articles, the internet or other sources have been used in any way, all references – including those found in electronic media – have been acknowledged and fully cited.

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Abstract

Silicon has been the basis of semiconductor technology for the past couple of decades. Hence, engineers and manufacturers have made vast strides in silicon manufacturing, integrated circuit design, and semiconductor applications. However, due to the saturation of Moore's Law in recent years, Si-based semiconductor is about to see its limit in electronics applications. Meanwhile, there's a continuing need for faster, more efficient circuits. One of the paths forward from this point is for researchers and companies alike to look towards different materials to produce the devices of tomorrow. One material in particular that has caught the attention of the industry is gallium nitride (GaN). GaN power devices have lower specific on-resistance and faster switching speeds when compared to silicon power devices. These attributes make the GaN devices attractive for applications in the high efficiency class D audio amplifiers, a field that has not been widely studied. To that end, this thesis work set out to compare the performance of GaN based class D amplifiers with their Si counterparts. A class D audio amplifier was designed in the full bridge (bridge tied load – BTL) topology having a second order Butterworth filter for its output. The GaN based class D circuit had a high efficiency of about 97.7% while the Si had 85.7% at 100kHz switching frequency. It was also observed that as the switching frequency increased the efficiencies decreased. The GaN efficiency decreased to about 89.5% and the Si to 63.1% at 800kHz. This concludes that GaN class D amplifiers are certainly better than Si, especially for higher switching frequencies.

Keywords: *GaN (Gallium Nitride), Class D audio amplifier, Bridge Tied Load (BTL), High Electron Mobility Transistor (HEMT)*

Acknowledgement

First and foremost, I would like to thank God for all the blessings that He has bestowed upon me, the family and friends He has given me. Without His grace I would have been lost.

"The Lord is my rock, my fortress, and my deliverer, my God, my rock in whom I take refuge, my shield, and the horn of my salvation, my stronghold."

(Psalm 18:2)

Terminologies and Abbreviations

2DEG	2-Dimensional Electron Gas
AC	Alternating Current
AlGaN	Aluminum Gallium Nitride
eGaNFET	enhancement type GaN based Field Effect Transistor
EMI	Electromagnetic Interference
EPC	Efficient Power Conversion Corporation
FOM	Figure of Merit
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PAM	Pulse Amplitude Modulation
PDM	Pulse Density Modulation
PPM	Pulse Position Modulation
PWM	Pulse Width Modulation
RF	Radio Frequency
Si	Silicon
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
TI	Texas Instruments

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Chapter 1

1. Introduction

1.1. Amplifiers

Amplifiers can be thought of as a simple box or block containing either a Bipolar Transistor, a Field Effect Transistor or an Operational Amplifier, with the output signal being proportional to the input signal [1]. However, not all amplifiers are the same and there is a clear distinction made between the way their output stages are configured and operate. The main operating characteristics of an ideal amplifier are linearity, signal gain, efficiency and power output but in real world amplifiers there is always a tradeoff between these different characteristics [2]. Amplifiers could be classified based on the parameters they are amplifying, such as voltage amplifiers, current amplifiers and power amplifiers. There is still further classification among the various kinds of power amplifiers. One method of classifying power amplifiers based on circuit configuration and method of operation is by class.

Amplifier classes are mainly lumped into two basic groups [2]. The first are the classically controlled conduction angle amplifiers forming the more common amplifier classes of A, B, AB etc., which are defined by the length of their conduction state over some portion of the output waveform, such that the output stage transistor operation lies somewhere between being “fully-ON” and “fully-OFF”. The second set of amplifiers are the newer so-called “switching” amplifier classes of D, E, F, G, S, T etc., which use digital circuits and modulation techniques to constantly switch the signal between “fully-ON” and “fully-OFF” driving the output hard into the transistor's saturation and cut-off regions. Switching amplifiers are the most efficient amplifiers and Class D amplifier was the first type of switching amplifier developed [3]. Class D amplifier is still one of the most widely used switching amplifiers in the category of audio amplifiers.

1.1.1 Common Audio Power Amplifier Classes

To understand the relevance and the advantage of class D audio amplifiers, some common audio amplifier classes will be discussed first. Conventional class A, B, or AB audio amplifiers directly amplify the analog signals and must work in the linear region. Linear amplifiers have a DC bias current which makes up for a large portion of their power consumption.

Linear-amplifier output stages are directly connected to the speaker (in some cases via capacitors) [4]. If bipolar junction transistors (BJTs) are used in the output stage, they generally operate in the linear mode, with large collector-emitter voltages. The output stage could also be implemented with MOS transistors.

1.1.1.1 Class A Amplifiers

Class A amplifiers are the most common type of amplifier class due to their simple design. It is the simplest form of power amplifier that uses a single switching transistor in the standard common emitter circuit configuration.

The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude of the output signal. Which means that this configuration is in the ideal operating mode, because there can be no crossover or switch-off distortion to the output waveform even during the negative half of the cycle [5].

In other words, the output transistors never turn "OFF". This results in the Class-A type being somewhat inefficient as its conversion of the DC power supply to the AC signal power delivered to the load is usually very low. This will make the board very hot, even when there is no input signal present, so some form of heat sinking is required. In general class A amplifiers have low efficiency of less than 25% since most of its DC power is converted to heat but at the same time, they also have good signal reproduction and linearity.

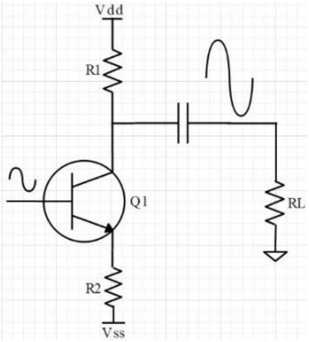


Figure 1: Class A audio power amplifier schematic

1.1.1.2 Class B Amplifiers

Class B amplifiers operate in the opposite way to Class A amplifiers, it tries to address the continuous operation of class A amplifier transistor even when there is no input signal. Class B introduced a second transistor in the topology to improve the full power efficiency of the Class A amplifier.

It uses one transistor only for amplifying one half or 180^o of the input waveform cycle while the other transistor amplifies the other half or remaining 180^o of the input waveform cycle with the resulting "two-halves" being put back together again at the output terminal [7]. In other words, if it is a push-pull topology, each transistor would drive the signal for half a cycle, a N type for the positive cycle and a P type for the negative one.

This advance had its tradeoffs: the transistors did not have a bias circuit and that meant that they could not drive any input below the ON voltage between the Base and the Emitter (that is usually 0.7 Volts for the NPN and -0.7 Volts for the PNP), an effect known as crossover distortion which leads to a significant nonlinearity [8]. Like any electronics design it is up to the designer to choose between the trade-offs.

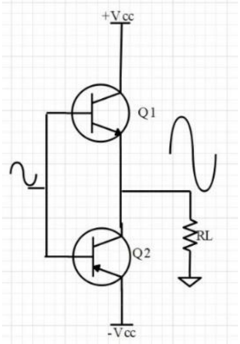


Figure 2: Class B complementary audio power amplifier schematic

1.1.1.3 Class AB

By combining the linearity of Class A amplifier and the efficiency of class B amplifier a structure called AB amplifier is created which offers both qualities. It is currently one of the most common types of power amplifier in existence. It is a variation of class B amplifier that allows both devices to conduct at the same time around the waveform’s crossover point, eliminating the crossover distortion problems of class B and enabling good sound quality [9]. This is done by biasing the push-pull stage of the class B amplifier with a small DC component. This means that the transistors conduct at the same time for small signals, increasing the risk of short circuiting the output stage [10]. In addition, its efficiency is still not satisfactory for most audio power amplifier designs.

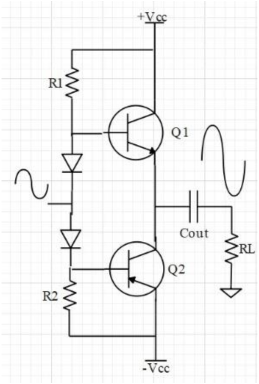


Figure 3: Common class AB complementary audio power amplifier schematic

1.1.2 Class D Audio Amplifiers

In the 1950s, a revolutionary new concept was brought to life: amplifying audio signals with active devices which are not operating in their linear gain mode but instead acting as electronic switches [11]. The first Class-D amplifier was invented by British scientist Alec Reeves in the 1950s and was first called by that name in 1955. The first commercial product released in 1964 suffered from the inconsistencies and limitations of the germanium-based BJT (bipolar junction transistor) transistors available at the time.

As a result, these early class-D amplifiers were impractical and unsuccessful. Practical class-D amplifiers were later enabled by the development of silicon-based MOSFET (metal-oxide-semiconductor field-effect transistor) technology. In 1978, Sony introduced the first class-D unit to employ power MOSFETs and a switching-mode power supply [11]. There were subsequently rapid developments in between 1979 and 1985. The availability of low-cost, fast-switching MOSFETs led to Class-D amplifiers becoming successful in the mid-1980s [12]. But the commercialization of class D audio amplifiers had to wait until the ‘90s when silicon (Si) MOSFETs with sufficiently good device parameters became widely available [11]. Unlike other classes of amplifiers, class D amplifiers operated in the active and cutoff regions only, hence not in the linear region. The MOSFETs used only acted as switches and were never on for the entire duration of operation, making their efficiencies better than the other classes.

1.1.3 Comparison of Audio amplifier classes

The goal of audio amplifiers is to reproduce input audio signals at sound-producing output elements, with desired volume and power levels—faithfully, efficiently, and at low distortion [4]. Audio amplifiers must have a good frequency response over the audible range of about 20Hz to 20kHz. The power capabilities of the audio amplifier can also vary widely depending on the application, from milliwatts in headphones to hundreds of watts and beyond for powerful home and commercial sound systems.

Class A amplifiers are the simplest and hence the most common type of amplifier classes. Class A means “the best class” of amplifier because of their low signal distortion levels and are probably the best sounding of all classes [9]. However, their major shortcoming is their very low efficiency making them impractical for professional audio applications. Low efficiency, due to the excessive power dissipation, implies more power burned on-chip, which can cause heating problems [9]. One method to remedy this problem is by using heat sinks to avoid the overheating of the device.

Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the class A amplifier [9]. Class B comprises of two transistors connected complementarily (push-pull), such that each transistor conducts for only one-half cycle of the input. This arrangement greatly increases its efficiency; however, it is at the cost of degraded linearity. During the crossover of the transistors neither device is ON, which leads to very bad crossover distortion in the output waveform; hence they have inferior sound quality.

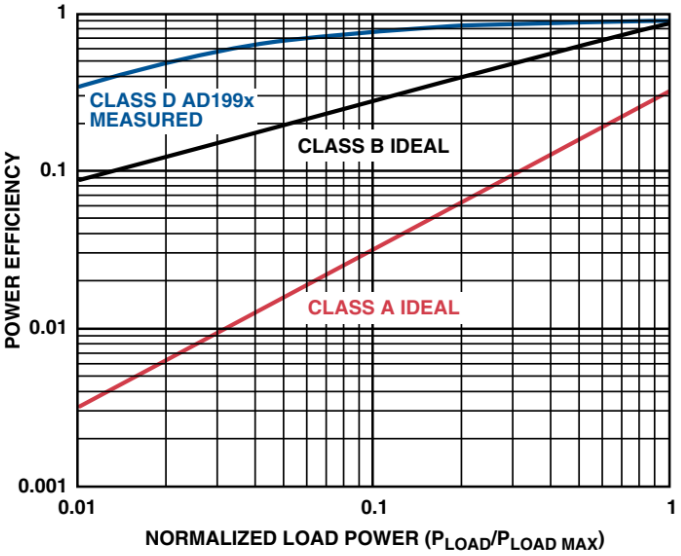


Figure 4: Power efficiency of class A (25%), class B (78.5%) and class D (90%) audio amplifiers [4]

Class AB amplifier is a hybrid compromise between class A and class B amplifiers in terms of efficiency and linearity [4], [9]. In this design, each of the complementary transistors is conducting for slightly more than the half cycle of conduction in class B but much less than the full cycle of conduction of class A [9]. With the drawback of having a limited output swing range due to headroom requirements it is terribly inefficient in terms of having a fixed supply for audio applications [9]. Some methods (such as employing push-pull output stage) are applied to compensate class-AB amplifiers, but when the power is high, power devices are still threatened and power output is limited, thereby the practical efficiency is 30%–40%, leading to a serious energy waste problem [13].

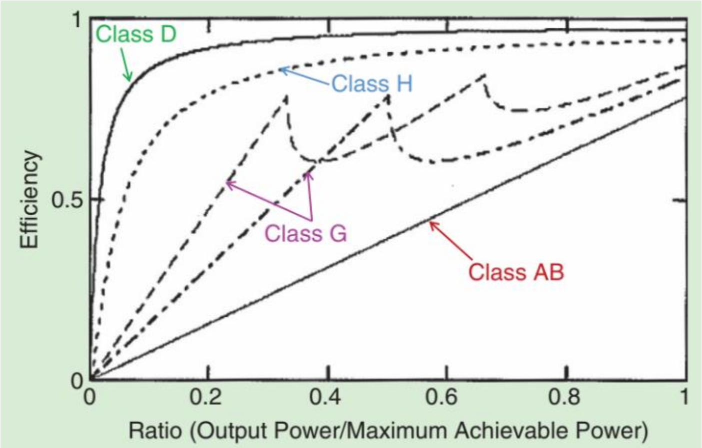


Figure 5: Ideal efficiencies of class AB, class G, class H and class D Amplifiers [9]

There are also other modifications of the class AB amplifier, such as class G and class H amplifiers with improved efficiencies. However, since they are all linear, the transistors operate in the linear region and directly amplify the analog signals resulting in a large power loss that inevitably hurts efficiency, as it can be seen in Figure 5 above [9], [13].

In contrast, class D amplifiers (or so-called switching amplifiers) theoretically can reach 100% efficiency because their transistors work on switching state. Even with practical drawbacks of a real implementation, class D audio amplifiers exceed the efficiency of traditional class A, class B, class AB, class G and class H audio amplifiers, as can be seen from the figures given above [14]. This exceeding efficiency lowers power dissipation; the lower power dissipation produces less heat, saves chip area and circuit board space, and extends battery life in portable systems [4], [13]. In contrast, the linearity achieved by class D audio amplifiers is worse when compared to the performance of their counterparts [14]. Therefore, the main task of a class D amplifier designer is to improve linearity and minimize quiescent power consumption while maintaining their high efficiency.

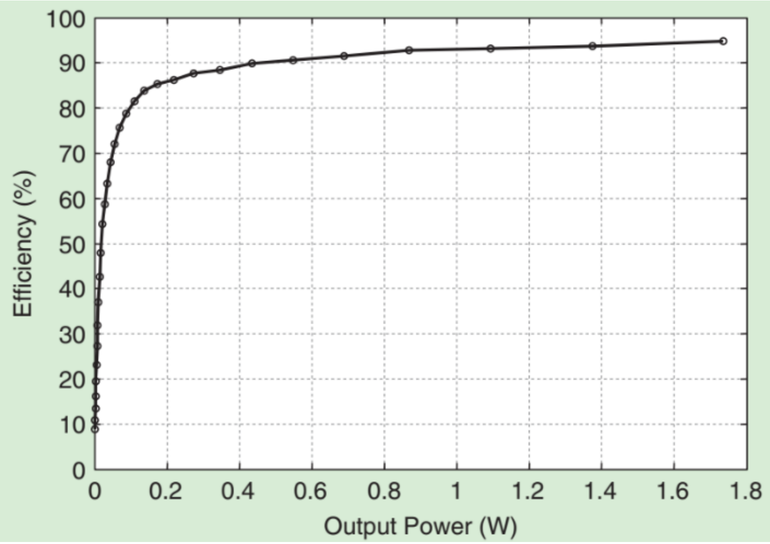


Figure 6: Measured efficiency of class D amplifier [9]

1.2. Gallium Nitride

The trade-offs in Class D audio have been limited by the performance capabilities of the output Field Effect Transistors (FET) amongst other reasons. Output FETs capable of switching at much higher speeds would allow for smaller passive circuit elements in the output filter and lower the dead-time needed to prevent shoot-through current. To improve the FET, the gate charge must be reduced, and the carrier velocity must be increased, which is not a possibility with the current state-of-the-art Silicon devices [6]. Therefore, researchers are exploring the option of using newly developed Wide Band Gap (WBG) materials like GaN technology to replace the current Silicon FETs.

1.3.Problem statement

Even though the majority of modern electronics is based on the mature and very well-established silicon semiconductors the demands and applications are quickly approaching the maximum performance capabilities of Silicon (Si) devices. Motivated by the desire for increased efficiency, new materials are now competing directly with Si technology which has proven to be limited with respect to blocking voltage capability, operation temperature, and switching frequency. Silicon semiconductors lack low ON-state resistance and faster and cleaner switching which are key device parameters in class D audio amplifiers to achieve higher audio performance and increased power efficiency. A new device GaN can be used to alleviate the aforementioned shortcomings of Si in class D amplifiers. Yet, as a new semiconducting technology, the practical applications of GaN have not been well studied.

1.4.Objectives

The inherent performance benefits of using GaN over Silicon in power electronics switching circuits with respect to faster switching speeds, higher power density, and higher power efficiency have been widely discussed in other previous works yet, little is shown to support the sonic advantages or disadvantages of using GaN in Class D audio amplifiers.

- To explore and understand Si based class D amplifier
- To explore and understand GaN based class D amplifiers
- To simulate and compare class D audio amplifiers using LT-Spice
- Demonstrate any benefits of using GaN over Si.
- Categorize any application specific disadvantages to GaN over Si.
- Contribute literature to this under-explored application of GaN.

1.5.Organization of the Thesis

The thesis is organized as follows: the first chapter outlines introduction of the thesis along with the objectives and the problems it is trying to solve. The second chapter describes the background needed including Class D amplifier design and GaN material properties. In the third chapter previous works related to the current thesis are reviewed. The fourth chapter describes the methodology used for this thesis work. Chapter 5 gives the results and discussions, while the final chapter concludes and gives proposed future works along with the limitations of the work.

Chapter 2

2. Background

2.1 Class D Amplifier Design

A class D amplifier is an electronic amplifier in which the amplifying devices (transistors, usually MOSFETs) operate as electronic switches, and not as linear gain devices as in other amplifiers. They operate by rapidly switching back and forth between the supply rails, being fed by a modulator using pulse width, pulse density, or related techniques to encode the audio input into a pulse train. The audio escapes through a simple low-pass filter into the loudspeaker [12].

The performance of class D amplifiers has been advancing incrementally with the evolution of Si MOSFET performance as the preferred transistor device technology. Recently however, as GaN-based high-electron mobility transistor (HEMT) devices with much better physical properties have become a reality, a leap in class D amplifier performance is on the doorstep [11].

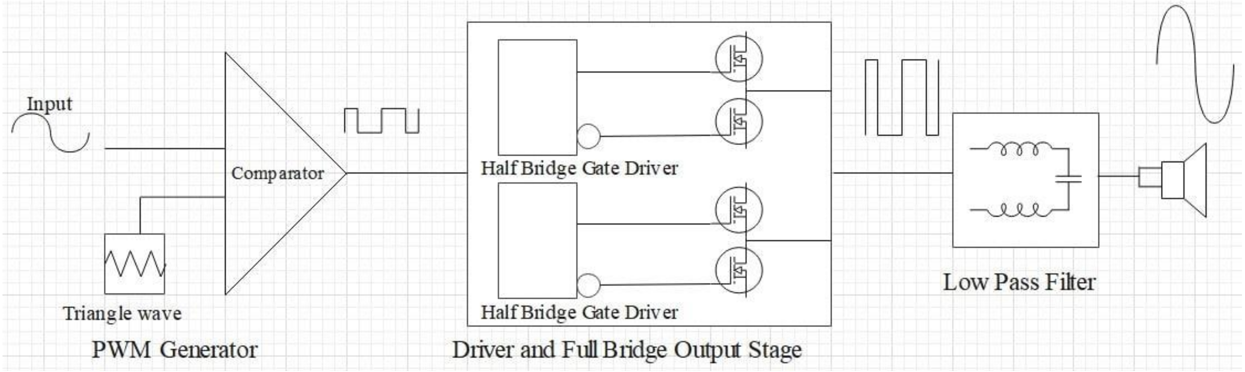


Figure 7: Block diagram of a basic Class D amplifier

It has a specific target group in the audio amplification market. This includes mostly amplification solutions with requirements which give high priority to small size and high efficiency. This implies most devices which use audio amplifiers in: consumer electronics (small to medium powered stereo sound systems, televisions multimedia speakers), car audio, portable devices (instrument amplifiers, laptops, portable music players, smartphones, tablets). With the booming growth of the latter aforementioned devices, Class D amplifier has a high potential of dominating the market as the solution of choice because there is a gap of efficiency with the next most efficient topology in line. The option of omitting the filter stage for small size designs (e. g. smartphones) is a nontrivial factor when analyzing the cost of production [8].

2.1.1 Operation of Class D amplifiers

A class D amplifier consists of three basic stages: modulation, power amplification and filtering. Input signal modulation is the core principle behind the high efficiency of Class D. Without it, the transistors would have to operate in the linear region for longer periods of time in order to amplify the same signal, thus dissipating larger amounts of heat and becoming inefficient. By modulating the input signal, the transistor is spending the least possible amount of time operating in resistor mode [8]. This signal is then used to drive the output stage devices. In the output stage there are two possible configurations, a half-bridge configuration and a full-bridge configuration. The output stage amplifies the input gating signal determined by the level of supply voltage. It is then demodulated by a low pass filter to filter out the high frequency components and recover the original signal and lastly this signal drives the speaker.

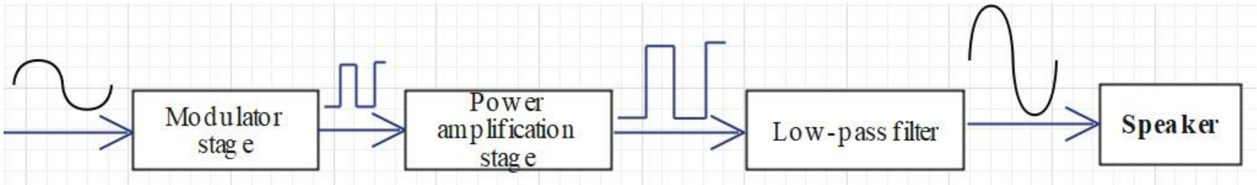


Figure 8: Class D amplifier block diagram

2.1.1.1 Modulation Stage

The modulation schemes are techniques that encode an input waveform into an output gating signal [16]. This stage is responsible for transforming the input signal in to pulses that drive the power MOSFETs efficiently. The signal can be sampled depending on a specific technique used like time, amplitude and frequency. The input audio signal is sampled to a series of high frequency pulses representing ON and OFF states which are used to drive the power MOSFETs. The four basic Pulse Modulation techniques are Pulse Amplitude Modulation (PAM), Pulse Position modulation (PPM), Pulse Density modulation (PDM) and Pulse Width Modulation (PWM).

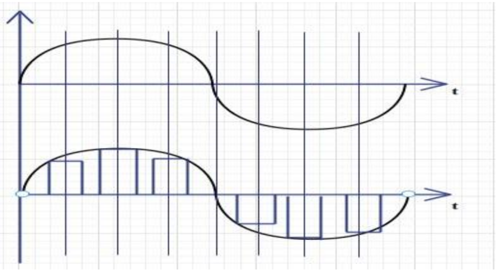


Figure 9: Pulse Amplitude Modulation (PAM)

PAM is a modulation system in which the signal is converted into amplitude-modulated pulses [8]. In this type of modulation, each sample is made proportional to the amplitude of the signal at the instant of sampling. The PAM signal follows the amplitude of the original signal, as the signal traces out the path of the whole wave, as it can be seen from Figure 9. However, PAM suffers when it comes to the amplification of the amplitude modulated pulses. The power stage cannot amplify accurately the pulses and this is why techniques which use two or three discrete amplitude levels, such as PPM, PDM and PWM, are much easier for the power stage to amplify.

In PPM the value of each instantaneous sample of a modulating wave is caused to vary the position in time of a pulse, relative to its non-modulated time of occurrence. Both the amplitude and width of the pulse are kept constant which gives the pulse identical shape independent of the modulation depth.

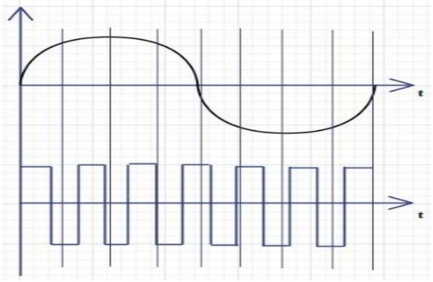


Figure 10: Pulse Position Modulation (PPM)

In general, PPM is an analog modulation technique where the amplitude and width of the pulse are kept constant, while the position of the pulse with respect to the position of a reference pulse is varied according to the instantaneous value of message signal [17]. The simple reproduction of uniform pulse with a simple switching power stage is its advantage. The power supply level of the switching power stage will have to be much higher than the required load voltage. This leads to sub-optimal performance on several parameters as efficiency, complexity and audio performance [8].

PDM is based on a unity of pulse height, width and a constant time of occurrence for the pulses within the switching period. The modulated parameter is the presence of the pulse. For each sample interval it is determined if the pulse should be present or not. It is appealing to have a unity pulse since this is easier to realize by a switching power stage.

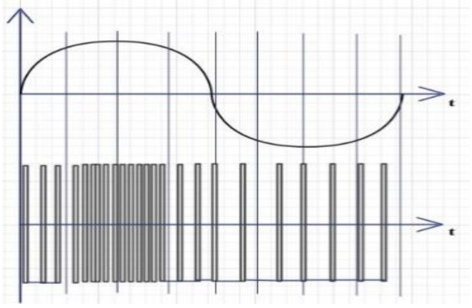


Figure 11: Pulse Density Modulation (PDM)

Another advantage of PDM is the simplicity of modulator implementation. There are reports that have been given regarding the use of PDM both in a digital modulator implementation and analog implementation with the power stage incorporated in the loop. However, the average switching frequency is higher than that obtainable with Pulse Width Modulation (PWM). This leads to lower performance and a considerably lower efficiency compared with PWM based topologies. A further disadvantage is the necessity for a high order loop filter in order to obtain a sufficient noise shaping effect. This is difficult to realize and limits the modulation depth of the modulator [8].

PWM is the sampling of the signal that results in pulses modulated by time [8]. As the name suggests, the width of the pulse is varied in proportional to the amplitude of the signal. Since the width is changing, the power loss can be reduced when compared to PAM signals [17]. The requirement for a high switching frequency introducing non-linear problem can be considered as one of its major disadvantages.

It is a technique that codes the amplitude of the input signal in the form of a duty cycle (a percentile of the supply voltage). The most common way this is achieved consists of a comparator being fed the input signal (analog) and a triangle/saw tooth wave. The result of the voltage difference between the two is a logic High if the input signal is higher than the triangle wave and a logic Low otherwise. Pulse width modulation is typically classified in two types, depending on the input signal's nature: natural sampled PWM (NPWM) and uniform sampled PWM (UPWM) [8].

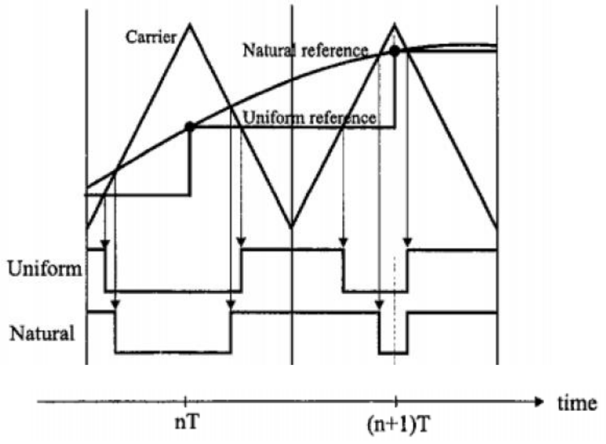


Figure 12: Basic PWM methods [8]

There are also Delta-Sigma (a discrete time technique, abbreviated as ΔΣ) and a new input modulation technique which includes the use of Digital Signal Processors (DSP) leading to significantly reduced noise.

2.1.1.2 Power Amplification Stage

The power amplification stage consists of MOSFETs arranged in either of two configurations to provide power gain, a half bridge configuration or a full bridge configuration. This stage amplifies the input gating signal determined by the level of supply voltage [16]. Power amplification of class D amplifiers occurs in this stage.

The half bridge configuration employs complementary MOSFETS, an N-channel MOSFET used for the low side and a P-channel MOSFET used for the high side connected in the common source configuration as shown in Figure 13 [18]. Since Q1 and Q2 transistors are complementary they will never be on at the same time; otherwise, it will short circuit. This might occur during transition times, when Q1 is turning OFF and Q2 is turning ON or vice versa, requiring an additional 'dead time' (a topic to be discussed later on) to avoid the short circuit. If a single power supply is used to bias the transistors, a DC bias voltage will be present across the speaker load, leading to power loss in the load and also damaging the speaker [6]. To avoid this a DC blocking capacitor must be used. In most cases, however, the half bridge configuration uses complementary power supplies (as shown in the figure below) in order to avoid using a large DC blocking capacitor.

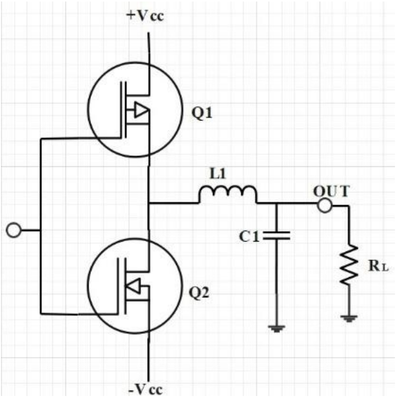


Figure 13: Half bridge configuration with an LC low pass filter

It is called a half bridge because it has half the components present in the corresponding full bridge configuration and offers a more economical and compact design. However, the design needs more care in order to have low distortion, low Electromagnetic Interference (EMI) and a good Total Harmonic Distortion performance (a topic to be discussed later on) [8]. Hence, it is not commonly used in class D amplifiers due to some of its inherent issues, which are remedied in the full bridge configuration.

Each MOSFET in the power amplification stage operates as a switch and switches between the on state and the off state complementarily. When a MOSFET is on, there is very little voltage across it and, therefore there is very little power dissipated even though it may have a high current through it [21]. This little power dissipation depends on the Figure of Merit (FOM), which in turn depends on the internal resistance between drain and source (R_{DSon}). Hence, to ensure high efficiency, R_{DSon} of the MOSFETs must be low [10]. On the other hand, when a MOSFET is off, there is no current through it and, therefore, there is no power dissipated. The only time power is dissipated is during the short switching time, ensuring the amplifier to have high efficiency.

Interestingly, N-channel MOSFETs have better switching characteristics with less power dissipation capabilities than that of corresponding P-channel devices. This is because the movement of electrons (the majority carriers in N-channel) is much faster than that of holes (the majority carriers in P-Channel). Therefore, in some cases, power amplification stages often employ N-channel devices for both the lower and the higher side instead of a complementary MOSFET. However, these devices require more complex driver circuits [18]. One of the requirements is a level shifter circuit that will give the inverted input of the higher side to the lower side, so that both NMOS will have complementary inputs, as shown in Figure 14.

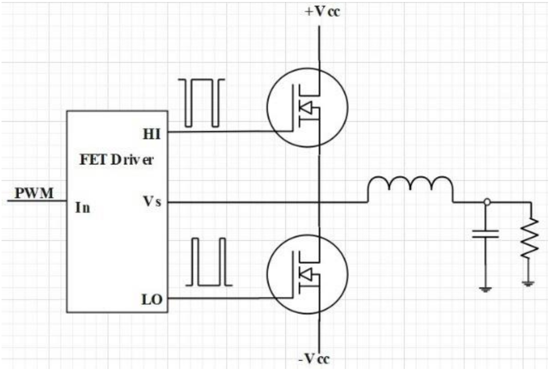


Figure 14: Half bridge with N-channel high side and low side MOSFETs

The full bridge or H-bridge is employed when the aim is to produce as much audio power as possible from a low-voltage supply. It is often referred to as a Bridge-Tied Load (BTL) in audio applications because it consists of a load connected between two half-bridge switching stages shown in Figure 15 [6]. It allows twice the voltage swing across the load, and therefore theoretically four times the output power, and also permits the amplifier to run from one supply rail without the need for bulky output capacitors of doubtful linearity [19].

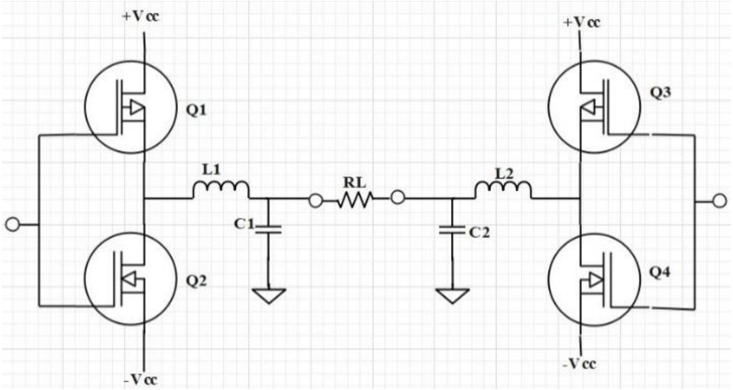


Figure 15: Full-bridge configuration with an LC low pass filter

The full bridge requires twice as many components, but only half the power supply voltage to realize a given output power capability, with the added advantage of cancelling DC offsets and harmonic distortion [18], [20]. The full bridge configuration, shown in Figure 15, operates in a similar fashion to its half bridge counterpart. The gating signals for Q1 and Q4 are the same, while those for Q2 and Q3 are the same. A full bridge configuration allows the load to have a differential output twice the supply, while also removing inherent DC component as well as rejecting inherent power supply [16]. Even though, the full bridge has a higher complexity and overall cost, it is still preferred in most designs because of its high Signal-to-Noise Ratio and lower distortion.

The most important differences between the two configurations can be depicted in the table below:

	Half Bridge	Full Bridge (BTL)
Supply Voltage	0.5 X 2 channel	1
MOSFET	2 per Channel	4 per Channel
Gate Driver	1 per Channel	2 per Channel
DC Offset	Adjustment Needed	Can be cancelled out
PWM Pattern	2 level	3 level can be implemented
Feedback	Needed due to pumping effect	Suitable for open loop

Table 1: Qualitative Comparison Between Half Bridge and Full Bridge Configurations

In the case where one MOSFET (or two for the full bridge configuration) starts conducting before the other one (or two for the full bridge configuration) stops, even for a brief amount of time, it causes a large shoot-through current to flow directly from the positive supply to the negative supply [8], [18], [19]. This overlap of the transistor switching times could occur due to the finite switching speeds of the transistors. This mode of operation not only reduces the overall efficiency of the amplifier because of the power dissipated due to the large current generating heat in the transistors; it can also severely - even irreparably - damage the MOSFETs [8], [18].

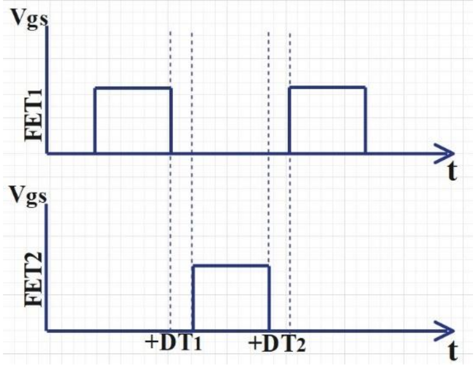


Figure 16: +DT1 and +DT2 dead-times inserted between the gating signals

As a practical and safety measure, a very small time-delay (dead-time) is added to the gating signal, as shown in Figure *16*, to ensure that there is always a very small time when both devices are turned off [16], [18]. This might add additional circuitry which adds an amount of delay to one rail so that the switching time does not coincide with that of the opposite transistor half [8]. However, the presence of this dead time causes distortion, so only the minimum is applied. A small amount of dead-time in the tens of nano-seconds can easily generate more than 1% of THD [22]. Therefore, the dead time needs to be carefully adjusted in order to minimize harmonic distortion while at the same time avoiding shoot-through current.

2.1.1.3 Filtering Stage

After being amplified, the signal contains large amounts of high frequency energy that need to be filtered out in order for the audio signal to be driven to the load. To filter this high frequency energy a low pass filter is needed to block any signal containing higher frequencies than the corner frequency. The corner frequency of the filter is chosen so that the filter will have minimal effect on the desired output frequency range while attenuating the switching noise as much as possible [8]. It is almost impossible to remove all unwanted switching signal which is the major source of noise and distortion for this class of amplifiers.

While some low-power integrated applications have no output filter at all, most Class-D amplifiers have a second-order LC filter between the amplifier output and the loudspeaker. In some cases, a fourth-order filter is used [19]. Usually, Butterworth alignment is chosen to give maximal flatness of frequency response.

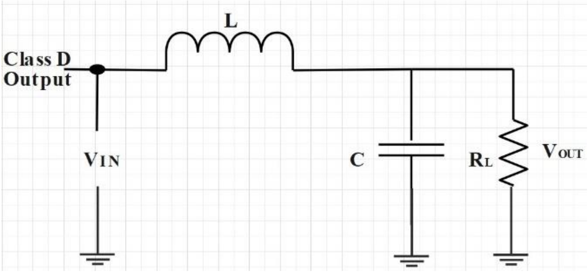


Figure 17: A single ended typical low pass LC filter

In a Low-Pass Filter the optimum value for the filter inductor (L) and capacitor (C) is

$$C = \frac{1}{\sqrt{2} \cdot R_L} = \frac{1}{2 \cdot \pi \cdot f_c \sqrt{2} R_L}$$

$$L = \frac{1}{C} = \sqrt{2} \cdot R_L = \frac{\sqrt{2} \cdot R_L}{2 \cdot \pi \cdot f_c}$$

where $\mathbf{f_C}$ is the desired corner frequency of the filter and $\mathbf{R_L}$ is the load (speaker) resistance. since the inductor value is dependent not only on the corner frequency but also on the load resistance so it will vary depending on the speaker impedance change.

There are also filter less class D amplifiers that operate without the filter stage. Even if there is a large amount of high-frequency switching noise on the outputs, this noise is far outside of the response range of most speakers so it is not necessary to include filters for a good audio quality [24]. However, this filter less class D amplifiers are less efficient since the high-frequency energy that is filtered(absorbed) by the filter stage is now dissipated as electromagnetic interference and heat.

2.1.2 Noise

One of the downsides of Class D amplifiers is the large amount of high-frequency switching noise created by the modulated pulses. Even if it is far outside the audible frequency, it is still dissipating power. There is also unavoidable noise generated in different parts or stages of class D amplifier driven to the speaker that impairs the overall sound quality. Therefore, it is critical to decrease the noise figure as much as possible to its least possible point since the audio quality is a very important aspect of the audio amplifier performance.

Noise is a general concept which is quantitatively defined by its two subtypes: general noise which is portrayed by the Signal-to-Noise Ratio (SNR) of the output and harmonic noise which relates directly to the Total Harmonic Distortion (THD) figure [8].

2.1.2.1 Signal to Noise Ratio (SNR)

A Signal to Noise Ratio is a parameter that describes the ratio of the signal power to the noise power in a system. It is considered to be the ratio of the final amplified signal power to the final amplified noise power and it’s measured on the output of the filtering stage. Even though it is impossible to remove this noise entirely it can be reduced by designing it carefully.

A random thermal excitation in the silicon and any sort of background noise in the input signal is the source of the noise reducing the SNR. Since a higher SNR means a higher output quality it is very important to keep the SNR as high as possible [8].

2.1.2.2 Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency; it measures the harmonic distortion present in a signal. Clipping of the audio signal in modulation stage, non-idealities in the transistor, non-linearity in the amplifier are some of the factors that contribute to the harmonic disorder. The clipping of signal can be avoided by carefully monitoring input levels and the non-linearity can be reduced by taking good care of the modulation technique and filtering quality. Keeping the THD as low as possible leads to a higher power factor, lower peak current and higher efficiency for class D audio power amplifiers.

2.1.3 Applications of Class D amplifiers

The present electronic industry aims at small volume, low power and high efficiency devices [13]. Class D audio amplifiers are preferred over the other linear classes of audio amplifiers in applications that need more efficiency than audio quality. It is also advantageous for portable devices because it does not contain any extra heat sink arrangements making it easy to carry around. Since the power efficiency of class D amplifiers is very high it can preserve the battery lifetime in portable electronics products. It has become the standard in consumer electronic product applications such as:

- Mobile technology,
- Television sets and home-theatre systems,
- Automotive,
- Hearing aids,
- Headphone amplifiers,
- High volume consumer electronics,
- Active subwoofers,
- Powered speakers,
- Sound reinforcement systems,
- Bass instrument amplification,
- RF amplifiers

2.2 Gallium Nitride (GaN) in Class D Audio Amplifiers

2.2.1 What is Gallium Nitride (GaN)?

Gallium Nitride (GaN) was first synthesized using hydride vapor phase epitaxy (HVPE) in 1969 but didn’t realize its true potential until 1991 when suitable metalorganic chemical vapor deposition (MOCVD) equipment was developed for GaN [25]. It is a very hard, mechanically stable wide bandgap semiconductor that has a faster switching speed, higher breakdown strength, lower on-resistance and higher thermal conductivity as compared to Si, the material traditionally used for electronic devices. These properties permit the creation of smaller devices which consume less energy and can operate at higher frequencies, a feat appealing for power devices.

2.2.1.1 GaN Fabrication

Unlike most semiconductors, GaN is not found in nature and is purely a man-made material [25]. GaN devices can be fabricated on a variety of substrates, including bulk GaN crystal, Silicon Carbide (SiC), Sapphire (Al_2O_3) and Silicon (Si) [26]. Growing GaN epitaxial layer on top of silicon enables it to use the widely available and highly specialized manufacturing technology infrastructures of Silicon while at the same time eliminating the need for costly specialized production sites from scratch. Thus, addressing the immaturity of processing and fabrication removes the primary obstacle preventing GaN materials from equal market share with its Si equivalent. Si substrates can be used for devices in more cost-sensitive commercial applications such as DC-DC conversion, AC-DC conversion, class D audio amplifiers and motion control [26]. Furthermore, GaN is used in the production of semiconductor power devices as well as RF components and analog applications such as light-emitting diodes (LEDs) because of its capability to be the displacement technology for silicon.

2.2.1.2 History of GaN

GaN devices first made an impact in about 2004 with depletion-mode RF transistors made by Eudyna Corporation in Japan [6]. Using GaN-on-SiC substrates, Eudyna successfully produced transistors with benchmark power gain in the multi gigahertz frequency range designed for the RF market [15]. In 2005, Nitronex Corporation introduced the first depletion mode RF transistor made with GaN grown on silicon wafers [26]. GaN RF transistors have continued to make inroads in RF applications but the acceptance outside this market, however, has been limited by device cost as well as the inconvenience of depletion mode operation.

In June 2009 Efficient Power Conversion Corporation (EPC) introduced the first enhancement-mode GaN on silicon power transistors designed to be drop-in improvements for their Si counterparts [6]. These products were designed to be produced in high-volume at low cost using standard silicon manufacturing technology and facilities. Currently, Matsushita, Transphorm, GaN Systems, ON Semiconductor, Panasonic, TSMC, Navitas, Infineon, and others are pursuing the manufacture of GaN transistors.

2.2.2 GaN High Electron Mobility Transistor (HEMT)

HEMTs, also called heterostructure FETs (HFET) or Modulation Doped FETs (MODFET) are field effect transistors (FET) for which the channel is generated by the heterojunction of two materials that have different band gaps instead of doping different regions [27]. The HEMT was first announced by Fujitsu Laboratories in 1980 using GaAs/AlGaAs heterojunction [28]. In which successful fabrication of a new heterojunction FET, which they called a High Electron Mobility Transistor (HEMT), with extremely high-speed microwave capabilities was reported. This GaAs/AlGaAs combination has been widely used for

HEMT ever since. One major feature of HEMT was the ability to be applied to a variety of compound semiconductors apart from the conventional GaAs HEMT [29]. Lately, research and development of high efficiency/high output HEMTs using GAN has attracted considerable interests because of their outstanding electronic properties.

GaN HEMT utilizes high-density two-dimensional electron gas (2DEG) accumulated in the boundary layer between GaN and AlGaN through their piezoelectric effect and natural polarization effect [30]. This natural polarization occurs because inside the Gallium Nitride crystal the individual atoms are electronically charged and the large Gallium and small Nitrogen atoms are arranged somewhat irregularly with respect to each other, because of the difference in size, which leads to a spontaneous polarization within the crystal, or a separation of charge into countless, regularly spaced negative and positive atoms [31]. This polarization, however, does not accumulate in an ordinary GaN crystal because of the overall cancellation of the oppositely charged regions. But this cancelling out doesn't occur where the GaN crystal ends abruptly, such as at a heterojunction with AlGaN, which gives rise to an electrically charged region at the boundary.

The charged, polarized region is augmented, furthermore, by a piezoelectric polarization, which arises from the strain caused by the coming together of the two different crystal lattices [31]. If the GaN crystal lattice is subjected to strain, the deformation will cause a miniscule shift in the atoms in the lattice and generate an electric field (voltage) – the higher the strain, the greater the electric field [26], [29]. When a very thin layer of AlGaN is grown on the surface of the GaN crystal, a lot of strain over a very small distance at the interface is created that induces a piezoelectric polarization near the AlGaN layer and hence a compensating two-dimensional electron gas (2DEG) at the interface [32]. This 2DEG, formed without the application of external electric field, can be used to efficiently conduct large amounts of current when an electric field is applied across it.

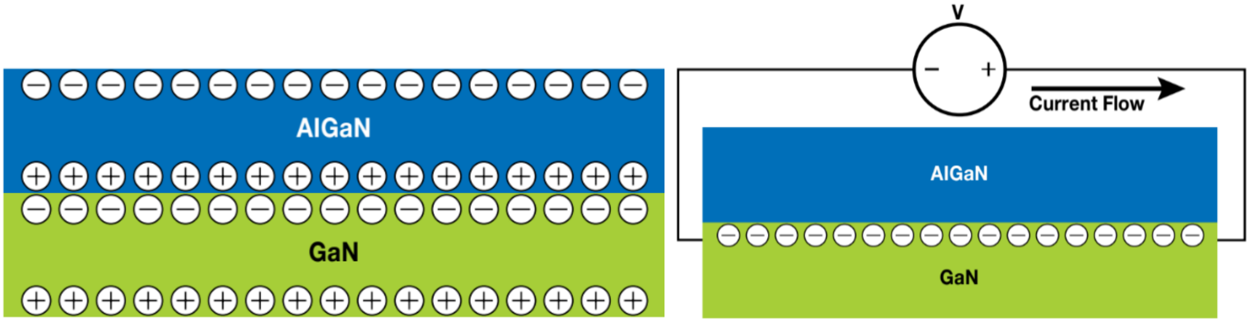


Figure 18: a) Simplified cross section of a GaN/AlGaN heterostructure showing the formation of a 2DEG, b) By applying a voltage to the 2DEG an electric current is induced in the crystal [26]

The 2DEG is a gas of electrons free to move in two dimensions, but tightly confined in the third [27]. This confinement causes the 2DEG to be highly conductive by increasing the mobility of electrons from about

1000cm^2/V·s in unrestrained GaN to between 1500 and 2000cm^2/V·s in the 2DEG region [26]. The high sheet-carrier density of the 2DEG and large critical breakdown electric field allow the HEMT devices with unprecedented high drain current density and large breakdown voltage, which are essential for the important applications of power devices [33]. The increase of the mobility of electrons is the basis for GaN to be used in high frequency applications and as HEMT devices as well.

Another way to approach the concept of GaN HEMTs is by using energy bands and their diagrams. When a heterojunction is formed in HEMTs, the conduction band and valence band throughout the material must bend to form a continuous level [34]. For GaN-based HEMT, this heterojunction is formed from AlGaN and GaN, in which AlGaN has a wider bandgap than GaN. The wide band element (AlGaN) has excess electrons in the conduction band due to polarization charge and the narrow band material (GaN) has conduction band states with lower energy.

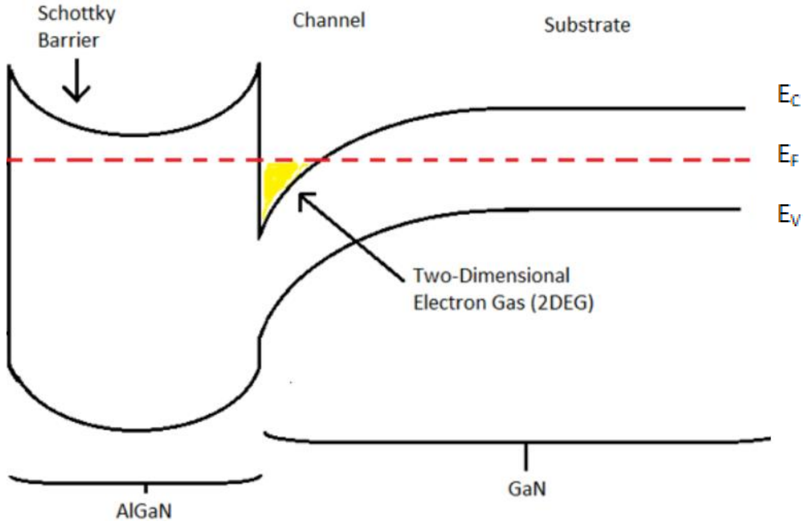


Figure 19: Energy band diagram of GaN HEMT and 2DEG formation [35]

Therefore, electrons will diffuse from the conduction band of AlGaN to the adjacent conduction band of GaN as it has states with lower energy [32]. Thus, a change in potential will occur due to movement of electrons and an electric field will be induced which will drift electrons back to the conduction band of AlGaN. This process of drift and diffusion will continue until an equilibrium junction is reached. GaN now has excess electrons and no donor atoms to cause scattering, which yield high switching speed and high mobility [34]. This diffusion of carriers leads to the accumulation of electrons along the boundary of the two regions inside GaN.

These accumulated electrons are also known as two-dimensional electron gas (2DEG). The generalized band diagram formed at the heterojunction for typical GaN HEMTs is as shown in Figure *19*. It can be inferred that both the conduction band (E_c) and valence band (E_v) bend with respect to the Fermi level (E_F) resulting in a quantum well filled with 2DEG and eventually, a conducting channel as well.

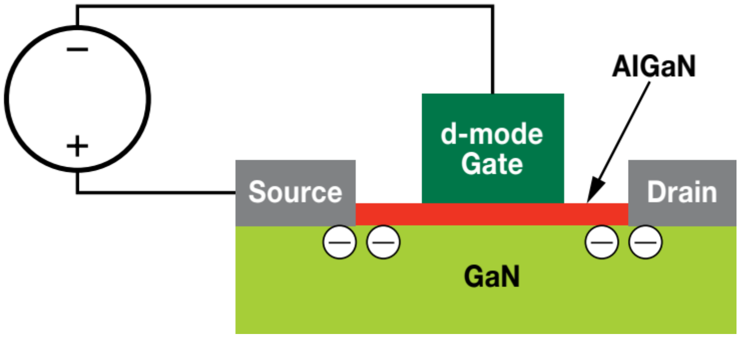


Figure 20: A d-mode device in which the electrons are depleted by applying a negative voltage [[26]]

There are two common modes of GaN HEMTs, namely, depletion-mode (d-mode) and enhancement-mode (e-mode). The depletion mode transistor, also known as a normally on device, requires negative voltage relative to both drain and source electrodes to be applied at the gate to deplete the 2DEG. Otherwise the source and the drain will always be short circuited because of the 2DEG in the channel, hence the name normally on device. There are two common ways to produce a d-mode HEMT device, the first is by using a Schottky barrier gate and the second is by using an insulating layer and a metal gate like a MOSFET.

On the other hand, an e-mode device is OFF and will not conduct with zero bias at the gate. The channel (2DEG) is enhanced or created by applying a positive voltage at the gate. There are five popular structures that have been used to create enhancement-mode devices: recessed gate, implanted gate, pGaN gate, direct drive hybrid, and cascode hybrid [26]. In power conversion applications, e-mode devices are preferred over d-mode because a short circuit will result unless a negative bias is first applied to the power devices.

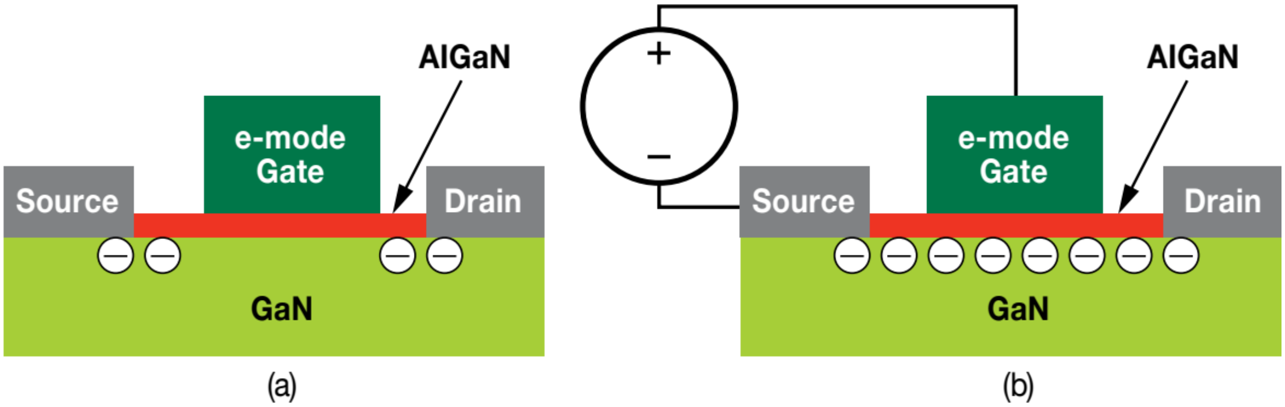


Figure 21: (a) An e-mode device depletes the 2DEG with zero volts on the gate. (b) By applying a positive voltage to the gate, the electrons are attracted to the surface, re-establishing the 2DEG [26]

GaN HEMT is used in high-frequency products like cell phones, voltage converters, radar equipment and satellite television receivers, mainly because of their operability at higher frequencies than ordinary transistors [27]. High frequency GaN HEMT is an indispensable component for power amplifiers for transmission of wireless communication systems and radar systems, which need high-output-power and high-efficiency performance [30]. GaN HEMTs are well suited for high-power switching applications, with a projected ×100 performance advantage in the square breakdown voltage per specific on-resistance figure of merit (V_{BR}^2/R_{ON}) over silicon power devices [36]. GaN HEMTs can achieve 2DEG with sheet carrier concentrations of up to $2\text{x}10^{13}\text{cm}^{-2}$ close to the interface due to their piezoelectric and spontaneous polarization even without intentional doping [31], [37]. Because of their high speed and low loss switching performance, they are attractive for applications in switching power supplies with ultrahigh bandwidth (in the megahertz range) and microwave power devices for base stations of cellular phone.

2.2.3 GaN Material property

In term of power devices, most of the current research is focused on wide bandgap materials, such as GaN since silicon transistors are reaching their performance limits.

Material Property	Si	GaN
Band Gap (eV)	1.12	3.39
Critical Breakdown Electric Field (MV/cm)	0.23	3.3
Electron Mobility (cm^2/V-sec)	1350	2000 (2DEG)
Electron Saturation Velocity (10^7cm/sec)	1.0	2.5
Thermal Conductivity (Watts/cm K)	1.5	1.3

Table 2: Material Properties of Silicon and GaN

It is evident that GaN has material properties that make them better suited for power applications when compared to silicon in the above table. GaN has a higher critical breakdown electric field, making GaN based transistors preferable for high voltage applications. It has higher electron mobility and saturation velocity than Si, which improve the conductivity of the devices. For transistors with the same size and breakdown voltage, GaN transistors can provide a lower R_{on} compared to silicon. However, the thermal conductivity of GaN is almost the same as silicon, making them similar in heat dissipation [16]. Therefore, utilizing all material properties which makes them better suited for power applications, it is possible to design a class D amplifier with lower power loss and distortion compared to their silicon counterparts.

2.2.3.1 Bandgap (E_g)

The bandgap of a semiconductor is related to the strength of the chemical bonds between the atoms in the lattice. These stronger bonds mean that it is harder for an electron to jump from one site to the next. Among the many consequences are lower intrinsic leakage currents and higher operating temperatures for higher bandgap semiconductors [[26]]. GaN has these advantages over silicon since it has higher bandgap (3.39 for GaN over 1.12 of Si) than silicon as Table *2* shows.

2.2.3.2 Critical Field (E_{crit})

Strong chemical bonds cause a higher critical electric field needed to initiate impact ionization, which results in avalanche breakdown. The voltage at which a device breaks down can be approximated with the formula:

$$V_{BR} = {}^{1}\!/_{2}\, W_{drift} \cdot E_{crit}$$

The breakdown voltage of a device (V_{BR}) is therefore proportional to the width of the drift region (w_{drift}) [[26]]. Since the critical electric field of GaN is about 10 times higher than Si, the number of electrons in the drift region can be 100 times greater with only one tenth the distance to travel, which is why GaN outperforms Si in power conversion.

2.2.3.3 On-Resistance ($R_{DS_{(on)}}$)

The specific on-state resistance of any semiconductor device used for power electronic applications is one of the key performance parameters. An ideal power switching device should have a high breakdown voltage and its on-state resistance should be as small as possible.

The theoretical on-resistance of a one square millimeter majority-carrier device (measured in ohms [$\Omega \cdot mm^2$]) produces the following relationship between breakdown voltage and on-resistance:

$$R_{DS(on)} = 4 \cdot V_{BR}^{2} / \varepsilon_o \cdot \varepsilon_r \cdot \mu_r \cdot E_{crit}^{3}$$

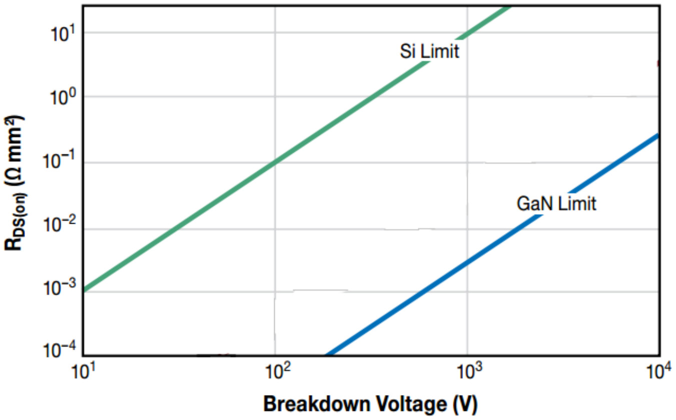


Figure 22: Theoretical on-resistance versus breakdown voltage for Si and GaN based power devices

This equation is then plotted as shown in Figure *22* for Si and GaN.

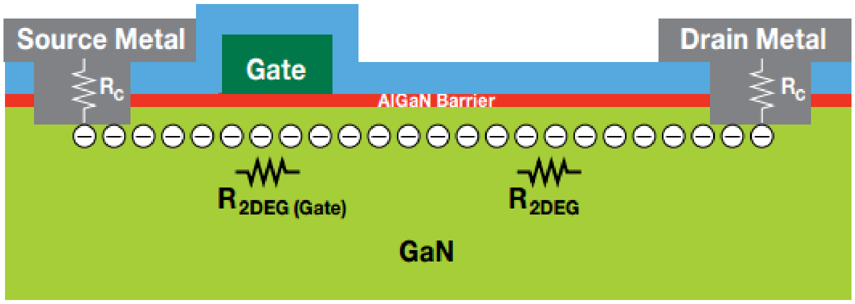


Figure 23: Cross section of a GaN transistor showing the major components of RDS (on) [26]

Another way to explain the concept of on-resistance is using Figure *23*. The following equations will also help derive the drain to source resistance ($R_{DS\ (on)}$). The electrons flow in the 2DEG with a resistance R_{2DEG} which is expressed by the equation:

$$R_{2DEG} = L_{2DEG}/(q \cdot \mu_{2DEG} \cdot N_{2DEG} \cdot W_{2DEG}$$

Where: μ_{2DEG} is the mobility of the electrons

N_{2DEG} is the quantity of electrons created by the 2DEG

L_{2DEG} is the distance the electrons must travel

W_{2DEG} is the width of the 2DEG

q *is* the universal charge constant, q ($1.6 \cdot 10^{-19}$ C)

The number of electrons in the 2DEG will depend on the amount of strain induced by the AlGaN barrier. However, the 2DEG could have a lower concentration beneath the gate than in the region between the gate and drain electrodes, depending on the type of gate, the particular process used, as well as the heterostructure deployed. It also depends on the voltage applied to the gate. A fully enhanced gate will have a higher electron concentration than a partially enhanced gate. A good approximation of the resistance of the transistor shown in Figure *23* can then be calculated as follows:

$$R_{HEMT} = 2 \cdot R_C + R_{2DEG} + R_{2DEG(gate)}$$

Where: R_C is the contact resistance which connects the source and drain metals to the 2DEG through the AlGaN barrier.

$$R_{DS(on)} = R_{HEMT(fully\ enhanced)} + R_{parasitic}$$

Where: $R_{parasitic}$ comes in from the multiple metal buses that conduct the current from the individual source and drain electrodes to the terminals of the transistor.

2.2.3.4 Figure of Merit (FOM)

One common way to express the relative performance excellence of eGaN FETs over power MOSFET is the Figure of Merit (FOM). Although more specialized FOMs exist for advanced comparisons, basic FOM is defined as the product of a device's $R_{DS(ON)}$ and the total gate charge, Q_G [26]. In other words, it is defined as a device's on-resistance multiplied by the total charge that must be supplied to the gate to switch the device at operating voltage and current [15]. This FOM has proven to be useful in predicting a device's performance in a power conversion system, i.e., the lower the FOM, the lower the power losses from conduction and switching [38]. In Figure *24*, a comparison of FOMs between several state-of-the-art power MOSFETs and EPC's eGaN FETs is presented, showing that the eGaN FET has an FOM more than a factor of 10 lower than silicon.

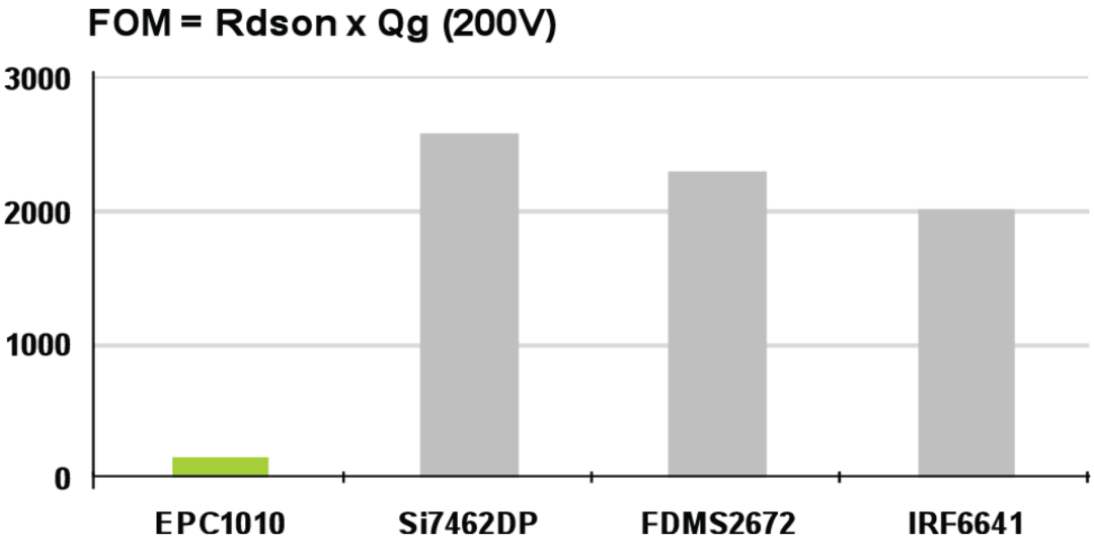


Figure 24: Comparison between 200V power MOSFET and eGaN FET figure of merit [38]

2.2.4 Modeling of Power GaN HEMTs

For any power-conversion application, the power circuit designers must evaluate the impact of the power-semiconductor devices used in the circuits using simulation tools and device models for the corresponding power-semiconductor devices [43]. The main objective of semiconductor device modeling is to achieve a predictive description of the device performance at some specific conditions such as bias (e.g., applied voltages and currents), environment (e.g., temperature, radiation), and physical characteristics (e.g., geometry, doping levels) [44]. There are various modeling approaches for GaN-HEMTs in the literature. Formulation of a valid model involves trade-off between accuracy and computational speed to analyze the device operation in a circuit [44]. In general, GaN-HEMT modeling can be classified into four categories: Behavioral models, semi physics-based models, physics-based models, and numerical models [43], [44].

Physics-based (Analytical) Model was developed by studying the physical phenomena that occur during the device operation based on the specific device parameters [44]. It involves solving semiconductor physics equations to obtain the electrical behavior of GaN-HEMTs [43]. This model is very accurate in predicting device behavior but includes very complex equations making it very time consuming for power electronics simulation.

Behavioral (Empirical) model is a popular modeling approach that fits mathematical equations to experimental data without considering the actual physical mechanism to predict device operation [43], [44]. Its major advantage is computational efficiency that provides a very fast simulation, but accuracy becomes compromised once operating conditions go beyond the fitting conditions.

Semi-Physics (Semi-Empirical) models attempt to establish a balance between the accuracy obtained from physics-based model and the simulation speed from empirical model [44]. These models are accurate, fast, and applicable to different devices from the same class even though some of their empirical parameters lack physical meaning [43]. Therefore, these models are preferrable for most practical operations such as, SPICE based circuit simulators.

First Author	Year	Model Level	Contributions	Simulation Tool
Yigletu [45]	2013	Physics	Accurate determination of 2DEG charge density.	ADS
Okamoto [46]	2011	Behavioral	Power loss estimation made by the model for an ac-ac direct converter.	SPICE
Waldron [47]	2013	Semi-Physics	Statz model, utilized to model both static and switching characteristics of GaN HEMTs.	SPICE
Strauss [48]	2014	Numerical	Calibration guide for device modeling.	Synopsis TCAD

Table 3: Published GaN Power HEMT Models and Their Contributions

Numerical model requires detailed information regarding internal structure, device geometry, and material properties of the GaN-HEMT and uses complex simulation tools such as SILVACO, TCAD, Sentaurus, MEDICI etc. [43]. Numerical models are used as virtual environment for device optimization under different conditions and the results can be used to validate the simulation model for other operating conditions which are otherwise very expensive and time consuming to achieve by actual measurement [44]. Their accuracy is good, but computation is very intensive with very high complexity.

Many GaN models have been developed using the four modeling categories. They each have their contributions to the overall progress of modeling GaN. Since there is no standardized model, the use of any of the models depends on the particular purpose required. Some of the published power GaN HEMT models have been mentioned in **Error! Reference source not found.** along with their corresponding contributions.

Modeling a GaN-HEMT requires mathematical equations for the drain current (I_D) as a function of the applied gate-to-source (V_{GS}) and drain-to-source (V_{DS}) voltages. In SPICE, there are different sets of equations, referred to as model levels, MOSFET LEVEL 3 is utilized to model GaN-HEMTs Since its key equations are almost as simple as in MOSFET LEVEL 1 and as accurate as the complex equation in the MOSFET LEVEL 2 model.

The equations shown below, represent the selection from MOSFET LEVEL 3 model, for the purpose of modeling GaN-HEMTs.

$$I_D = \frac{\boldsymbol{KP}}{1+\boldsymbol{Theta}(V_{GS}-\boldsymbol{Vto})} \frac{\boldsymbol{W}}{\boldsymbol{L}}(V_{GS} - \boldsymbol{Vto})(V_{DS} - \boldsymbol{Rs}I_D - \boldsymbol{Rd}I_D) - \left[1 + \frac{\boldsymbol{Gamma}}{2\sqrt{\boldsymbol{Phi}}}\right] \frac{(V_{DS}-\boldsymbol{Rs}I_D-\boldsymbol{Rd}I_D)^2}{2} \text{Triode Region}$$

$$I_D = \frac{\boldsymbol{KP}}{1+\boldsymbol{Theta}(V_{GS}-\boldsymbol{Vto})} \frac{\boldsymbol{W}}{\boldsymbol{L}}\left[\frac{2\sqrt{\boldsymbol{Phi}}}{2(2\sqrt{\boldsymbol{Phi}}+\boldsymbol{Gamma})}\right](V_{GS} - \boldsymbol{Vto})^2 \times \text{ Saturation Region}$$

Where:

KP: is the transconductance parameter

Vto: the threshold voltage

L, W: the channel length and width

Rd: drain resistance

Rs: source resistance

Gamma: body-effect parameter

Phi: the surface potential in strong inversion

Theta: the mobility modulation constant

In [43], a 600 V GaN Power transistor, manufactured by GaN Systems (GS66504B) was used along with an Agilent Power Device Analyzer (B1505A) to measure the transfer characteristic and extract the values of KP = 8.79 A/V^2, Vto = 1.26 V, Rs = Rd = 27.15 mΩ. Along with the set values of W = L = 1 µm and Phi = 2 V and the default values Theta = 0, and Gamma = 0, the non-linear fitting was applied to the above two Equations to give the GaN-HEMT model. This model was plotted against the measured value of the I_D Vs V_{GS} and I_D Vs V_{DS}.

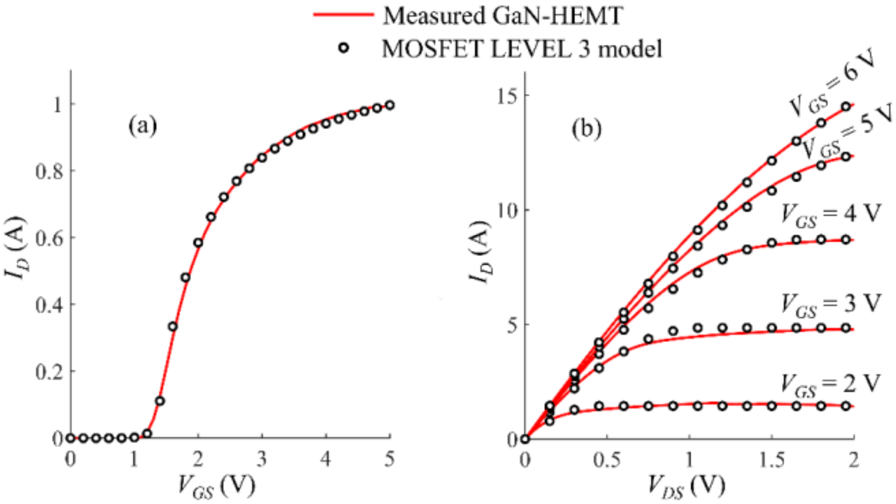


Figure 25: Verification of MOSFET LEVEL 3 model for GS66504B [44]

From Figure *25* it is evident that the SPICE simulations are in very good agreement with the measured results. This demonstrates that the MOSFET LEVEL 3 equations can be used to model GaN HEMTs for SPICE simulations.

Chapter 3

3. Literature Review

There are very few researches undertaken in the novel field of GaN based class D amplifiers. There are many researches undertaken on GaN material for various applications and many researches on silicon-based class D amplifiers, but very few engendering the two. Hence, it was a very arduous task to review literature written in this field. Here some of the literature reviewed have been presented, the papers by Joshua Chung [39] and by Jordan Sangid [41] were both based on their corresponding MSc Thesis, which was a comparison of GaN and Si based Class D amplifiers. In order to have a little bit of perspective, a paper based on GaN Class D amplifier by Allyfrahy [40] and another one based on maximizing the efficiency of Si based Class D amplifier by A. I. Colli-Menchi [42] were also added.

In [39] Joshua Chung et al. studied the performance of a single ended, open-loop 25 W full-bridge class D audio power amplifiers using a Pulse Density Modulation Scheme. They compared the performance of GaN and Silicon in the output stages based on their distortion, efficiency, and thermal effects. The GaN power HEMT chosen was an enhancement mode device from GaN Systems, while the silicon power device was a NexFET from Texas Instruments (TI). An FPGA was used to generate the Pulse Density Modulation signal along with the necessary dead time and delays.

In [40] Allyfrahy N. Alves et al. designed a 1KWrms Class D audio power amplifier with GaN switches using full bridge topology using unipolar Sinusoidal Pulse Width Modulation (SPWM). The simulation was performed using the PSIM software and the proceeding prototype was also designed. The GaN transistor used in the simulations was the TPH2112PS model from the company transphorm, while for the prototype the GaN FET model LMG341Xr050 was used from the company Texas Instruments.

In [41] Jordan Sangid et al. provided a side-by-side comparison of enhancement-mode GaN devices with currently available silicon MOSFETs with 60V drain-to-source voltage ratings for class D amplifier applications. A single-ended self-oscillating Class D amplifier topology was chosen with interchangeable output FET modules to achieve a side-by-side comparison of GaN and Si FETs. The selected devices consisted of examples from the EPC eGaN – FET series, Texas Instruments (TI) NexFET series, and Infineon’s OptiMOS – 3 series.

In [42] A. I. Colli-Menchi and E. Sanchez -Sinencio implemented a high-efficiency self-oscillating class D amplifier for piezoelectric speakers using stacked-cascode CMOS transistors with H-bridge topology. This configuration provided low input capacitance to allow high switching frequency to improve linearity with high efficiency. A prototype was produced based on these parameters.

Author	Year	Material	Topology	Peak Efficiency
Joshua Chung et al. [39]	2016	GaN	Full Bridge	82.3%
Joshua Chung et al. [39]	2016	Si	Full Bridge	67%
Allyfrahy et al. [40]	2020	GaN	Full Bridge	97.2%
Jordan Sangid et al. [41]	2018	GaN	Half Bridge	93.2%
Jordan Sangid et al. [41]	2018	Si (TI)	Half Bridge	90.7%
Jordan Sangid et al. [41]	2018	Si (Infineon)	Half Bridge	90.4%

Table 4: Summary of Reviewed Articles

The basic challenge for the comparison of audio power amplifiers is the lack of standards for performance metrics [6]. Due to this perceived inconsistency, the metrics used to compare the literature reviewed in this text will be the best claimed or interpreted performance levels consistent with typical operating levels. The audio power amplifiers reviewed offer a wide range of performance as shown in Table *4*. It can also be inferred from the table that the full bridge topology offers a better efficiency, however, since the analysis of Chung et al. [39] was performed on the hardware device it has a very low efficiency.

Since GaN HEMT shows a lower Ron and the switching speed is faster compared to the conventional Si power devices, it is expected to improve power conversion efficiency and contribute to system miniaturization [30]. Today enhancement mode GaN devices are designed into hundreds of applications including DC-DC power converters for servers and notebook computers, envelope tracking systems for cell phone base stations, motor drives for robots, drones and factory automation, vehicle headlamps, class D audio amplifiers, wireless power systems, and satellite power distribution systems [49].

Chapter 4

4. Methodology

4.1 Components and Software Used

The designed class D amplifier circuit consisted of a PWM generator block, a power output stage and a filter stage using the simulation software LTspice as shown in the block diagram in Figure *26*.

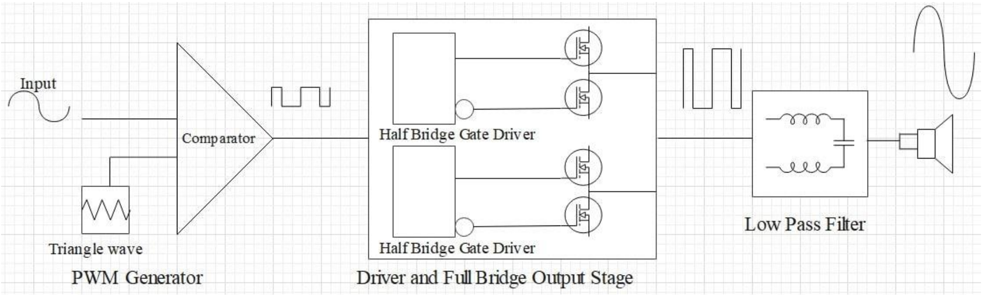


Figure 26: Block diagram of a basic Class D amplifier

In order to compare the performance of Gallium Nitride based class D amplifiers with their Silicon counterparts, the design, the power devices (i.e., the GaN and Si transistors) and the topology of the class D amplifier had to be selected. First the power devices were selected based on their applicability in class D design. For the GaN, EPC's EPC2021 enhancement mode GaN power transistor was selected. It was chosen due to its low on-resistance as well as its particular design by the manufacturer for class D application [50]. The Silicon power device selected was an Infineon OptiMOS$^{(TM)}$3 Power-Transistor with a similar voltage rating to the GaN device but with a slightly higher on-resistance, hence a higher FOM. Their specifications are outlined in Table 5.

	GaN	Silicon
Manufacturer	EPC	Infineon
Part Number	EPC2021	IPA100N08N3
Voltage Rating	80V	80V
Current Rating	90A @ 25	40A @ 25
On-Resistance (R_{on})	2.2mΩ @ V_{GS} = 5V, I_D = 29A	10mΩ @ V_{GS} = 10V, I_D = 40A
Gate Charge (Q_g)	15nC @ V_{GS} = 5V, I_D = 29A	26nC @ V_{GS} = 0 to 10V, I_D = 40A
Threshold Voltage (V_{th})	1.2V @ V_{DS} = V_{GS}, I_D = 13mA	2.8V @ V_{DS} = V_{GS}, I_D = 46µA

Table 5: Comparison Between GaN and Silicon Transistors From [50] And [51]

Next, the topology of the class D amplifier was selected based on the selected power devices. Therefore, based on the analysis done in the previous chapters (Chapter 2 – Class D amplifier design), a pulse width modulated full bridge (Bridge Tied Load – BTL) Class D amplifier circuit was selected.

For the PWM generator a triangle wave of 200kHz was initially used to envelope the input sine wave that had a frequency of 20kHz to model a high frequency audio signal (audio spectrum is 20Hz – 20kHz). The triangle wave and the sine input wave were fed into a comparator (LT1394) to generate the PWM signal. The comparator was supposed to output a positive pulse of 5V when the sine wave becomes greater than the triangular wave as shown in the Figure *27*.

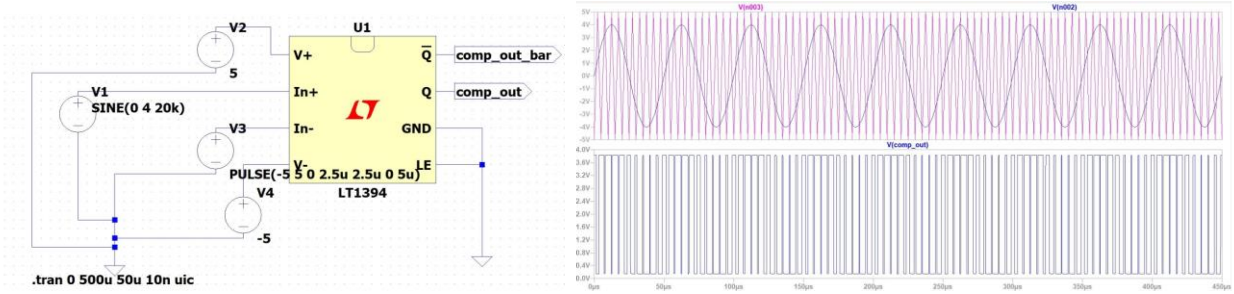


Figure 27: PWM generation using a triangular wave and LT1394 comparator

The major shortcoming of this approach was that the output of the comparator was slightly below 4V for the on state and slightly above 0V for the off state. This was not enough as an input for the gate driver for the next stage, and it needed a behavioral voltage source to convert it to such. Therefore, a design that incorporated feedback in order to add an error amplifier stage was proposed. This was done in order to make the circuit more resilient and minimize error. The PWM signal generated from a circuit obtained from the internet, which included an error amplifier, is shown in Figure *28*.

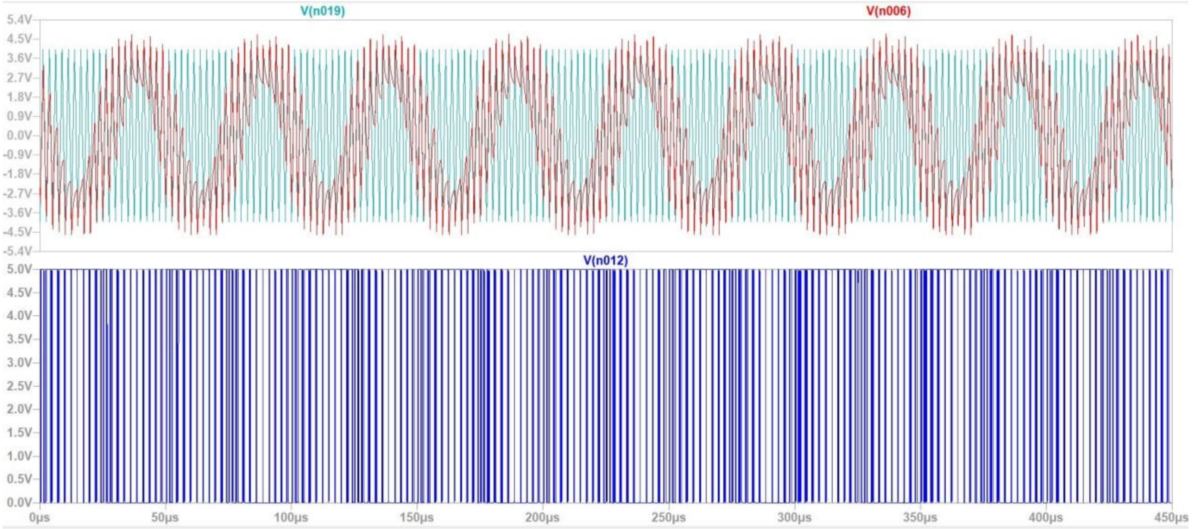


Figure 28: PWM generation with feedback error corrector network

The full bridge network of the final design didn’t have much use for the feedback network as it could eliminate noise and source interference without the aid of a feedback network. Upon further analysis, the feedback network for a full bridge design didn’t have much improvement on the efficiency of the amplifier but only strained the software for the simulation, and hence the processing computer as well. Therefore, in the final design, the feedback was removed and a better comparator was used that could directly connect to the gate drivers.

The comparator was first changed to LT1713 but due to its speed it was again changed to the LT1711, an ultrafast 4.5ns, Low Power dual rail-to-rail comparator [52]. It was fast enough for the design and generated 5V Dual complementary PWM signal, which was what was needed by the next stage of the design. Next to the comparator, a gate driver was needed to drive the corresponding transistors (i.e., GaN FET or MOSFET) in the power stage. Initially a common gate driver, that could drive both GaN FETs and MOSFETs, the LMG1210, was considered. But the lack of proper models on the internet as well as design circuits, prevented its use in the final design. Hence, separate drivers were necessary.

For the GaN the commonly used LM5113 from Texas instruments was initially considered, but was finally changed to the LMG1205 upon the recommendation of TI themselves (the LM5113 is not recommended for new designs). Both are 100V half bridge gate drivers for GAN FETs. Then, for the Si power device the UCC27211 120V half bridge gate driver from Texas instruments was used. Both of these gate driver’s models were autogenerated, as shown in the figure below, since LTspice does not have their models in its library and a symbol for the model was also not available from online resources.

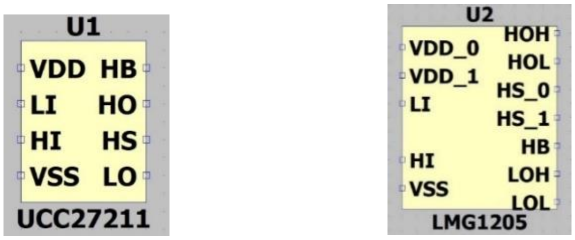


Figure 29: power stages gate driver model symbols

Since the design is full bridge, two of the gate drivers and four of the power devices were used in their corresponding designs for the GaN and Si class D amplifiers, as can be shown in the appendix. Next, after the gate drivers and the power devices, the output was connected to a low pass filter to eliminate the high switching frequency of the pulse width modulator.

The filter stage is a hybrid of a second order Butterworth LC filter with a Zobel network. The second order Butterworth filter is used to block the high frequency signal in the output of the amplifier. A Zobel network is recommended in every Class-D amplifier application to damp the filter resonance that occurs due to the inductive behavior of the speaker voice coil [53].

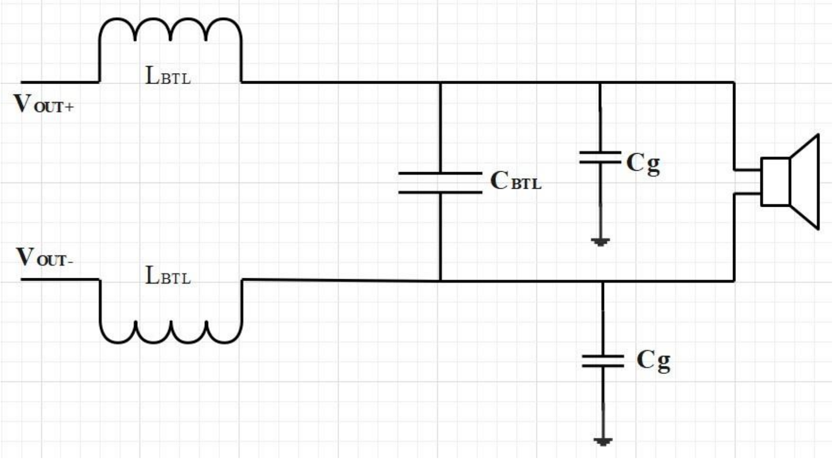


Figure 30: Low-Pass Filter for BTL Application

The first step in the design of the filter was to determine the values for the LC filter using either the formula mentioned below or using different precalculated table sets that give the value of L and C based on the cutoff frequency.

$$C_{BTL} = \frac{1}{2\sqrt{2} \cdot \pi \cdot R_L \cdot f_C}$$

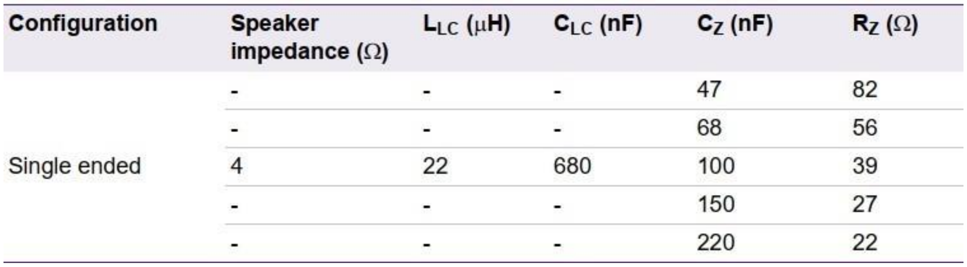
$$L_{BTL} = \frac{\sqrt{2} \cdot R_L}{4 \cdot \pi \cdot f_C}$$

The capacitors labeled C_g in Figure *30* serve as high frequency bypass capacitors, and are empirically chosen to be approximately 10% of 2 * C_L, and their small value has a negligible impact on the filter cutoff frequency [23]. But the values from the table given below will do good for the desired filtering. At a cut-off frequency of 40kHz, 22µH bridge tied load inductor value and 330nF bridge tied load capacitor value is taken and for the Capacitors connected directly to ground C_g of 68 nF is taken.

8 Ω					
f_o (kHz)	PEAKING AT 20 kHz (dB)	L_{BTL} (µH)	C_{BTL} (µF)	C_g (µF)	$\text{Gain}_{\text{Diff\_250kHz}}$ (dB)
28	–1.2	33	0.47	0.1	–38
41	–0.28	22	0.33	0.068	–31
34	2	15	0.68	0.1	–35

Table 6: Recommended Butterworth filter component values for R_{BTL} = 8 Ω measured [54]

A Zobel network is an Impedance Equalization Circuit, which can be used to counteract the rising impedance of a voice coil caused by inductive reactance of a speaker. The cause of this impedance rise is due to the speaker's voice coil inductance. A Zobel network is required for audio amplifiers applications to get the desired output. There is a formula to find the damping resistor and capacitor values, but in most cases, similar to the current design, they were found to be erroneous. Therefore, the values are taken from a table depending on the bridge tied load inductance and the load resistance.



Configuration	Speaker impedance (Ω)	L_{LC} (μH)	C_{LC} (nF)	C_Z (nF)	R_Z (Ω)
Single ended	-	-	-	47	82
	-	-	-	68	56
	4	22	680	100	39
	-	-	-	150	27
	-	-	-	220	22

Table 7: Zobel damping resistors for different capacitor values [53]

In Table 7, the values of the Zobel resistance and capacitances are suitable for single ended as well as BTL, and for a speaker load of 4Ω, 6 Ω and 8 Ω. The final low pass 2nd order Butterworth LC filter combined with the Zobel network which is suitable for attenuating the switching noise as much as possible while having minimal effect on the desired output is designed as shown in Figure 31.

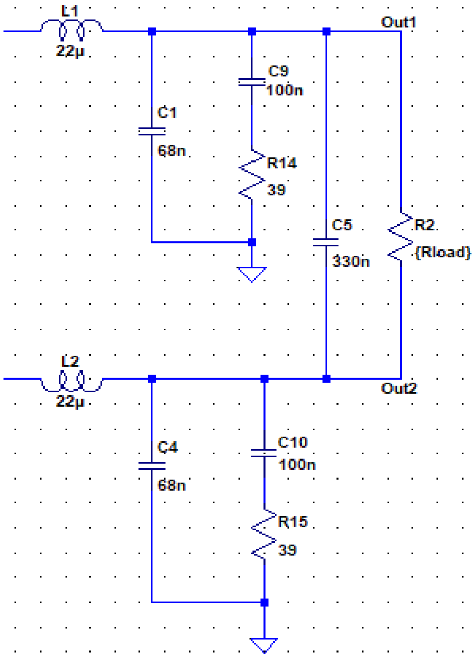


Figure 31: The final filter used in the current design

4.2 Approach

The methodology used in this thesis to compare the performance of GaN based Class D amplifiers with conventional Si based amplifiers was by first understanding the design of Class D amplifiers, then understanding GaN material and finally, by designing the circuit in order to make the comparison. The simulation was performed using the LTspice software in an 11th Gen Core i7 Dell Laptop with 16GB RAM and 500GB SSD.

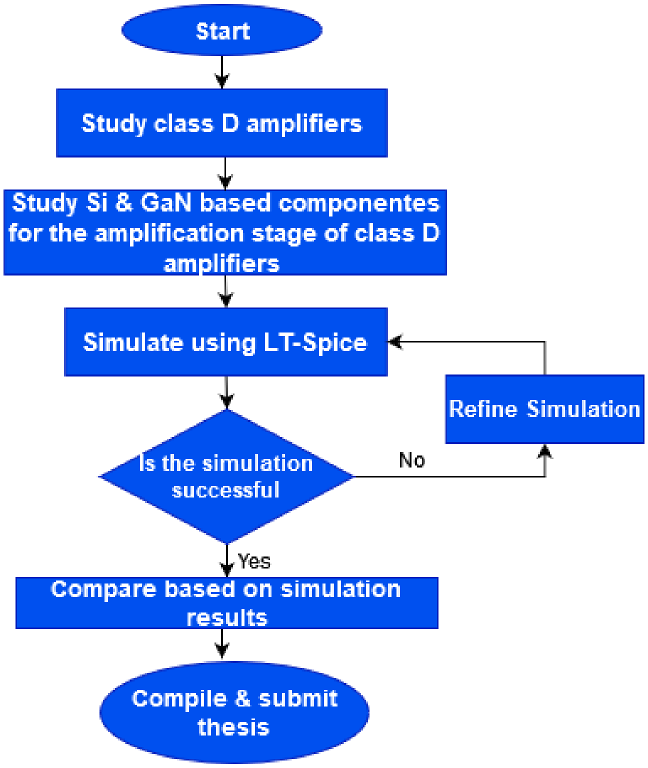


Figure 32: Methodology used for the thesis

Chapter 5

5. Results and Discussion

5.1 Summary of Simulation Results

Now the output of the different stages of the amplifiers can be seen in the following figures. The PWM signal generated from the input sine wave and the triangular wave using the LT1711 comparator can be seen in Figure *33* below.

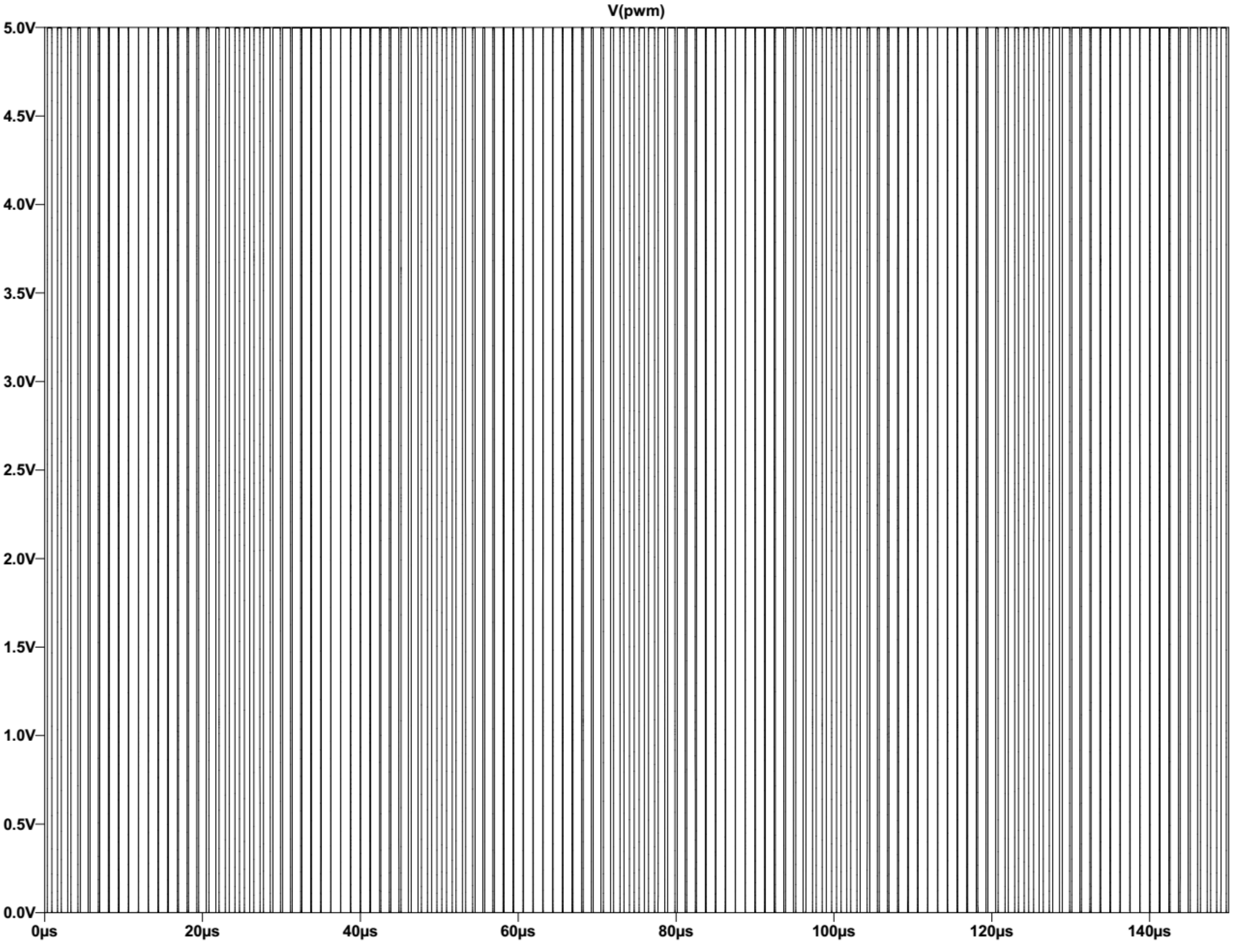


Figure 33: PWM signal generated from the comparator

The PWM signal generated from the comparator enters the power devices via the gate drivers. The PWM signal is then amplified as it can be seen in the figures below. There is a slight difference between the GaN output, Figure *34*, and the MOSFET output, Figure *35*.

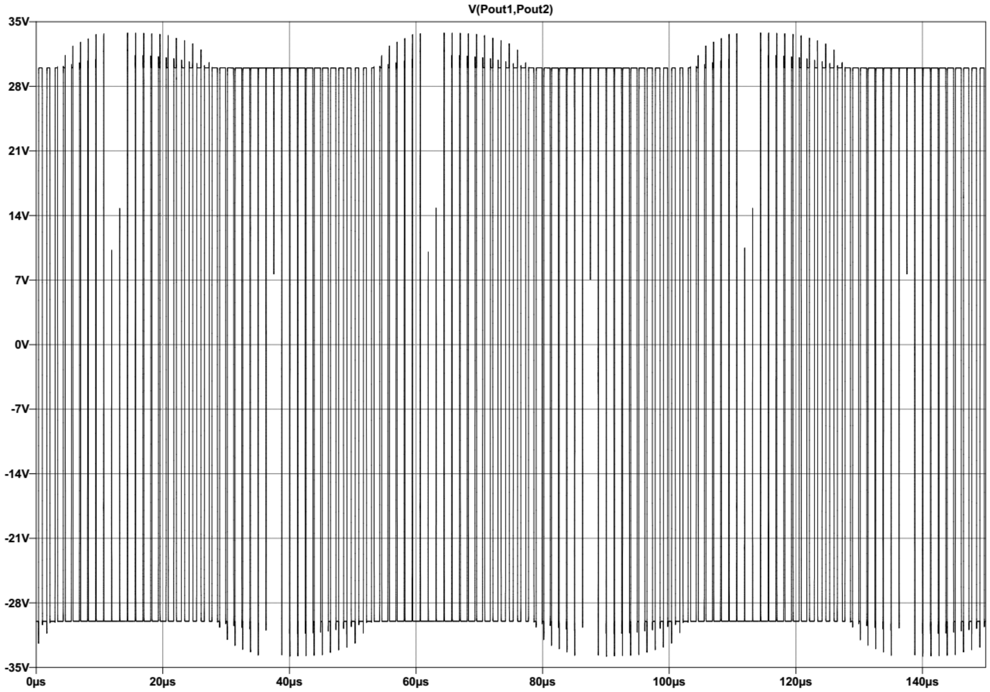


Figure 34: power stage differential output before the filter of EPC 2021

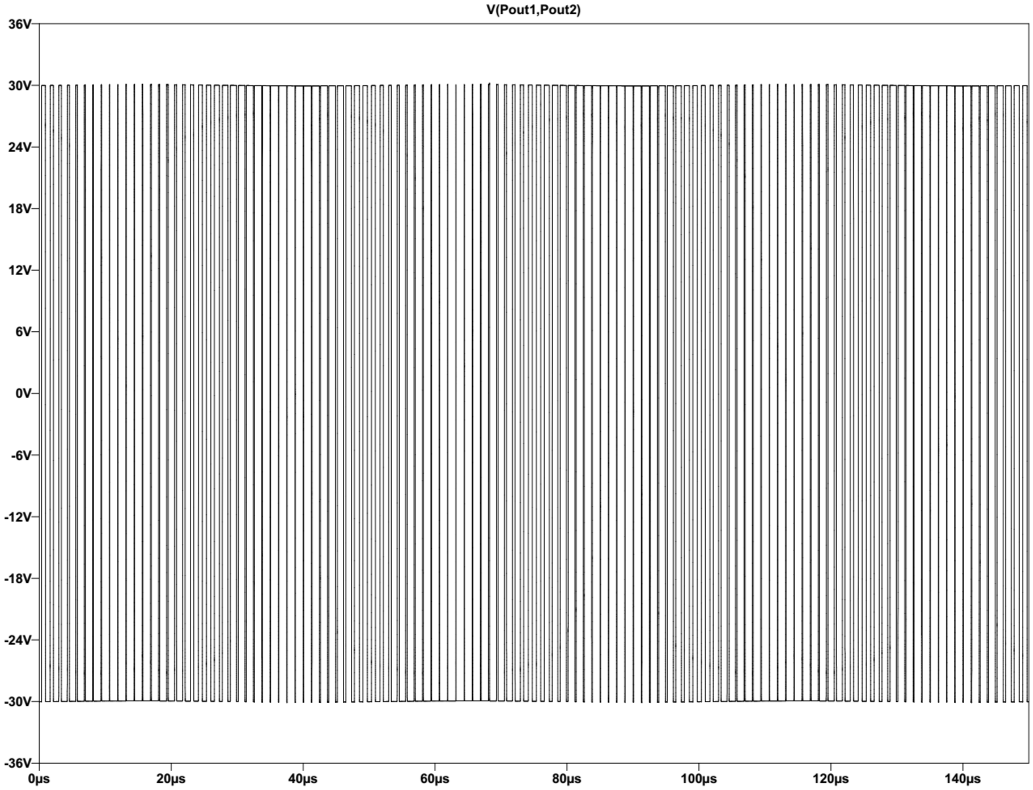


Figure 35: power stage differential output before the filter of IPA100N08N3

Then, the output of the power devices, which is an amplified PWM signal, is fed to the hybrid filter. As compared to the input sinusoidal AC signal, the output becomes an amplified sinusoid with an approximate gain of about 30 (i.e., 29.9 for the GaN and 29.7 for the Si). The final output after the filtering stage compared to the input is shown in the figures below, where the output and the input waveforms are as labeled.

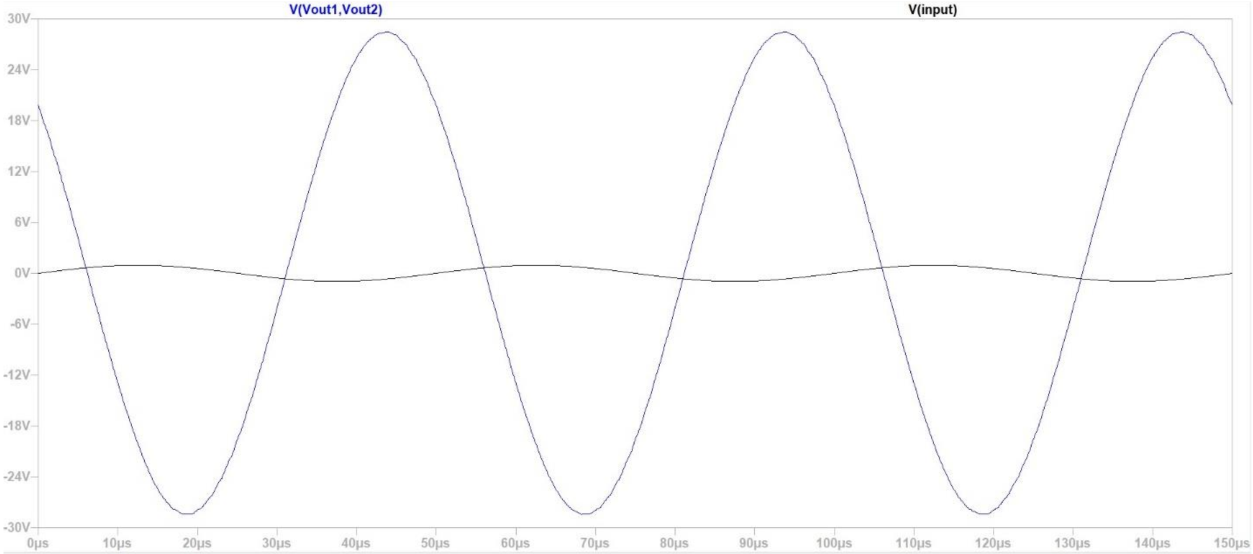


Figure 36: EPC 2021 BTL output after the filter stage vs input

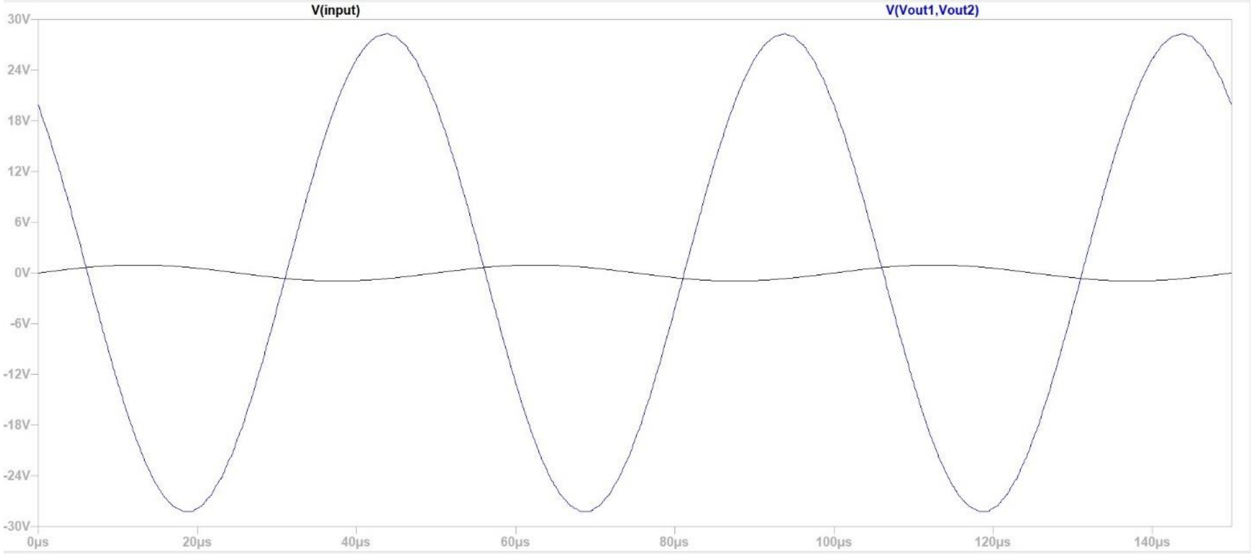


Figure 37: IPA100N08N3 BTL output after the filter stage vs input

The slight difference in the gain of GaN over Si can be seen in Figure *38*. It shows a juxtaposed waveform of the filtered output of the GaN Class D amplifier and the Si Class D amplifier. Where the blue colored waveform shows the GaN and the red colored waveform shows the Si output respectively.

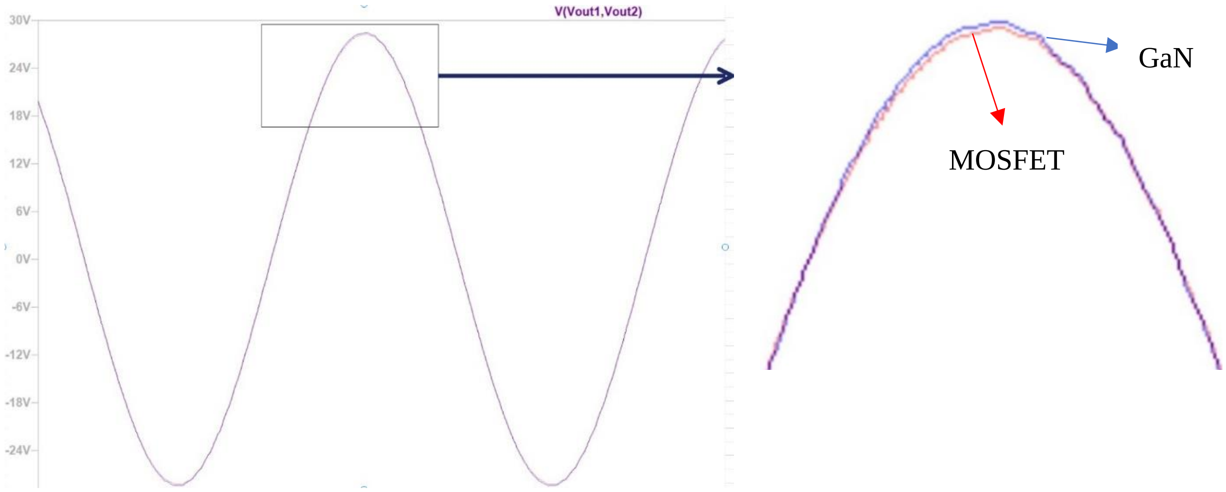


Figure 38: Comparison of the gain of GaN and Si Class D amplifiers

After designing and simulating the desired circuit the efficiency was measured using several methods. Since this is an amplifier, the input power is the DC power supply and the output power is the AC power measured at the load.

$$P_{in} = i_{in} \cdot V_{dc_{in}}$$

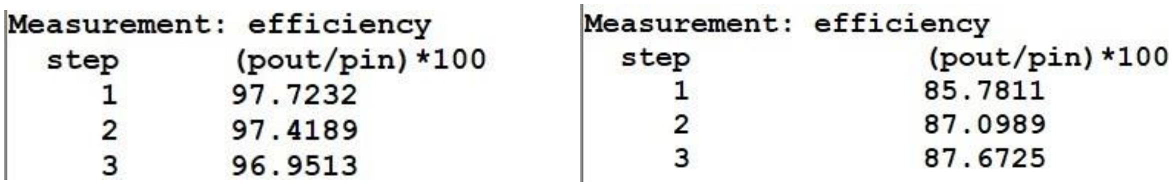
$$P_{out} = i_{load} \cdot V_{out}$$

$$\eta = \frac{P_{out}}{P_{in}} * 100\%$$

There were several methods used to calculate the efficiency of the class D amplifier. In the first method, the efficiency was calculated manually, i.e., measuring the input and output power and calculating the efficiency for both the EPC2021 and IPA100N08N3. In the second, the .measure command was used from LTspice to measure the input power, output power and efficiency at the same time.

The efficiency was measured at different speaker loads as well as different switching frequencies. This was done to show the resilience of GaN class D amplifiers compared to their Si counterparts for higher switching frequencies as well as for different speaker conditions (typical speaker loads of 4Ω, 6Ω and 8Ω were used).

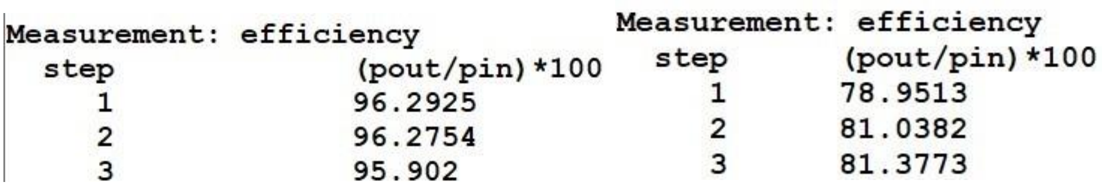
The following tables show this effect for different loads and different switching frequencies. The efficiencies were measured at the switching frequencies (the frequency of the PWM) of 100kHz, 200kHz, 400kHz and 800kHz for both the GaN device and the Si device. In LTspice the .step command was used for these measurements to find the efficiencies for the different frequencies and different speaker loads at the same time.



```
Measurement: efficiency
  step       (pout/pin)*100
     1       97.7232
     2       97.4189
     3       96.9513
```

```
Measurement: efficiency
  step            (pout/pin)*100
   1              85.7811
   2              87.0989
   3              87.6725
```

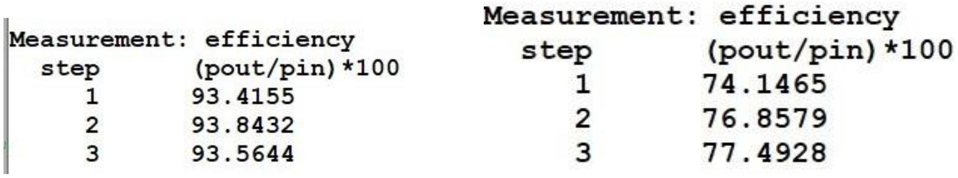
Table 8: efficiency for 4Ω, 6Ω and 8Ω loads at 100kHz for a) EPC2021 and b) IPA100N08N3



```
Measurement: efficiency
  step                 (pout/pin)*100
     1                 96.2925
     2                 96.2754
     3                 95.902
```

```
Measurement: efficiency
  step         (pout/pin)*100
     1         78.9513
     2         81.0382
     3         81.3773
```

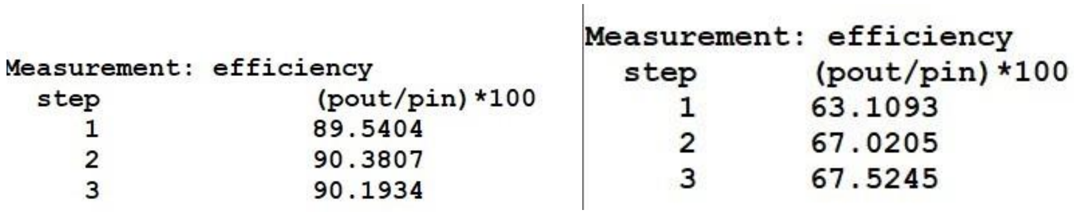
Table 9: efficiency for 4Ω, 6Ω and 8Ω loads at 200kHz for a) EPC2021 and b) IPA100N08N3



```
Measurement: efficiency
  step       (pout/pin)*100
     1       93.4155
     2       93.8432
     3       93.5644
```

```
Measurement: efficiency
  step        (pout/pin)*100
     1        74.1465
     2        76.8579
     3        77.4928
```

Table 10: efficiency for 4Ω, 6Ω and 8Ω loads at 400kHz for a) EPC2021 and b) IPA100N08N3



```
Measurement: efficiency
  step                 (pout/pin)*100
     1                 89.5404
     2                 90.3807
     3                 90.1934
```

```
Measurement: efficiency
  step        (pout/pin)*100
     1        63.1093
     2        67.0205
     3        67.5245
```

Table 11: efficiency for 4Ω, 6Ω and 8Ω loads at 800kHz for a) EPC2021 and b) IPA100N08N3

These results can be simply tabulated as below:

Frequency	4 Ω		6 Ω		8 Ω	
	EPC2021	IPA100N08N3	EPC2021	IPA100N08N3	EPC2021	IPA100N08N3
100KHz	97.7232	85.7811	97.4189	87.0989	96.9513	87.6725
200KHz	96.2925	78.9513	96.2754	81.0382	95.902	81.3773
400KHz	93.4155	74.1465	93.8432	76.8579	93.5644	77.4928
800KHz	89.5404	63.1093	90.3807	67.0205	90.1934	67.5245

Table 12: Comparison of EPC2021 and IPA100N08N3

5.2 Comparison with past related works

The literature reviewed in chapter 3 can be compared arbitrarily with the simulation in this thesis. Only the efficiency can be used for this comparison based on the claimed efficiencies of each paper.

Author	Year	Material	Topology	Peak Efficiency
Joshua Chung et al. [39]	2016	GaN	Full Bridge	82.3%
Joshua Chung et al. [39]	2016	Si	Full Bridge	67%
Allyfrahy et al. [40]	2020	GaN	Full Bridge	97.2%
Jordan Sangid et al. [41]	2018	GaN	Half Bridge	93.2%
Jordan Sangid et al. [41]	2018	Si (TI)	Half Bridge	90.7%
Jordan Sangid et al. [41]	2018	Si (Infineon)	Half Bridge	90.4%
** This Work	2022	GaN	Full Bridge	97.7%
** This Work	2022	Si	Full Bridge	87.6%

Table 13: Comparison of this work with past related works

Chapter 6

6. Conclusion and Future work

6.1 Conclusion

Gallium Nitride is gaining market share in the areas of high power, high frequency power conversion applications from Silicon. This is mainly due to its very low on-resistance and gate charge, leading to a very small figure of Merit as compared to Silicon. This enables it to perform well in high voltage, high speed (high frequency) applications, such as Class D amplifiers.

The results of this thesis show that the efficiency of the GaN circuit is categorically greater than that of the Si circuits. This was also emphasized when the switching frequency was increased, reaching to a region where GaN is well adaptable. Even though, GaN can theoretically achieve efficiencies of about 100%, this study proved that it could get close enough (97.7%). This is a great improvement from the Silicon of yesteryear, which peaked at a mere 87.6%.

The theoretical assumption that GaN is better at high frequencies than Si was also proved in this work since the Class D efficiency was measured at high as well as low frequencies. The gap between the efficiencies of GaN and Si in Class D more than doubled when the switching frequency was increased from 100kHz to about 800kHz. Even at a high frequency of 800kHz the GaN circuit achieved about 90% efficiency, which is much higher than other classes of amplifiers (A, B, AB…).

When considering the effect of the output speaker load on the efficiency of the system, there was very little variation to be observed. This might be due to the fact that the speaker was modeled using a Zobel filter for the hybrid filter stage. For the GaN the 6Ω load seemed to have better results, whereas for the Si, the efficiency seemed to increase with increasing speaker load.

When comparing the output of this work to those in the literature, the GaN had better efficiency while the Si didn't fare any better. This could be for various reasons, for instance the topology, the presence of feedback, the modulation technique used (i.e., PWM, PDM…), the type of filter used and much more. In comparing the Si Class D circuits, the past related works reviewed had, in addition to using the full bridge topology, better modulation techniques and in some cases even implemented feedback, with the aim of achieving better efficiencies with Si.

Overall, this work can be used to conclude that the performance of GaN Class D amplifiers is greater than that of Silicon Class D amplifiers. This is even more exaggerated for higher frequencies, as the simulations in this thesis has proven.

6.2 Limitations

This current study was performed under a lot of constraints, which limited its scope from the beginning of the research. The first constraint was funds; since this thesis didn’t have any funding the scope was only limited to a software performance comparison (i.e., simulation only). Therefore, a free Spice simulation software had to be selected (LTspice) and also the components selected for simulation had to be freely available online with their libraries.

Despite using LTspice, the computing capacity of the LTspice solver and the laptop itself was also limited. Therefore, higher frequency comparisons couldn’t be made (the maximum was 800kHz). Some circuit arrangements (feedback arrangements, three level PWM generators, error amplifier circuits…) were also observed to have a lot of strain on the computer. Therefore, a full bridge topology with a PWM generator network limited to 800kHz was used.

Since this is a relatively new field of study, there was also a limitation of research material that shows the application of GaN in Class D amplifiers. There wasn’t much reported data on the comparison of GaN and Si in Class D amplifier networks to compare with this work. Hence, it was an arduous task trying to design and piece together the different blocks of a Class D amplifier, which is a great addition to the pool of studies in the scientific community.

6.3 Future work

The work done under the circumstances mentioned in the limitations section is very promising, but much more work needs to be done to reach an absolute conclusion on the performance of GaN class D amplifiers. A PCB design and a physical implementation of the designed networks could also be implemented to physically compare GaN and Si Class D amplifiers. Without the limitation of the processing power, a better circuit could also be designed using feedback and analysis for higher frequency comparisons.

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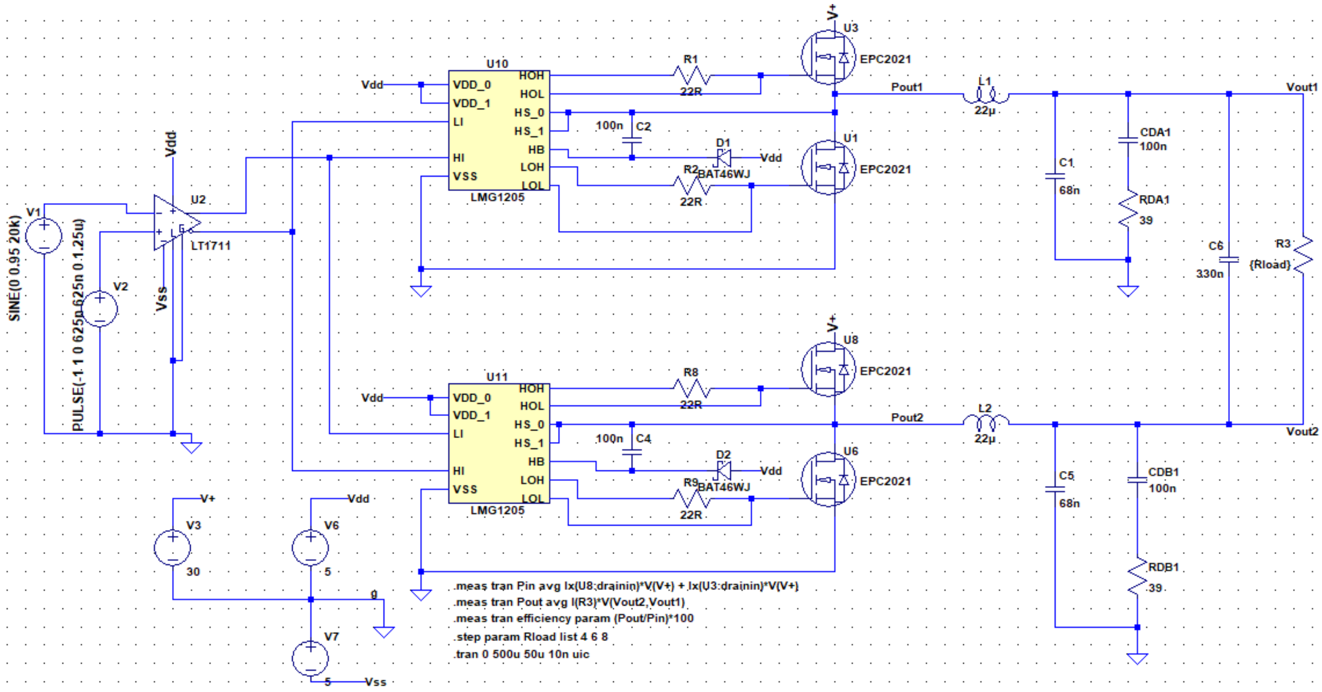
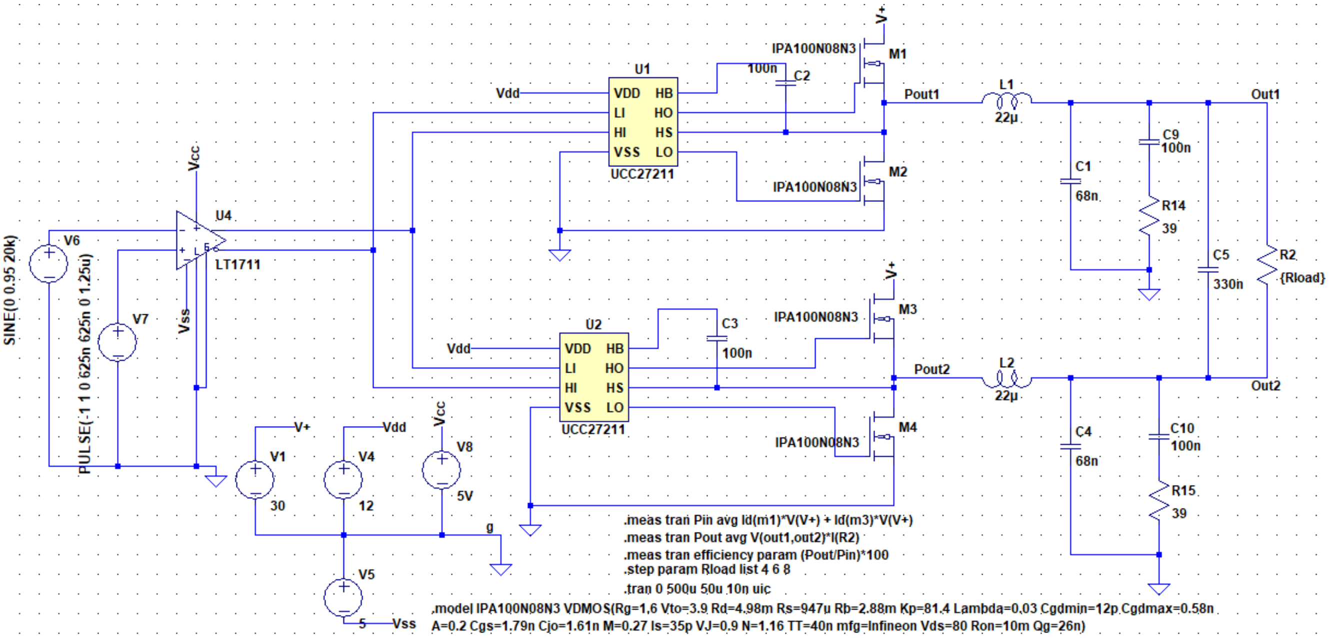
Appendix – Designed Circuit

The designed circuit for this paper, performance analysis of GaN based Class D Amplifiers with their Silicon counterparts, is shown in the following figures. Two separate circuits were designed, one incorporating GaN and the other Si Power MOSFETS. The only difference in the two circuits is the power amplification stage.



```
.meas tran Pin avg Ix(U8:drainin)*V(V+) + Ix(U3:drainin)*V(V+)
.meas tran Pout avg I(R3)*V(Vout2,Vout1)
.meas tran efficiency param (Pout/Pin)*100
.step param Rload list 4 6 8
.tran 0 500u 50u 10n uic
```

Figure 39: EPC2021 based full bridge class d amplifier



```
.meas tran Pin avg Id(m1)*V(V+) + Id(m3)*V(V+)
.meas tran Pout avg V(out1,out2)*I(R2)
.meas tran efficiency param (Pout/Pin)*100
.step param Rload list 4 6 8
.tran 0 500u 50u 10n uic
.model IPA100N08N3 VDMOS(Rg=1.6 Vto=3.9 Rd=4.98m Rs=947u Rb=2.88m Kp=81.4 Lambda=0.03 Cgdmin=12p Cgdmax=0.58n
A=0.2 Cgs=1.79n Cjo=1.61n M=0.27 Is=35p VJ=0.9 N=1.16 TT=40n mfg=Infineon Vds=80 Ron=10m Qg=26n)
```

Figure 40: IPA100N08N3 based class d amplifier