EXPERIMENTAL STUDY OF CHARGE DISTRIBUTION IN METAL-OXIDE-SEMICONDUCTOR(MOS) STRUCTURE

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DEDICATION

This work is totally dedicated to my father Ato *G/MARIAM KALLO* for educating his children and to my sister *TADELECH G/MARIAM*.

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I am greatly indepted to my advisor and Instructor *Dr. P. Hrushka* for his encouragement and continuous help through out the work. His unreserved guidance on computer operation is also acknowledged.

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CONTENTS

ABSTRACT

Theoretical review of MOS structure is done. Ideal MOS structure was considered first. After it various effects such as work function difference, oxide charges etc, that deviate the ideal MOS property are discussed.

Three electrical measurement techniques are discussed. The capacitance measurement technique at room temperature is used for the experiment. Description of the experimental set up is given and properties of individual instruments including the computer are discussed.

Measurement is done on three samples. Insulating layer on samples 6f and 8a is SiO_2, on sample 12c the layer is Indium - Thin - Oxide. From high frequency c-v measurement surface charge density and surface state density is determined and their value is compared with data previously published. From combined high and low frequency capacitance measurement values of energy distribution of density of states and doping profile are obtained. On all samples the effect of illumination was observed in depletion and inversion layers. Distinct deviation from theoretically predicted high frequency c-v curves was observed on sample 12c. Two peak appears between accumulation and depletion layer. These peaks are at bias value - 0.95v and + 0.12v. The bias value are independent

of frequency. The capacitance values of the peaks decrease with frequency.

INTRODUCTION

Metal-Oxide-Semiconductor (MOS) structure play dominant role in many solid state devises and integrated circuits (IC). The most important examples are MOS capacitors(MOSC) and MOS field effect transistors (MOSFET). Fabrication of stable and high performance small volume IC for purpose of Very Large Scale Integration (VLSI) motivated thorough study of MOS structures. The present interest for further IC size reduction requires further investigation of MOS structures.

Electric charges in MOS structure are distributed in a very complicated way. Their distribution depends on the potential function in the structure, on impurity levels and their concentration, on electron and hole traps, both shallow and deep. It strongly depends on oxide thickness. In applications like semiconductor devises production it is crucial to have sufficient knowledge about the traps and impurity levels. Several methods have been developed for the charge distribution study. The most important of these are: I-V, C-V, Noise measurements and Deep Level Transient Spectroscopy (DLTS).

At the oxide (eg. SiO_2) - semiconductor (eg. Si) interface of MOS structures, the change in

the periodicity of the lattice creates trap levels. These interface traps interact with free charge carriers in the semiconductor. The traps are filled with majority carriers when the interface state is biased in to accumulation condition. When the interface is biased in to depletion or inversion conditions, the charge in the interface region is changed. It leads to unstability of MOS devices. Despite many years of research and effort of many scientists and engineers interface state in MOS structure is still unknown. Thus, research in the Physics (also Chemistry) of interface states or traps continues to be needed. Measurement techniques has been developed for the study of interface state. Some of these are : Quasistatic Capacitance Voltage (C-V) technique, Conductance technique, DLTS, Electron spin resonance (ESR). But we considered the first three techniques in our work.

The objective of the thesis is to introduce the individual methods to our Physics department laboratory, to write necessary computer programs for instrument control and compare the result obtained with the theoretical result.

The first chapter deals with ideal MOS structure. It describes charge distribution near

the surface, high and low frequency capacitance of the interface. The second chapter gives brief discussion of effects like interface trapped and oxide charges, Work-Function difference and some others. It deals with carrier transport in insulating films (oxides) too. The third chapter gives brief description of measurement techniques. The fourth chapter includes apparatus and their arrangement, techniques used in our work and experimental result and discussion.

CHAPTER 1

Ideal Metal - Oxide - Semiconductor (MOS) structure.

Introduction

The Metal-insulator-Semiconductor (MIS) structure is very useful in experimental study of the semiconductor surface. Since the reliability and stability of semiconductor devices are related to their surface conditions, an understanding of the surface and interface physics with the help of MIS structure is of great importance.

The MIS structure was first proposed as a voltage-variable capacitor in 1959 by Moll | 1 | and by Pfann and Garrett | 1|. Its characterstics were then analyzed by Frenkel and Linder | 1 |. The MIS structure was first employed in the study of thermally oxidized silicon surface by Terman and by Lehovec and Slobodsky | 1 |. If the insulator is an oxide, then the structure is refered to as Metal-Oxide-Semiconductor (MOS) structure.

1.1 Ideal MOS structure

The MOS structure is shown in Fig. 1, where d is the thickness of the oxide and v is the applied voltage on the metal plate. Throughout this paper we use the convention that the voltage v is positive when the metal plate is positively biased with respect to the ohmic contact, and v is negative when the metal plate is negatively biased with respect to the ohmic contact.

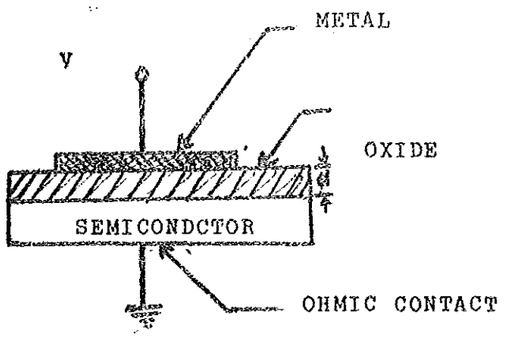


Fig. 1 MOS structure

The energy-band diagram of an ideal MOS structure for v = 0 is shown in Fig. 2, for p-type semiconductor. An ideal MOS is defined as follows[1] . (1) At zero applied bias, energy difference between the metal work function ϕ_m and the semiconductor work function ϕ_s, ϕ_{ms} is zero.

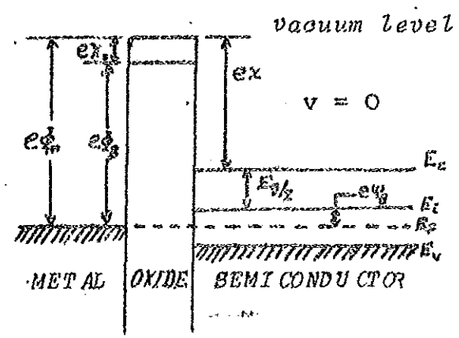


Fig.2 Energy band diagram of ideal MOS structure at v = 0 for p-type semiconductor

The following relation applies:

$$\phi_{ms} = \phi_m - (\chi + E_g/2e + \psi_B) = 0 \quad \text{for P-type} \tag{1.1.1}$$

Similarly

$$\phi_{ms} = \phi_m - (\chi + E_g/2e - \psi_B) = 0 \quad \text{for n-type} \tag{1.1.2}$$

Where ϕ_m is the metal work function, χ the semiconductor electron affinity, χ_o the oxide electron affinity, Eg. the bandgap, ϕ_B the potential barrier between the metal and the oxide, and ψ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i. In other words, the band is flat (flat-band condition) when there is no applied voltage.

(2) The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those with the equal but opposite sign on the metal surface adjacent to the insulator. (3) There is no carrier transport through the insulator under dc biasing conditions, since the resistivity of the insulator is assumed to be infinite.

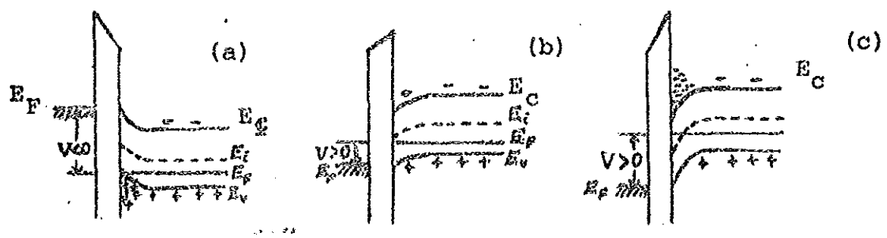
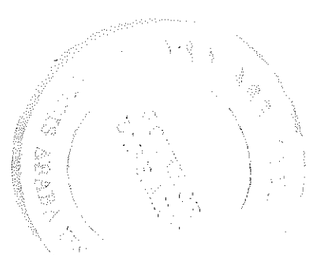


Fig. 3.. Energy - band diagrams of ideal MOS structure when v ≠ 0 for P-type semiconductor, for the following cases:

(a) accumulation; (b) depletion; (c) inversion

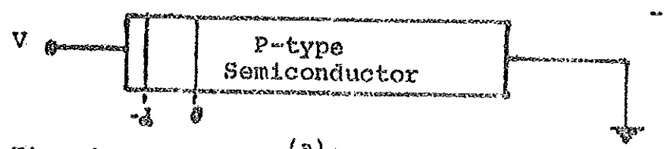
When an ideal MOS structure is biased with positive or negative voltage, basically three cases may exist at the p-type semiconductor. When a negative voltage (v<0) is applied to the metal plate, the top of the valence band bends upward and is closer to the Fermi level(Fig.3a) For ideal MOS structure, no current flows in the structure, so the Fermi level remains constant in the semiconductor. Since the carrier density depends exponentially on the energy difference $(E_F - E_V)$, $P = N_V \exp\left(\frac{-E_F - E_V}{KT}\right)$, this band bending causes on increase of majority carrier conductivity near the semiconductor surface. This is the "accumulation" case. When a small positive voltage ($v > 0$) is applied, the bands bend downward, and the concentration of majority carriers decrease (Fig. 3b). This is the " depletion " case. When a large positive voltage is applied, the bands bend even more downward so that the intrinsic level E_i at the surface crosses over the Fermi level E_F (fig. 3C). At this point the number of electrons (minority carriers) at the surface is large than that of the holes, the type of conductivity of the surface is thus inverted (to n-type). This is the "inversion" case. Similar results can be obtained for the n-type semiconductor. The polarity of the voltage, however, should be changed for the n-type semiconductor.



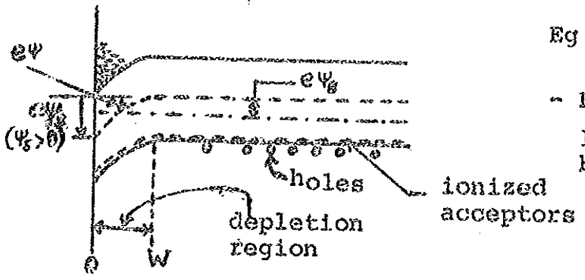
1.2 Surface Space-Charge Region

Relation between surface potential, space charge, and electric field will be discussed. The relation will be used later to discuss c-v characterstics of ideal MOS structure.

Consider a P-type semiconductor without surface states as shown in Fig. 4.

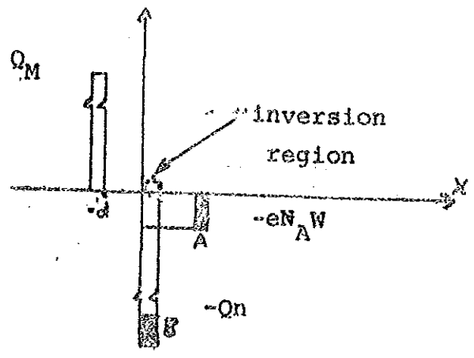


(a) - MOS structure



(b) $E_g = E_c - E_v$

- Energy band at large positive bias.

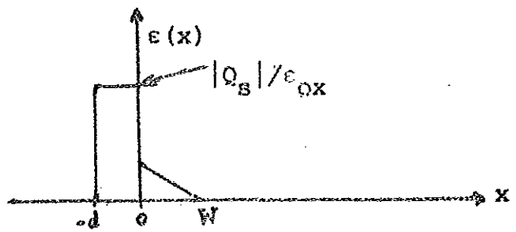


(c) - Idealized charge distributions with in the semiconductor for large positive bias.

eN_AW and Q_n are density of ionized acceptors and electron per unit area in inversion region respectively.

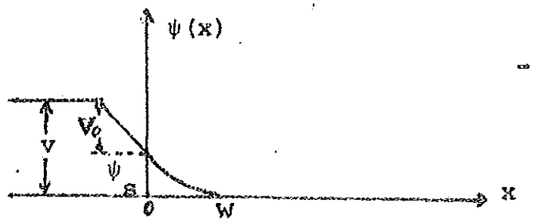
Fig. 4

(d)



-Electric field for charge distribution given above.

(e)



- Potential distribution ($V=V_o+\psi_s$, applied voltage)

In Fig. 4b the potential ψ is defined as zero in the bulk of semiconductor and is measured with respect to the intrinsic Fermi level E_i. At the semiconductor surface, $\psi = \psi_s$, and ψ_s is called the surface potential. The electron and hole concentration as a function of ψ are given by the relation:

$$\eta_p = \eta_{po} \exp(\beta\psi)$$
$$P_p = P_{po} \exp(-\beta\psi) \qquad (1.2.1)$$

where η_{po} and P_{po} are the equilibrium densities of electrons and holes respectively, in the bulk of the semiconductor, and $\beta = e/KT$. At the surface the densities are

$$\eta_s = \eta_{po} \exp(\beta\psi_s) \qquad (1.2.2)$$
$$P_s = P_{po} \exp(-\beta\psi_s)$$

From our discussions in section 1.1 and with the help of Eq. 1.2.2. the following regions of surface potentials are distinguished [1]:

$\psi_s < 0$ accumulation of holes (bands bend upward)

$\psi_s = 0$ flat-band condition

$\psi_\beta > \psi > 0$ depletion of holes (bands bend downward)

$\psi_s = \psi_\beta$ midgap with $\eta_s = P_s = \eta_i$ (intrinsic concentration)

$\psi_s > \psi_\beta$ inversion (electron enhancement, bands bend downward).

Under inversion condition, electrons will be attracted to the surface so that the negative charge in the semiconductor will consist partly of the electrons in a narrow inversion region near the surface and partly of the exposed acceptor ions in the depletion region (Fig.4c). At large biases the charge of the electrons dominates,

in contrast with a revers biased p-n junction where accumulation of minority carriers is impossible and all of the charge must consist of the acceptor ions with in the depletion region. This result is very important [2]: In a reverse biased p-n junction the width of the depletion region will keep increasing with increasing bias, whereas in an MOS structure it will not.

The presence of electron inversion region will determine the size of the depletion region under the given dc bias. The depletion width can be defined from charge neutrality requirement, i.e.,

$$Q_M = Q_n + eN_A W = Q_s \qquad (1.2.3)$$

Where Q_H is charge perunit area on the metal, Q_n is electron per unit area in the inversion region, $eN_A W$ is the ionized acceptors per unit area in the space charge region with space charge width w, and Q_s is the total charge per unit area in the semiconductor.

To arrive at the result of interest, consider one dimensional poisson's equation,

$$\frac{d^2\psi}{dx^2} = \frac{-\rho(x)}{\varepsilon_s} \qquad (1.2.4)$$

Where $\rho(x)$ is total space-charge density in semiconductor, ψ is pptential due to charge distribution under consideration, and ε_s is permitivity of semiconductor. Total space-charge density is given by

$$\rho(x) = e\ (N_D^+ - N_A^- + P_p - \eta_p) \qquad (1.2.5)$$

Where N_D^+ and N_A^- are the densities of the ionized donors and acceptors, respectively. The condition of charge neutrality must exist in the bulk, that is, far from the surface where $\psi(x) = (\infty) = 0$ and $\rho(x) = \rho(\infty) = 0$. Since impurity is fully ionized it follows

$$N_D = \eta_{po} \quad , \quad N_A = p_{po} \tag{1.2.6}$$

Using Eq. (1.2.1), (1.2.5); (1.2.6) and integrating Eq (1.2.4) yields electric field given by

$$\varepsilon = \pm \frac{\sqrt{2}KT}{eL_p} \left[(e^{-\beta\psi} + \beta\psi - 1) + \eta_{Po}/p_{po} \ (e^{\beta\psi - \beta\psi - 1})\right]^{\frac{1}{2}},$$

$$L_p = \sqrt{\frac{KT\varepsilon_s}{e^2 p_{po}}} \tag{1.2.7}$$

where L_p is called the extrinsic Debye length for holes. Introducing the function F[3]

$$F(\beta\psi, \frac{\eta_{po}}{p_{po}}) = \left[e^{-\beta\psi} + \beta\psi - 1 + \frac{\eta_{po}}{p_{po}}(e^{\beta\psi - \beta\psi - 1})\right]^{\frac{1}{2}} \geq 0$$

(1.2.8)

electric field becomes $\varepsilon = \pm \frac{\sqrt{2}KT}{eL_D} F(\beta\psi, \frac{\eta_{po}}{p_{po}})$ (1.2.9)

Electric field at the surface is

$$\varepsilon_s = \pm \frac{\sqrt{2}KT}{eL_D} F(\beta\psi_s, \frac{\eta_{po}}{p_{po}}) \tag{1.2.10}$$

Using Gauss's law the space-charge per unit area required to produce this field is

$$Q_s = -\varepsilon_s \mathcal{E}_s = \mp \frac{\sqrt{2KT\varepsilon_s}}{eL_D} F(\beta\psi_s , \frac{\eta_{po}}{p_{po}}) \qquad (1.2.11)$$

Computer program showing the dependence of Q_s on ψ_s is prepared. Name of the program is "Scd-Sp" (see appendix A). It shows the effect of temperature and doping density on space charge density and energy band. At temperature $T = 300^{o}k$ varying the concentration one can see that near and above $N_A = 5x10^{17}/cc$ the semiconductor is degenerate and depletion region increases. As the acceptor concentration decreases to a value $10^{10}/cc$ the semiconductor becomes intrinsic type, depletion region decreases, the band gap increases and below this value it changes to n-type semiconductor. The band varying with concentration with respect to the Fermi level is valence band. For concentration $N_A = 4x10^{15}/cc$ and for temperature near and below $215^{o}k$, the semiconductor becomes degenerate and depletion region increases. As the temperature increases the depletion region decreases and the semiconductor tends to have intrinsic behaviour. Both bands E_c and E_v shift relative to the Fermi level. Computer simulated graph is shown in Fig. 5. What one can see from the graph in relation to the relations derived above is the following. For negative ψ_s , Q_s is positive and corresponds to the accumulation region. The function F is dominated by the first term in Eq. 1.2.8, that is $Q_s \sim \exp(e|\psi_s|/2kT)$.

For $\psi_s = 0$, we have the flat-band condition and $Q_s = 0$. For $\psi_\beta > \psi_s > 0$, Q_s is negative and we have the depletion case. The function F is now dominated by the second term, that is, $Q_s \sim \sqrt{\psi_s}$. For $\psi_s >> \psi_\beta$ we have the inversion case with function F dominated by the fourth, that is, $Q_s \sim \exp(e\psi_s/2kT)$. Also the strong inversion begins at a surface potential,

$$\psi_s(\text{inv}) \simeq 2\psi_\beta = \frac{2kT}{e} \ln (N_A/\eta i) \qquad (1.2.12)$$

In figure 5a

1, $N_A = 10^{10}/cc$

2, $N_A = 10^{13}/cc$

3, $N_A = 10^{15}/cc$

4, $N_A = 10^{17}/cc$

In Figure 5b

1, $T = 215^{o}k$

2, $T = 250^{o}k$

3, $T = 300^{o}k$

4, $T = 350^{o}k$

The long vertical lines show the corresponding strong inversion potential $2\psi_B$ and shorter once to the left of 0.2V, corresponds to valence band and to the right of it corresponds to conduction band with the Fermi level at the origin.

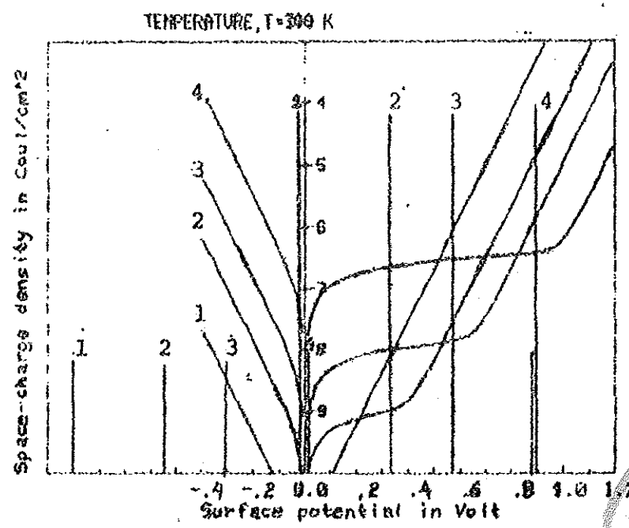


Fig 5a Concentration variation

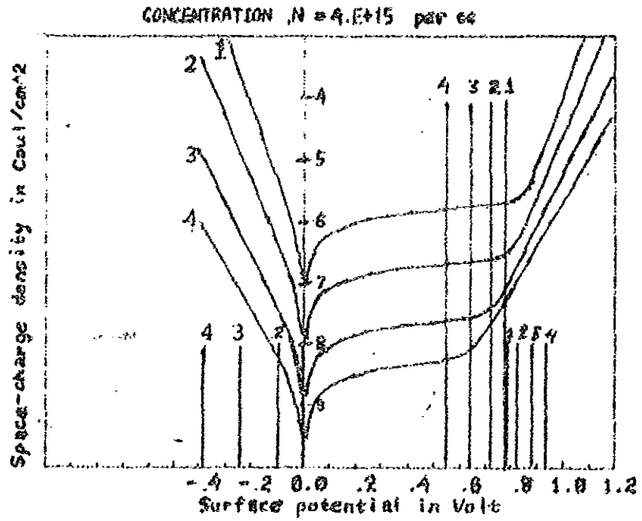


Fig 5b Temperature variation

Fig. 5

To determine the change in hole density ΔP, and electron density Δn, per unit area when ψ at the surface is shifted from zero to ψ_s, consider Fig. 6

$$P = \int_0^\infty (P(x) - P(\infty))\, dx \tag{1.2.13}$$

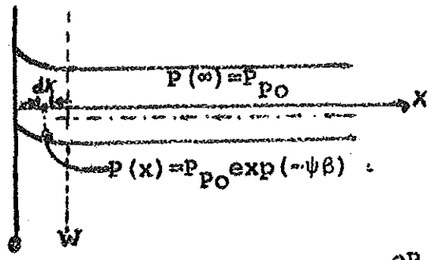


Fig 6

Making change of variable and the necessary substitution we get

$$\Delta P = \frac{eP_{po}L_o}{\sqrt{2kT}} \int_{\psi_s}^{o} \frac{(e^{-\beta\psi}-1)}{F(\beta\psi, \eta_{po}/P_{po})}\, d\psi \tag{1.2.14}$$

Similarly

$$\Delta n = \frac{e\eta_{po}L_p}{\sqrt{2kT}} \int_{o}^{\psi_s} \frac{(e^{\beta\psi} - 1)\, d\psi}{F(\beta\psi, \eta_{po}/P_{po})} \tag{1.2.15}$$

But one can see that $e\Delta n$ is nothing but Q_n, hence

$$Q_n = \frac{e^2\eta_{po}L_o}{\sqrt{2kT}} \int_{o}^{\psi_s} \frac{(e^{\beta\psi} - 1)\, d\psi}{F(\beta\psi\ ,\ \eta_{p}/P_{po})} \tag{1.2.16}$$

Relation between Q_n and Q_s can be found from Eq. (1.2.16) that

$$Q_n(\psi_s) = e\eta_{po}\varepsilon_s \int_{o}^{\psi_s} \frac{(e^{\beta\psi} - 1)\, d\psi}{Q(\psi)} \tag{1.2.17}$$

Limiting cases:

Case 1 $\psi_s \to 0$ that is $\psi \to 0$

$$Q(\psi) \simeq \frac{\psi \epsilon_s}{L_D} (1+ {}^{\eta po}/_{p_{po}})^{\frac{1}{2}}$$

$$Q_n \simeq \frac{e\eta_{po}\epsilon_s}{\epsilon_s/L_D(1+{}^{\eta po}/_{p_{po}})^{\frac{1}{2}}} \int_0^{\psi_s} \frac{(e^{\beta\psi}-1)}{\psi} d\psi \qquad (1.2.18)$$

Case 2 $\psi_s \to \infty$ (ψ_s very large), $\psi \to \infty$

$$Q(\psi_s) = Q_s \simeq \sqrt{2kT\epsilon_s \eta_{po}}\ e^{\beta\psi_s/2}$$

$$Q_n(\psi_s) \simeq \sqrt{2kT\epsilon_s \eta_{po}}\ e^{\beta\psi_s/2} \qquad (1.2.19)$$

From the above analysis, for small ψ, $Q_n(\psi_s) \to 0$ faster than Q_s (see Eq. 1.2.18). Hence, $Q_s \simeq eN_A W$ (see Eq.1.2.3). For large ψ $Q_n(\psi_s) \simeq Q_s$, which inturn shows that the depletion region ceases to change with increasing voltage.

To obtain potential as a function of position, consider Eq.(1.2.3). Space-charge density is given by

$$\rho = -(eN_A + Q_n/W) \qquad (1.2.20)$$

Solving posson's equation using conditions $\psi'(w)=0=\psi(w)$ we get

$$\psi = \psi_s(1-{}^{x}/_{W})^2 \quad , \quad \psi_s = \frac{W^2}{2\epsilon_s}(eN_A + Q_{n/W}) \qquad (1.2.21)$$

Relation between applied voltage and surface potential is obtained considering Fig 4e. Applied voltage v, is given by

$$V = V_o + \psi_s \qquad (1.2.22)$$

From the continuity condition, electric displacement vector at the insulation - semiconductor boundary

$$Q_s = \varepsilon_s \xi_s = \varepsilon_{ox} \xi_o \qquad (1.2.23)$$

where v_o is voltage drop across oxide, ε_{ox} is permitivity of oxide and ξ_o is electric field in insulator. Since $v_o = \xi_o d = (|Q_s|/\varepsilon_{ox})d$ using Eq. 1.2.11, Eq. 1.2.22 reduces to

$$V = \frac{\sqrt{2}kTd}{eL_D \varepsilon_{ox}} F(\beta\psi, \frac{\eta_{po}}{p_{po}}) + \psi_s \qquad (1.2.24)$$

When the applied voltage increases, ψ_s and w increases. Eventually strong inversion will occur at $\psi_s(inv) \simeq 2\psi_\beta$. Once strong inversion occurs, the depletion-layer width reaches maximum.. When bands are bent down far enough that $\psi_s = 2\psi_\beta$, the semiconductor is shielded from further penetration of the electric field by the inversion layer. Accordingly, the maximum width W_m of the surface depletion region under steady-state condition can be obtained from Eqs.1.2.12 and 1.2.21. It follows that

$$W_m \simeq \sqrt{\frac{2\varepsilon_s \psi(inv)}{eN_A}} = \sqrt{\frac{4\varepsilon_s kT \ln(N_A/\eta_i)}{e^2 N_A}} \qquad (1.2.25)$$

The turn - on voltage, V_T, at which strong inversion occurs can be obtained from Eqs 1.2.3(at V_T, $Q_s = eN_A W_M$), 1.2.12 and 1.2.25 and we get

$$V_T = \frac{d}{\epsilon_{ox}} \sqrt{2\epsilon_s e N_A (2\psi_\beta)} + 2\psi_\beta \qquad (1.2.26)$$

Computer program which shows the dependence of ψ_s on applied voltage for p-type silicon with N_A 10^{16} cm^{-3} and oxide thickness taken as a parameter is prepared. The result shows that for a given applied voltage when the oxide thickness is small surface potential is large and when oxide thickness is large surface potential is small. For very large oxide thickness ($\sim$ 40000Å) the graph almost coincides with ψ_s = 0 line, which shows that almost all applied voltage drop across the oxide. Name of the program is "Sp - Ap - V" (see Appendix A). Computer simulated graph is shown in Fig. 7.

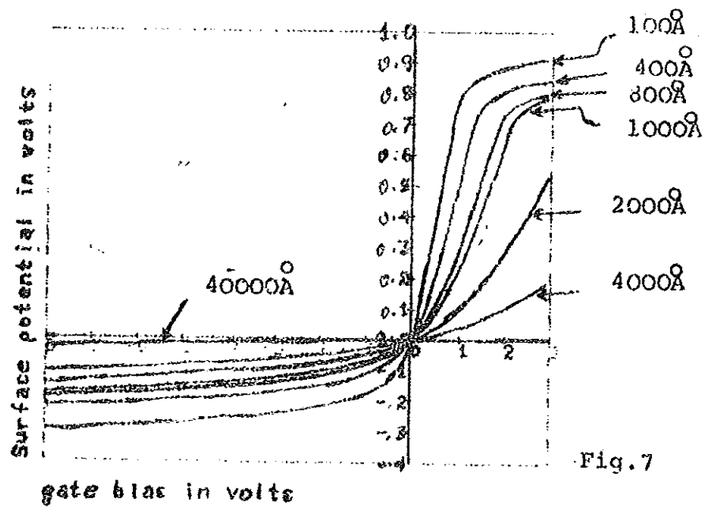


Fig.7

1.3 Capacitance of MOS structure

The charge distribution in MOS structure can be experimentally determined by the capacitance messurement. We have two types of capacitance, constant capacitance and differential capacitance. Constant capacitance is a capacitance value obtained simply by applying a dc bias on a capacitor. Whereas differential capacitance measurement is done by superimposing small alternating voltage on a dc bias with the help of capacitance bridge. Differential capacitance is the most important in MOS capacitance measurements because small-signal measurements determine the rate of change of charges with voltage.

To derive the small-signal equivalent circuit of the MOS capacitor consider Eq. 1.2.22, rewriting

$$v(t) = v_o + \psi_s(t) \tag{1.3.1}$$

$$v(t) = v + \delta v(t) \quad \text{and} \quad \psi_s(t) = \psi_s + \delta\psi_s(t) \tag{1.3.2}$$

$\delta v(t)$ - superimposed small ac voltage, $\delta\psi_s(t)$ - surface potential due to small ac voltage.

Field in the oxide $$\mathcal{E}_o = \frac{v(t) - \psi_s(t)}{d} \tag{1.3.3}$$

Using Gauss's law (see Eq. 1.2.22)

$$C_o\,(v(t) - \psi_s(t)) = -Q_s(t) \tag{1.3.4}$$

Where C_o is oxide capacitance per unit area

In addition there will be a small-signal variation in Q_s, $\delta Q_s(t)$. If $\delta Q_s(t)$ is small enough to be in the small-signal regime, it can be estimated using only the first term of a Taylor series expansion of Q_s.

$$Q_s(t) = Q_s(\psi_s + \delta\psi_s(t)) = Q_s(\psi_s) + \left(\frac{dQ_s}{d\psi_s}\right) \delta\psi_s(t)$$

$$Q_s(t) - Q_s(\psi_s) = - C_D(\psi_s)\,\delta\psi(t) \qquad (1.3.5)$$

$$C_D(\psi_s) = - \frac{dQ_s(\psi_s)}{d\psi_s} \qquad (1.3.6)$$

The equilibrim version of Eq. 1.3.4, that is, with no excitation is

$$C_o(v - \psi_s) = - Q_s(\psi_s) \qquad (1.3.7)$$

Subtracting Eq. (1.3.7) from Eq. (1.3.4) and using expressions in Eq. (1.3.2) and rearranging terms, we get

$$\delta\psi_s = C_o \left| C_D(\psi_s) + C_o \right|^{-1} \delta v \qquad (1.3.8)$$

Finally, the total capacitance per unit area C, which relates δQ_s to the small-signal ac gate voltage, becomes

$$C = - \frac{\delta Q_s}{\delta v} = - \frac{\delta Q_s}{\delta\psi_s} \frac{\delta\psi_s}{\delta v}$$

$$C = \frac{C_o C_D}{C_o + C_D} \qquad (1.3.9)$$

Eq. (1.3.9) Expresses the total capacitance per unit area of the MOS capacitor as a series combination of the silicon capacitor per unit area and the oxide capacitor per unit area. Since C_D is bias dependent it acts as a variable capacitor.

Explicit expression for C_D, can be obtained using Eq. (1.2.11)

$$C_D = \frac{\partial Q_s}{\partial \psi_s} = \frac{\varepsilon_s}{\sqrt{2} L_D} \cdot \frac{\left[1-e^{-\beta\psi_s} + \left(\frac{n_{po}}{p_{po}}\right)(e^{\beta\psi_s}-1)\right]}{F\left(\beta\psi_s, \frac{n_{po}}{p_{po}}\right)} \qquad (1.3.10)$$

At flat-band conditions, that is, $\psi_s = 0$, C_D is obtained expanding the exponential terms into series, and we obtain

$$C_D \text{ (Flat-band)} = \varepsilon_s / L_D \qquad (1.3.11)$$

Total capacitance at flat-band condition, that is, $v = 0$ ($\psi_s = 0$) is obtained using $C_o = \varepsilon_{ox}/d$ and Eqs. (1.3.9) and (1.3.11)

$$C_{FB}(\psi_s = 0) = \frac{\varepsilon_{ox}}{d + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right) L_D} \qquad (1.3.12)$$

Turn-on voltage (on set of strong inversion) capacitance is given by

$$C'_{min} \simeq \frac{\varepsilon_{ox}}{d + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right) W_M} \qquad (1.3.13)$$

Combination of Eq. (1.2.24), (1.3.9) and (1.3.10) gives the complete description of the ideal MOS c-v curve as shown in Fig. 8.

Low and High frequency capacitance

Low frequency capacitance is the capacitance measured under the condition that the minority carriers able to follow the source signal. It is said to be high requency capacitance if it is unable to follow the source signal. All the discussions above holds for low frequency capacitance. Even if it includes high frequency case, in-order to see the effect at high frequency consider Eq. 1.2.3 (P.11) From the definition of differential capacitance, $C = \frac{dQ_s}{dv}$, where dQ_s is increamental charge on the metal electrod for a voltage change dv. At high enough frequencies, when the minority carrier generation rate is too slow to follow the signal variation, dQ_s corresponds to the charge of hole distribution given by shaded area A in Fig. 4c. Hence high frequency capacitance is

$$c = \frac{dQ_s}{dv} \Big| Q_n = \text{const} \qquad (1.3.14)$$

From Eqs (1.2.3), (1.2.21) and (1.2.22)

$$v = \frac{Q_s^2}{2eN_A\epsilon_s} + Q_s \left(\frac{1}{C_o} - \frac{Q_n}{2eN_A\epsilon_s} \right)$$

From this $$Q_s = \frac{1}{2}\left(Q_n - \frac{2eN_A\epsilon_s}{C_o}\right) + \sqrt{\frac{2eN_A\epsilon_s}{C_o} - Q_n)^2 + 8eN_A\epsilon_s V} \qquad (1.3.15)$$

$$C = \frac{C_o}{\sqrt{\left(1 - \frac{Q_n C_o}{2eN_A\varepsilon_s}\right)^2 + \frac{2vC_o^2}{eN_A\varepsilon_s}}} \qquad (1.3.16)$$

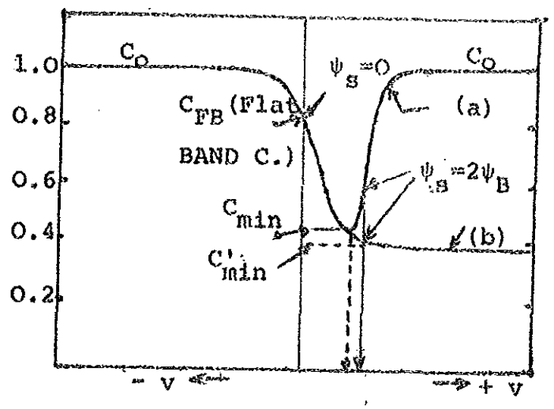


Fig. 8 MOS capacitance-voltage curves. (a) frequency (b) High frequency.

As to majority carriers, since its concentration is very large one can a assume continuous volume distribution of the charge (carriers). Characterstic response of the semiconductor (medium) is determined by majority carriers. Hence the life time of majority carriers is almost equal to the value of the time response of the medium which is equal to ε/σ, where ε permitivity of the medium, and σ conductivity of the medium. Usually it is of the order of 10^{-9} to 10^{-13} sec. Hence majority carriers can follow both high and low frequency signal sources.

Both low (a) and high (b) frequency c-v curves are shown in Fig. 8. It shows that at the left side (negative voltage) we have an accumulation of holes and therefore a

a high differential capacitance of the semiconductor. As a result the total capacitance is close to the insulator capacitance. As the negative voltage is reduced sufficiently, a depletion region is formed near the semiconductor surface, and the total capacitance decreases. The capacitance goes through a minimum, C_{min} (and corresponding voltage, V_{min}) and then increases again as the inversion layer of electron forms at the surface. Note that the increase of capacitance depends on the ability of the electron concentration to follow the applied ac signal. This only happens at low frequencies where the recombination-generation rate of minority carriers can keep up with the small-signal variation and lead to charge exchange with the inversion layer in step with the measurment signal.

Computer program for low-frequency c-v curve is prepared. File name is "C-V-Mos"(see Appendix A). It shows the dependence of capacitance on applied voltage with oxide thickness taken as a parameter. For very small oxide thickness($\sim 10^{O}$A) C_{min} is almost zero, the width of depression decreases tending to have constant value. As the oxide thickness increases the capacitance minimum shifts to the right and the width increases. For very large thickness ($\sim 40000^{O}$A)one can not find the depression, that is, the capacitance value is almost equal to the oxide capacitance. Curves obtained from computer simulation are shown in Fig. 9.

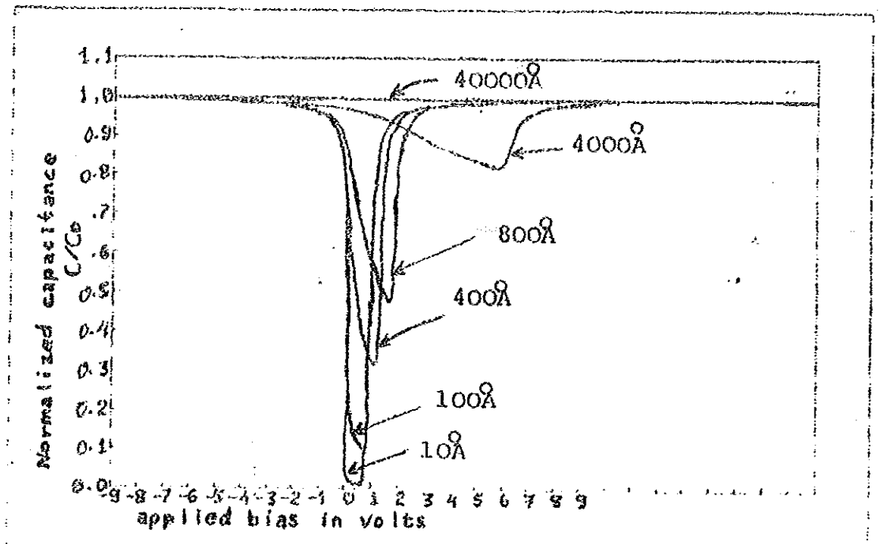

Normalized capacitance C/Co
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
40000Å
4000Å
800Å
400Å
100Å
10Å
-9 -8 -7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9
applied bias in volts

Fig. 9

CHAPTER 2

REAL - MOS STRUCTURE

Introduction

In the previous chapter ideal MOS structure were considered. In experimental study one can not find MOS structure that fulfill ideality conditions. But experiment is done on real MOS structure. Real MOS structure contains trap states | 5 | at the interface that contribute a space charge located at the surface. These interface traps and related charges affecte the ideal MOS characterstics. The space charge depends on the position of the Fermi level E_F at the surface and on the distribution of trap states across the band gap of the semiconductor.

MOS structure with charges related to traps are shown in Fig. 1. These are mobile and immobile charges in oxide. According to the standardized terminology given in 1980 | 4 |, mobile charges are mobile ionic charges (Q_m) (such as sodium and potasium ions) and immobiles are oxide trapped charge (Q_{ot}), fixed oxide charge (Q_f) and interface trapped charge (Q_{it})

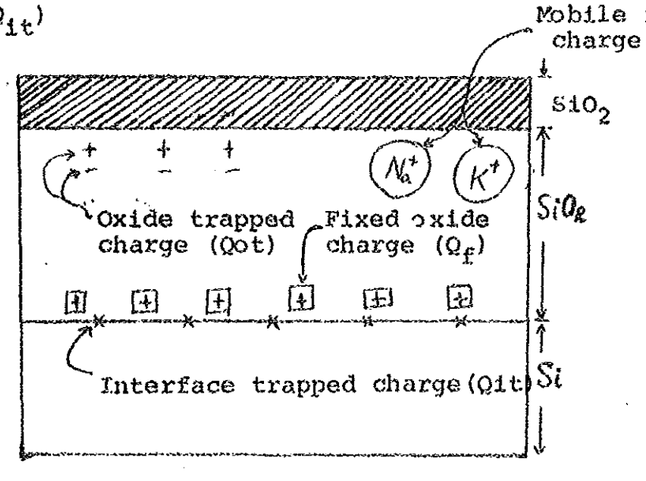


Fig. 1

Several other factors exist that affect ideal MOS characterstics. These are work function difference and other influences such as effect of temperature, illumination etc. There exists also current transport in oxide which has its own effect on MOS characterstics. In this chapter we are concerned primarily with these factors and related topics.

.1 Interface Trapped Charge and Surface States

.1.1. Interface Trapped Charge (Q_{it})

Interface trapped charges Q_{it}, which are located at the $Si - SiO_2$ interface exist with energy states in the forbidden band gap of silicon due to the interruption of the periodic lattice structure at the surface of a crystal as explained in section 2.1.2. They can also be created due to structural defects induced during the oxidation or metal impurities or other defects caused by high energy radiation or charge injection[4]. The existance of Q_{it} was confirmed experimentally by Shockley and Pearson in their surface conductance measurment.[6]

An interface trap. Where interface charges can be trapped, is considered a donor if it can become neutral or positive by donating (giving up) an electron. An acceptor interface trap can become neutral or negative by accepting an electron. The distribution functions for the interface traps are:

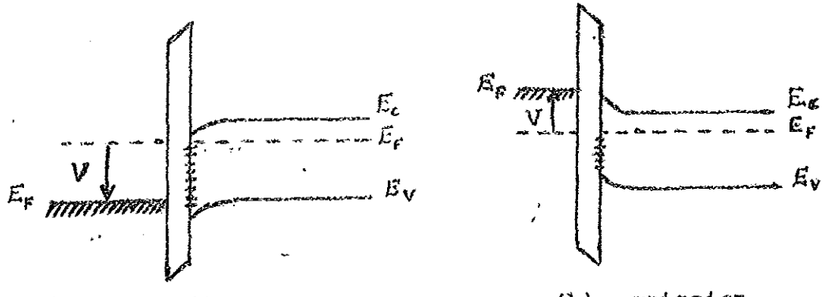
$$F_{SD}(E_t) = 1 - \frac{1}{1+{}^{1}/_{g}\ \exp(\frac{E_t - F}{kT})} = \frac{1}{1+g\ \exp(\frac{F-E_t}{kT})}$$

for donor interface taps and

$$F_{SA} = \frac{1}{1 + {}^{1}/_{g}\ \exp(\frac{E_t - F}{kT})} \qquad (2.1.2)$$

for acceptor interface traps, where E_t is the energy of interface trap, F is Fermi energy and g is ground-state degenenacy, which is 2 for donors and 4 for acceptor.[1]

When a voltage is applied, the interface-trap levels move up ordown with the valence and conduction bands, while the Fermi level remains fixed. A change of charge in the interface trap occurs when it crosses the Fermi level (Fig. 2). This change of charge contributes to the MOS capacitence and alters the ideal MOS curve.

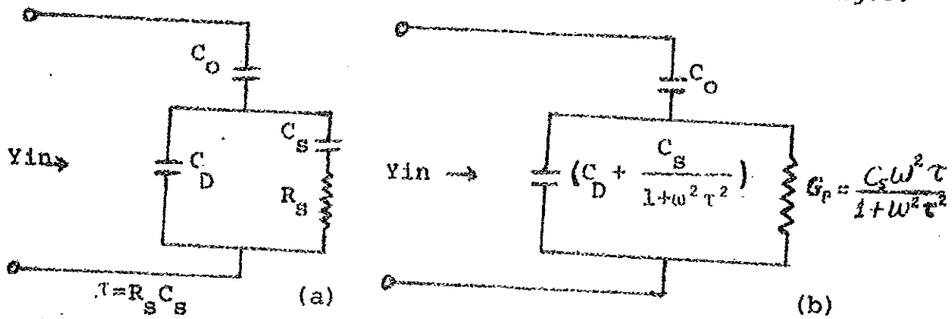


(a) trap filling (accumulation)

(b) emission

Fig. 2

EQUIVALENT CIRICUIT For ideal MOS structure total capacitance was considered to be a series combination of oxide capacitance and depletion layer capacitance. The basic equivalent circuit [1], first introduced by Lehovec and later improved by Nicollian and Goetzberger, incorporating the interface trap effect is shown in Fig.3.



In Fig 3, C_o and C_D are the oxide capacitance and semiconductor depletion layer capacitance, respectively, C_s and R_s are capacitance and resistance associated with interface-traps and are functions of surface potential. The product C_sR_s is defined as the interface-trap-life time, which

determines the frequency behaviour of the interface traps. The parallel branch of the equivalent circuit in Fig.3a can be converted into a conductance G_p in parallel with a capacitance C_p, as shown in Fig. 3b. Both G_p and C_p are frequency dependent.

$$\text{Admittance } y_p = G_p + i\omega C_p \qquad (2.1.3)$$

Using inverse relation of impedance and admittance, that is, $z = 1/y_p$ we obtain

$$y_p = \frac{\omega^2 \tau C_s}{1 + \omega^2\tau^2} + i\omega\left(C_D + \frac{C_s}{1+ \omega^2\tau^2}\right) \qquad (2.1.4)$$

Comparing Eqs. 2.1.3 and 2.1.4

$$G_p = \frac{\omega^2\tau \ C_s}{1+\omega^2\tau^2} \ , \ C_p = C_D + \frac{C_s}{1+\omega^2\tau^2} \qquad (2.1.5)$$

The input admittance y_{in} is given by

$$y_{in} = G_{in} + i\omega \ C_{in} \qquad (2.1.6)$$

Similarly

$$G_{in} = \frac{\omega^2 C_s \tau \ C_o^{\ 2}}{(C_o+C_s+C_D)^2 + \ \omega^2\tau^2 (C_o+C \ )^2} \qquad (2.1.7)$$

and

$$C_{in} = \frac{C_o}{C_o+C_D+C_s}\left\{C_D+C_s \frac{(C_o+C_s+C_D)^2 C_D\omega^2\tau^2 (C_o+C_D}{(C_o+C_s+C_D)^2+\omega^2\tau^2 (C_o+C_D}\right.$$

One can see that in the absence of ixerface traps i.e. $C_s = 0$, Eq. (2.1.7) reduces to Eq. (1.3.9).

Interface traps in the $Si - SiO_2$ system is comprised of many levels[1]. The levels are so closely spaced in energy that they cannot be distinguished as separate levels, and actually appears as a continuum over the band gap of the semiconductor (their nature will be discussed in the next section) Time constant of the equivalent circuit for an MOS structure with a single energy level should therefore be modified. We must also consider the statistical fluctuation of surface potential due to surface charges because small fluctuation in ψ_s causes a large fluctuation in τ, as seen from the relation

$$\tau = \frac{1}{\bar{v}\sigma_p n_i} \exp\left| - \frac{e(\psi_\beta - \psi_s)}{kT} \right| \quad \text{for p-type} \qquad (2.1.8)$$

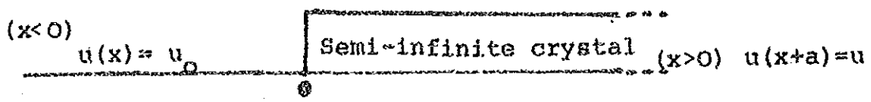
$$\tau = \frac{1}{\bar{v}\sigma_n n_i} \exp\left| \frac{e(\psi_\beta - \psi_s)}{kT} \right| \quad \text{for } \eta\text{-type}$$

refer Fig. 4 in chapter 1,

where σ_p and σ_n are the capture cross section of holes and electrons, respectively, and $\bar{v}$ is the average thermal velocity.[1] But this is not considered in this paper.

1.2 Surface States.

In order to understand the nature of interface state, let us consider the effect of crystal lattice boundry. The interruption of the periodic lattice structure at the surface of a crystal is a source for the formation of traps in the forbidden band gap. To see the changes which the existence of the boundaries introduce into the energy spectrum consider a one dimensional model of the lattice, Fig. 4.



In the interval $x<0$, $u(x) = u_o$ and in the interval $x > 0$ $u(x+a) = u(x)$, where a is the periodicity of the crystal lattice. Schrodinger equations in the first and second intervals are of the form

$$-\frac{\hbar^2}{2m}\frac{d^2\psi_1(x)}{dx^2} + u_o\psi_1(x) = E\psi_1(x) \quad x<0 \tag{2.1.9}$$

$$-\frac{\hbar^2}{2m}\frac{d^2\psi_2(x)}{dx^2} + u(x)\psi_2(x) = E\psi_2(x) \quad x>0$$

For $E<u_o$, solution in the first interval is given by

$$\psi_1(x) = Ae^{\varkappa x}, \quad \varkappa = \frac{\sqrt{2m(u_o-E)}}{\hbar^2} \tag{2.1.10}$$

where A is a constant.

Solution in the second interval: For large positive x the boundary will little affect electron motion, the solution should accordingly be in the form of Bloch functions.

$$\psi_2(x) = e^{\pm ikx}\varphi_{\pm k}(x)$$

continuity conditions at the boundary require k to be complex.

Let

$$k = k_1 + ik_2 \qquad (2.1.11)$$

Solution in the second interval is given by

$$\psi_2 = B\, e^{ik_1 x}\varphi_k(x)e^{-k_2 x} \qquad (2.1.12)$$

To find the relation between A and B consider the continuity of the wave function and its derivative at the boundary (x = 0)

$$\psi_1(0) = A = B\,\varphi_k(0) \qquad (2.1.13)$$

and

$$\psi_1'(0) = \mathcal{K} A = B\,(ik\,\varphi_k(0) + \varphi_k'(0)) \qquad (2.1.14)$$

It follows that, from Eqs. 2.1.13 and 2.1.14

$$\mathcal{K}\varphi_k(0) = ik\,\varphi_k(0) + \varphi_k'(0)$$

$$\mathcal{K} = ik + [\ln \varphi_k(0)]' \qquad (2.1.15)$$

The right hand side is complex one, on the other hand, $\mathcal{K}$ is real. Let,

$$| \ln \varphi_k(0) |' = \lambda + i\mu \qquad (2.1.16)$$

separating real and imaginary part. Substituting Eq. 2.1.16 into Eq. 2.1.15, rearranging and separating real and imaginary part, we get

$$\mathcal{K} = \lambda - k_2 , \quad k_1 = -\mu \qquad (2.1.17)$$

Expression for the energy $E(k) = u_o - \frac{h^2}{2m}(k_2-\lambda)^2$

(2.1.18)

There is definite band structure of $E(k) = E(k_1)$ for $k_2 = 0$. Possible values of $\mathcal{K}$ in the expression for the energy are limited by the condition $\mathcal{K} = \lambda$, where $\lambda = \mathrm{Re}\,[\ln \varphi_k(0)]'$, since $\varphi_k(x)|_{x=0}$ is a function of k. For $k_2 \neq 0$ and for fixed values of λ the energy turns out to be a quadratic function of k_2 for all value of λ. But this means that for $k_2 \neq 0$, new energy values appear in the energy spectrum of an infinite crystal, since in the latter case they were described by the condition $k_2 = 0$. New levels due to crystal boundaries should be located in the forbidden band. Consider the states which correspond to these levels:

$$\psi_1(x) = A\, e^{\mathcal{K}x} \qquad (x<0) \qquad (2.1.19)$$

$$\psi_2(x) = B\, e^{ik_1x} \varphi_k(x) e^{-k_2x} \qquad (x>0)$$

(2.1.20)

We see that the wave functions of states generated by the boundaries fall off exponentially both sides of the boundary it means that these states are localized within a boundary layer whose thickness is of the order of k_2^{-1}. The states are termed surface states, the additional levels are termed surface levels. The concrete form of the expression for surface levels depends on the form of the potential u(x) and the position of the boundary in respect to the field through $[\ln \varphi_k(0)]'$.

In addition to surface (Tamm) levels the surface layer contains many localized states due to numerous field imperfections (defects and adsorbed atoms). The number of states corresponding to Tamm levels is constant for a given crystal, but the number of states due to lattice deffects and adsorbed atoms may change depending on surface treatment. Various interactions are possible between the electron states on the surface and in the bulk of a crystal, and as a result surface states greatly affect physical processes in the semiconductor.

2.2 Oxide charges

Oxide charges include the oxide fixed charge Q_f, the oxide trapped charge Q_{ot}, and the mobile ionic charge Q_m.

Properties of fixed oxide charge [1]: - It is fixed and cannot be charged or discharged over wide variation of ψ_s; its density is not greatly affected by

the oxide thickness or by the type or concentration of impurities in the silicon ; it is generally positive and depends on oxidation and annealing conditions, and on the silicon orientation. The origin of fixed oxide charge was suggested to be excess silicon or the loss of an electron from oxygen centers.

The presence of Q_f at the interface causes the shift along voltage axis of c-v curve (high frequency) discussed in chapter 1. For both n-type and p-type substrates, positive Q_f causes the c-v curve to shift to more negative values of applied d.c. bias with respect to the ideal c-v curve, while negative Q_f causes the c-v curve to shift to more positive voltage. The magnitude of the shift is given by

$$\Delta v_f = Q_{f/c_o} \qquad (2.2.1)$$

where c_o is oxide capacitance per unit area and Q_f fixed oxide charge per unit area.

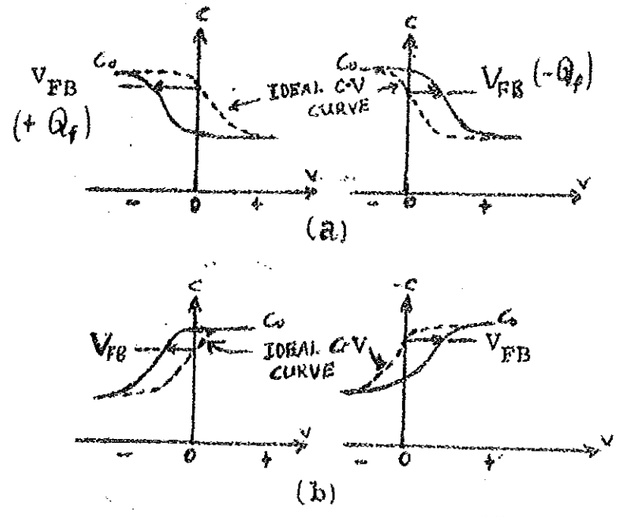


Fig.5. C-V curve shift alon the voltage oxide due to positive or negative fixed oxide charge.

(a) For p-type semiconducto

(b) For n-type semiconducto

It was fist demonstrated by Snow et.al [8], that alkali ions, such as sodium, in thermally grown SiO_2 films are mainly responsible for the instability of the oxide-passivated devices. Reliability problems in semiconductor devices operated at high temperatures and voltages may be related to the contamination by alkali metal ions, because under these conditions mobile ionic charges can move back and forth through the oxide layer depending on biasing conditions and thus give rise to voltage shifts. Large concentration of alkali ions at Si - SiO_2 interface causes large flat-band voltage shift and device instability. The flat-band voltage shift due to mobile ionic charge is given by

$$\Delta v_m = Q_m/c_o \qquad (2.2.2)$$

where Q_m is the effective net charge of mobile ions per unit area at the Si - SiO_2 interface.

Oxide trapped charge also can cause a voltage shift of the MOS c-v curve. These oxide traps are associated with defects in SiO_2. The oxide traps are usually electrically neutral, and are charged by introducing electrons and holes [1] into the oxide. The voltage shift due to this oxide trapped charge is given by

$$\Delta v_{ot} = \frac{Q_{ot}}{c_o} \qquad (2.2.3)$$

where Q_{ot} is the effective net charge in bulk oxide traps per unit area at the Si - SiO_2 interface. The

total voltage shift due to all the oxide charges is given by

$$\Delta v = \Delta v_m + \Delta v_f + \Delta v_{ot} = Q_o/c_o ,$$

$$Q_o = Q_m + Q_f + Q_o t \qquad (2.2.4)$$

Q_o is the sum of the effective net oxide charge per unit area at the $Si - SiO_2$ interface.

Voltage shift, Δv expressed above can be obtained by the application of Gauss' law. One can consider the possibility of a volume charge distribution $\rho(x)$ [8] within the oxide as shown in Fig 6.

Fig. 6

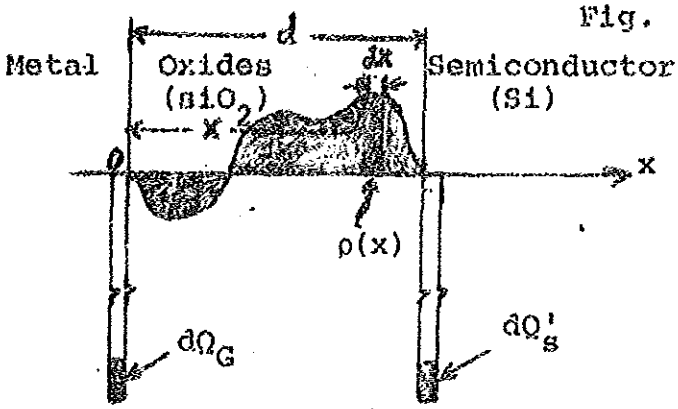


Fig. 6. Charge induced in the metal electrod and in the semiconductor substrate by an arbitary distribution of $\rho(x)$ in the oxide.

The element of oxide space charge $\rho(x)\,dx$ induces a charge

$$dQ_G' = \frac{(x-d)}{d}\,\rho(x)\,dx \quad \text{in metal}$$

and $dQ_s' = -\frac{x}{d}\,\rho(x)\,dx$ in the semiconductor. Here x is measured from the metal-oxide interface. Total charge induced in metal and semiconductor are

$$Q_G' = \int_0^d \frac{x-d}{d} \rho(x)\,dx \qquad (2.2.5)$$

and $$Q_s' = -\int_0^d \frac{x}{d} \rho(x)\,dx \qquad (2.2.6)$$

Note that $$Q_G' + Q_s' = -\int_0^d \rho(x)\,dx = Q_o \qquad (2.2.7)$$

where Q_o is total charge per unit area in the oxide. A voltage of $-Q_s'/C_o$ would be required to induce a charge Q_s' in the silicon. Hence the effect of the charge Q_s' in the oxide is to shift the c-v curve along the voltage axis by an amount

$$\Delta V = -\frac{Q_s'}{C_o} = \frac{1}{C_o} \left| \frac{1}{d} \int_0^d x\rho(x)\,dx \right| \qquad (2.2.8)$$

2.3 Work-Function Difference and other influences.

2.3.1 Work-Function difference

The effect of a work function difference ϕ_{ms} between the metal and the semiconductor is simply additive [8] to that of the applied field plate voltage and results in a shift of the c-v curve along the voltage axis. For an ideal MOS structure, it has been assumed that the work function difference (chapter 1, Fig. 2) for a p-type semiconductor,

$$\phi_{ms} = \phi_m - (\chi + Eg/2e + \psi_B) \qquad (2.2.1)$$

is zero. If the value of ϕ_{ms} is not zero, the effective

voltage across the MOS structure is

$$V_{eff} = V_G - \phi_{ms} \qquad (2.2.10)$$

which leads to voltage shift from the ideal theoretical curve by an amount.

$$V_G - V_{eff} = \phi_{ms} \qquad (2.2.11)$$

If interface trapped charge Q_{it} and oxide charges Q_o exist the effective voltage across the MOS structure is

$$V_{eff} = V_G + \frac{Q_o + Q_{it}}{C_o} - \phi_{ms} \qquad (2.2.12)$$

which leads to voltage shift V_{FB} from the ideal theoretical curve by an amount

$$V_G - V_{eff} = V_{FB} = \phi_{ms} - \frac{Q_o + Q_{it}}{C_o} \qquad (2.2.13)$$

where V_{FB} is called flat-band voltage shift.

2.3.2 Other influences

There are factors other than work function difference interface trapped charges and oxide charges which affect the MOS properties. Some of these are temperature, ionization radiation and illumination.

Let us consider the effect of illumination.

The main effect of illumination on the MOS capacitance-voltage curve is that the capacitance in the heavy inversion region approaches the low frequency

value as the intensity of illumination is increased. Two mechanisms are responsible for this effect [10]; first, the decrease of the time constant for generation of the inversion layer and, second, the decrease of the space-charge region by an effective decrease in the surface potential under illumination. In order to compare the quantitiative importance of the two mechanisms,

first evaluate the influence of illumination on the MOS capacitance, considering only the influence on time constant of inversion layer generation [10]. We shall express the time constant, θ as $\theta = N/u$, N being the density of acceptors or donors in the semiconductor and u the generation rate of minority carriers in the space - charge region. Approximate expression for u [10] is

$$U = n_i/\tau \qquad (2.3.6)$$

where n_1 is intrinsic concentration of carriers in the semiconductor, and τ is life time of minority carriers.

Under illumination, assuming a rate of generation g of hole - electron pairs by photons, the value U will become

$$U = \frac{n_i}{\tau} + g = \frac{n_i + g\tau}{\tau} \qquad (2.3.7)$$

it follows that the time constant decreases to

$$\theta = \frac{N\tau}{n_i + g\tau} \qquad (2.3.8)$$

The second mechanism is the influence of illumination on surface potential [10]. The limit (maximum) value of the depletion region versus the surface potential $\psi_s(inv)$ is given by Eq. 1.2.25 which is

$$W_m = \sqrt{\frac{2\epsilon_s \psi_s(inv)}{eN}} \qquad (2.3.9)$$

The reduction of the width of the space - charge layer as a result of decrease in surface potential leads to a corresponding increase of capacitance. This mechanism is independent of the frequency of measurement and is the predominant one at high frequencies.

2.4 Carrier Transport in Insulating films(oxides).

In an ideal MOS structure current carrier transport was neglected. It was based on the assumption that conductance of the oxide film is zero. Real oxides (insulator), however, show carrier conduction when the electric field and temperature is sufficiently high. One can estimate the electric field in an oxide under biasing conditions, from the continuity of displacement vector at Si - SiO_2 boundary.

$$\xi_o = \xi_s \left(\epsilon_s / \epsilon_{ox} \right) \qquad (2.4.1)$$

where ξ_o and ξ_s are the electric fields in the oxide and the semiconductor, respectively, and ϵ_{ox} and ϵ_s are the corresponding permitivities.

Different conduction processes[1] are described for carriers in oxide. Some of them are considered here.

If metal and oxide or oxide and semiconductor or metal and semiconductor are brought into contact, energy barrier with a certain barrier height will be formed at the interface. But there is a possibility for a carrier to have energy greater or equal to barrier height or less. Those having energy greater or equal to barrier height can be transported by Schottky emission process. In this case thermionic emission across the metal-oxide interface or the oxide-semiconductor interface are responsible for carrier transport. It depends both on termperature and applied field. Functional dependence is given by

$$J = A^* T^2 \exp - \left| \frac{(\phi_B - \sqrt{q\xi/4\pi\varepsilon_{ox}})}{kT} \right| \qquad (2.4.2)$$

where A^* is effective Richardson constant. Those having energy less than barrier height can be transmitted by tunnelling. It is a dominant process for a heavily doped semiconductor or for operation at low temperature. The tunneling is caused by field ionization of trapped electrons into the conduction band. The tunnel emission has the strongest dependence on applied voltage but is essentially independent of temperature. Functional dependence is given by

$$J \sim \xi^2 \exp\left| - \frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar\xi} \right| \qquad (2.4.3)$$

There exists also emission process where we have both thermionic and tunnel emission known as Frenkel-Pool emission. It is due to field-enhanced thermal excitiation of trapped electrons into the conduction band . Functional dependence is given by

$$J \sim \xi \exp\left| - q\,(\phi_B - \sqrt{q\xi/\pi\varepsilon_{ox}})/kT \right| \qquad (2.4.4)$$

To write it explicitly, temperature dependence is

$$J \sim e^{-a/T} \qquad (2.4.5)$$

and field dependence is given by

$$J \sim \xi e^{b\sqrt{\xi}} \qquad (2.4.6)$$

where a and b are constants. From the above relation one can see that the current increases as temperature and field increases.

CHAPTER 3

Measurement techniques

Introduction

The experimental techniques used to examine interfaces including those developed for surface studies as well as those that can probe deeper in to the solid. Their features were recently summarized by WEAVER[17].

Ultraviolet or x-ray radiation photoemission techniques are sensitive to the chemical state of atoms in the over layer as well as to their distribution and can therefore detect changes in bonding and charge distribution. Low energy electron diffraction reveals whether there is ordering on the surface and gives structural information. Auger and angle resolved Auger spectroscopies use electrons to identify the atomic species present and to determine their spatial distribution; these spectroscopies also reveal the structure of overlayer through diffraction modulation. Inverse photoemission, in which electrons stimulate the emission of photon, is a promising technique that gives detailed information about the empty electronic states in interface. Electron spin resonance(ESR) is chemically diagnostic analytic technique that can

reveal the nature atomic scale or point defects, the one most suitable for Si and SiO_2 interface[18].

There are different measurement techniques electrical, thermal and measurements mentioned above. they are listed here only for completeness. It was capacitance measurement method that have been applied in recent years to study interface properties. A great variety of different methods that have been suggested are shown in table 1.

This paper will summarize three approaches of electrical measurements:

- the quasistatic capacitance method.
- the conductance method.
- the Deep Level Transient spectroscopic(DLTS) method. These methods are singled out because of their specific features when used in practical measurements.

The quasistatic method the most versatile method. It is usually applied for first inspection of unknown samples, and it derives its significance from the fact that it is a powerful diagnostic tool for many particular features in MOS structures.

The conductance method and the DLTS method, on the other hand, belong to the most sensitive methods

for investigating interface state distributions.

As MOS measurement techniques have been reviewed several times[4], the experimental approaches of the methods mentioned above will therefore be only briefly dealt with here. Particularly in the passage on the quasistatic method, the measurement principles and diagnostic aspects will be emphasized. In the conductance method measurement principle and its advantage as compared to quasistatic capacitance method are described. As for DLTS method emphasis is put the principles of measurements.

Measurements are made with the help of charge exchange processes in the interface states. It is well established that the interface states behave like Schockley-Read centers. Virtually all procedures which are found in the literature for evaluating measured capacitance data are based on the Schockley-Read-Hall(SRH) theory of generation -recombination centers. According to this theory a trap(interface trap) is said to be SRH recombination center:

1, the trap is assumed to have energy level in the energy gap so that its charge may have either of

two values differing by one electronic charge. That is, either negative or neutral, similarly either positive or neutral.

2, recombination occurs through the mechanism of trapping.

3, the time required for an electron trapped in an excited state to fall to ground state is negligible. This theory provides us with quantitative relation between the interface properties and the phenomena observed experimentally. One of the properties which can be extracted from capacitance measurement is the interface state density Dit. It can be a function of the energy in the forbidden gap.

In capacitance measurement, if a small sinusoidal signal voltage is applied to a MOS capacitor, the energy bands of the semiconductor are bent a little upwards or downwards with the interface state centers moving accordingly (see Fig 2, Chapter 2). Only interface state crossing the Fermi-level are charged and discharged. All other interface trapped charges further away from the Fermi-level remain unchanged. We may therefore infer: In capacitance

measurement the Fermi function acts as a probe for interface states. The Fermi-level can easily be shifted across the forbidden gap, and in this way the interface state distribution can be scanned. Shifting of the Fermi-level can be performed either by bending the energy bands by the bias voltage or by a temperature variation.

The conductance method and the quasistatic method are typical examples in which this kind of charge exchange is employed.

Another basic process of charge exchange is the emission of charge carriers from occupied interface traps. By appropriate biasing program the interface states are first filled with majority carriers, which in the subsequent period are thermally emitted. According to the SRH theory the emission time constant of an interface trap at energy E_T may be expressed as

$$\tau^{-1} = \sigma_n v_{th} N_c \left[\exp\left(- \frac{E_c - E_T}{kT} \right) + \exp\left(- \frac{E_T - E_V}{kT} \right) \right] \quad \ldots (1)$$

where N_c is the effective density of states in the conduction band. In case the interface trap is much above the Fermi-level, say more than 3kT, then Eq. (1) reduces to

$$\tau^{-1} = \sigma_n v_{th} N_c \exp\left(- \frac{E_c - E_T}{kT} \right) \quad \ldots (2)$$

DLTS method is an example of the study of emission processes.

Table 1 methods suggested for investigating MOS interfaces[4].

High frequency methods (room temperature)

High frequency methods (low temperature)

Capacitance derivative

Isothermal transient methods

Thermally simulated measurement

MOS transistors :

Channel conductance and transconductance

Charge pumping

Subthreshold current

Noise measurements

Charge coupled devices

Photoelectric measurements

Electron spin resonance.

3.1 Quasi-static Capacitance-Voltage(CV) Technique.

The C-V measurement on MOS capacitor structure is the standard method in laboratory practice for determining the distribution of interface states in the forbidden band gap of Silicon. This is done using low and high frequency capacitance value. Low

frequency means that the interface states and minority carriers should respond fully to the test frequency. This condition requires a test frequency lower than of the order of 1 to 10^{-2} Hz. Accurate capacitance measurement at such low frequencies are very difficult to perform. This difficulty was over come by the quasistatic or slow ramp technique[4]. The opposite is true for high frequency and the differential capacitance is recorded by a commercial bridge.

The basic idea for low frequency capacitance measurement is quite simple. A slowly rising voltage ramp is applied to the capacitor under test, and the current is recorded as a function of applied voltage V. The current is proportional to the differential capacitance at the instantaneous voltage V :

$$I = C(V) \frac{dV}{dt} \qquad \ldots \quad 3.1.1$$

The shape of the C-V curve is thus reflected in the shape of the quasistatic displacement current if a linearity of ramp voltage is secured. In order to meet the low frequency requirements the voltage variation with time must be slow. Typical value

vary between 10 mv/s and 100 mv/s. Current, which are often smaller than 10^{-13}A, have to be measured accurately.

Extraction of interface state properties from capacitance measurement is done conveniently using the combined low and high frequency capacitance measurement. As it is explained in Sec. 2.2.1 the effect of interface state is to introduce capacitor parallel to depletion layer capacitor in the semiconductor. Total capacitance of the semiconductor is given by

$$C = C_S + C_D \qquad \ldots 3.1.2$$

Where C_S is interface state capacitance and C_D is depletion layer capacitance in the absence of interface state. At high frequency the interface state is unable to follow test frequency, which results to $C_S = 0$. At high frequency the above equation reduces to $C = C_D = C^S_{HF}$. Hence Eq. 3.1.2 can be written as

$$C^S_{LF} = C_S + C^S_{HF} \Leftrightarrow C_S = C^S_{LF} - C^S_{HF} \qquad \ldots 3.1.3$$

where C^S_{LF} and C^S_{HF} are low and high frequency capacitance of the semiconductor respectively. But it is not the semiconductor capacitance that is to be measured, rather it is the capacitance of MOS

structure. C_s should be expressed interms of capacitance at low and high frequency of MOS structure. Capacitance of the structure is assumed to be series combination of oxide and depletion layer capacitance. That is,

$$\frac{1}{C_{LF}} = \frac{1}{C_o} + \frac{1}{C^s_{LF}}$$

From this we get $$C^s_{LF} = \frac{C_{LF}}{1 - C_{LF}/C_o}$$

Similarly $$C^s_{HF} = \frac{C_{HF}}{1 - C_{HF}/C_o}$$

where C_{LF} and C_{HF} are low and high frequency capacitance of the structure and C_o is oxide capacitance. Hence

$$C_s = \frac{C_{LF}}{1 - C_{LF}/C_o} - \frac{C_{HF}}{1 - C_{HF}/C_o} \quad \ldots \quad 3.1.4$$

From the definition of interface state density D_{it}, $D_{it} = \frac{1}{q}\frac{dQ_{it}}{dv} = \frac{C_s}{qA}$ number of charge/$cm^2 eV$ Where Q_{it} is interface trapped charge per unit area, q is the elementary charge, and A the metal plate area. Thus the interface-state density is determined in the depletion region by the difference between the high and low frequency capacitance,

$$D_{it} = D_{it}(v) = \frac{C_o}{qA}\left[\frac{C_{LF}/C_o}{1 - C_{LF}/C_o} - \frac{C_{HF}/C_o}{1 - C_{HF}/C_o}\right]$$

... 3.1.5

This equation given the dependence of D_{it} on the gate voltage and not yet on the energy in the forbidden gap.

The relation between the gate voltage and energy in the forbidden band gap is provided by Berglund integration method[4]. When oxide trapped charges and mobile ionic charges can be neglected we obtain from the relation $V = V_o + \psi_s$ and the fact that $dQ = C_o dV_o = CdV$

$$\frac{\partial \psi_s}{\partial V} = 1 - C/C_o \qquad \text{and} \qquad \frac{\partial \psi_s}{\partial V_o} = \frac{C_o}{C} - 1$$

... 3.1.6

Integrating the first equation from v_1 to v_2 yields

$$\psi_s(v_1) - \psi_s(v_2) = \int_{v_2}^{v_1} [\,1 - C/C_o\,]\, dV \qquad \ldots \quad 3.1.7$$

This equation indicates that the surface potential at any applied voltage can be determined by integrating a curve of $\left[1 - \frac{C}{C_o}\right]$. Note that this equation is valid only when the interface trapped charges are in equilibrium at all times during the measurement of C(v); i.e the measurement frequency

must be low enough so that all interface traps can follow both the gate bias and the ac signal. The energy E_T of the interface trap is then given by

$$E_T - E_C = (E_F - E_C)_b + q\psi_s \qquad \ldots \quad 3.1.8$$

where the subscript b indicates that the difference is to be taken in the neutral region of the bulk of the semiconductor. The requirement of charge neutrality in the MOS system gives us the following relation. In addition to the space charge density in the semiconductor (Q_s), we now have $D_{it}(q\psi_s) = D^d_{it}(q\psi_s) + D^a_{it}(q\psi_s)$, where D^d_{it} and D^a are the donor and acceptor interface trap densities respectively. The charge neutrality requirement gives

$$\frac{\epsilon_{ox} V_o}{d} = q \int_{E_V}^{E} \left[D^d_{it} F_{SD}(E_t) - D^a_{it} F_{SA}(E_t) \right] dE_t + Q_s \qquad \ldots \quad 3.1.9$$

Differentiating Eq. 3.1.9 w.r.t ψ_s gives

$$\frac{\partial \psi_s}{\partial V_o} = \frac{\epsilon_{ox}/d}{\left[\frac{dQ_s}{d\psi_s} \right] + q^2 D_{it}(q\psi_s)} \qquad \ldots \quad 3.1.10$$

From the second relation in Eq. 3.1.6 and Eq. 3.1.7, a curve of $\frac{\partial \psi_s}{\partial V_o}$ versus ψ_s can be obtained directly using the low frequency

capacitance measurement of a MOS structure. If doping density of the semiconductor and the temperature are known, comparing this curve to the one given by Eq. 3.1.10 accurately determined D_{it}.

3.1.1 MOS Diagnostic by the Quasistatic Technique

A) Doping density

The most popular method for the first inspection of the doping density is the so called C_{min}/C_{max}- method. In inversion the space charge capacitance is a unique function of the doping concentration. In order to obtain the space charge capacitance one only need to determine the oxide capacitance (C_{max}) and the high-frequency capacitance in inversion, $C_{inv}(C_{min})$. Simple way for the determination of the surface charge is described by Whelan[16] using bias to obtain flat band condition. The voltage across the MOS structure is $V = V_o + \psi_s$ and charges are $Q_g = Q_{ss} + Q_{sc}$, where Q_{ss} is surface charge and Q_{sc} is space charge. Total charge of surface state is $Q_{ss} = C_o V_{fb}$ according to the discussion in chapter 2, section 2.

Procedure to determine the density of surface states;

a) First to measure high frequency curve and to determine C_{max} ,i.e, C_o(oxide capacitance).

This oxide capacitance is determined either by the average capacitance in the accumulation region or using the method developed by McNutt and Sah.[21] Formula to apply this method was derived as follows[24]. Formula for C_D applicable in accumulation.

$$C_D(\text{S.C. capacitance}) = \frac{\text{Sgn}(U_s)\epsilon_s\left[1 - \exp(U_s)\right]}{\sqrt{2}\, L_n\left[U_s - 1 + \exp(-U_s)\right]^{\frac{-1}{2}}} \quad \ldots \quad 3.1.11a$$

$U_s = \beta\psi_s = \frac{e\psi_s}{kT} < -4$ for P-Si

the approximation $4 < -U_s << \exp(-U_s)$ can be used in Eq(3.1.11a) to give

$$C_D = \epsilon_s/\sqrt{2}\, L_D \exp(-\frac{1}{2} U_s) \quad \ldots \quad 3.1.11b$$

Similar approximation used in the bias(voltage) expression

$$V = V_{FB} + \psi_s + U_s(kT/e)(C_{Di}/C_o)F(\beta\psi_s, n_{p_o}/p_{p_o})$$

Simplify it to

$$V = V_{FB} - \sqrt{2}\,(kT/e)(\epsilon_s d/\epsilon_{ox} L_D)\exp(-\frac{1}{2} U_s) \quad \ldots \quad 3.1.11c$$

where C_{Di} is intrinsic Debye capacitance.

$$\frac{dC_D}{dU_s} = -\frac{\epsilon_s}{2\sqrt{2}\,L}\exp\left(-\frac{1}{2}U_s\right) \qquad \ldots \quad 3.1.11d$$

$$\frac{dV}{dU_s} = \frac{\sqrt{2}\,kT}{e}\,\frac{\epsilon_s}{2L_D C_o}\exp\left(-\frac{1}{2}U_s\right) \qquad \ldots \quad 3.1.11e$$

So that $$\frac{dC_D}{dV} = -\frac{eC_o}{2kT} \qquad \ldots \quad 3.1.11f$$

from $$C = \frac{C_D\,C_o}{C_o + C_D} \qquad \ldots \quad 3.1.11g$$

we get

$$\frac{dC}{dV} = \left(\frac{C_o}{C_o + C_D}\right)^2 \frac{dC_D}{dV} \qquad \ldots \quad 3.1.11h$$

Using Eq. 3.1.11f

$$\left(-\frac{dC}{dV}\right)^{1/2} = \left(\frac{e}{2kTC_o}\right)^{1/2}(C_o - C) \qquad \ldots \quad 3.1.11i$$

This relation provides a rapid and accurate graphical or numerical method of obtaining C_o from the measured C-V data.

b) To determine C_{min} from high frequency curve, with the help of this one can determine the minimum capacitance of the space charge region. It is given by

$$C_{sc} = \frac{C_o C_{min}}{C_o - C_{min}}$$

c) From the theoretical curve determine the space charge capacitance C_{SCFB} for flat band condition.

d)evaluate the total flat bound capacitance C_{FB} of the MOS structure for V_{FB}.

$$C_{FB} = \frac{C_o C_{SCFB}}{(C_o + C_{SCFB})}$$

e) For this quantity C_{FB} determine on the measured curve the corresponding flat band bias V_{FB}.

f) Effective surface charge density is

$$\frac{Q_{ss}}{A} = \frac{C_o V_{FB}}{A} = eN_{ss}.$$

g) It follows that the density of surface states is equal to

$$N_{ss} = \frac{Q_{ss}}{eA}$$

where A is metal plate area and e is electronic charge.

B) Doping profiles

Doping profiles can be determined by evaluating the space charge capacitance in depletion:

$$N(W) = \frac{2}{q\varepsilon_s}\left[\frac{d(1/C_D^2)}{d\psi_s}\right] \qquad \ldots \quad 3.1.12$$

$$W = \varepsilon_s / C_D$$

W is the space charge width and simultaneously the position where the doping is determined. This method was first published by Schottky 1942. The stretch-out of the C-V curve by interface states

give rise to factitious profiles. This effect can be eliminated by taking the low frequency capacitance too into consideration[14]. J.R Brews[24] was shown that the apparent doping profile obtained from $1/C_{HF}^2$ vs V plot can be corrected for interface-state effect to obtain a more accurate doping profile. This more accurate doping density N(W), at distance W from semiconductor-oxide interface is related to the uncorrected density, $N_o(W)$, obtained by neglecting interface states, is given by[14]

$$N(W) = N_o(W)\frac{\left(1 - C_{LF}/C_o\right)}{\left(1 - C_{HF}/C_o\right)} \qquad \ldots \quad 3.1.13$$

$$N_o(W) = \frac{2}{q\epsilon_s}\left[\frac{d(1/C_{HF}^2)}{dV}\right]^{-1}$$

USE OF EQUATION 3.1.13 IN INVERSION

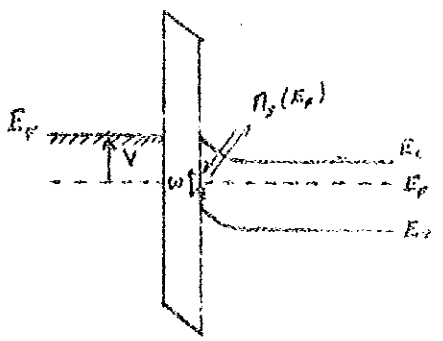
Eq. 3.1.12 is equivalent to Eq. 3.1.13. They yield the true doping density only when the depletion approximation is valid[14], i.e, only when a change in charge in the semiconductor, dQ, is related to a change in the depletion width, dw, by

$dQ = qN(W)dW$ and $dQ = C_D d\psi_s$ 3.1.14

then, the standard result of Eq. 3.1.13 results at once. In other words, the standard formulas of Eq. 3.1.13 and Eq. 3.1.12 are valid so long as any change in voltage across the capacitor is compensated by an increase in depletion width. This will not be the case with inversion, where the change in voltage is partly compensated by minority carrier piling up at the interface. However, so long as the change in the depletion-layer charge, Eq. 3.1.14 remains approximately valid, and hence does Eq. 3.1.12.

3.2 Conductance Method

In the conductance technique, the full frequency dispersion of the MOS capacitance is analyzed, rather than just the high and low-frequency capacitance. In the same manner as for the quasistatic technique, the Fermi energy is used to probe the energy position of the interface states.



Basic measurement principle of the quasi-static and the conductance techniques. The Fermi energy at the interface is used to probe the energy position of the interface state.

The accuracy in the quasistatic capacitance technique relies on two measured quantities (C_{LF} and C_{HF}), whereas in the conductance technique much more measurement data are available so that more advanced data processing schemes along with data averaging and smoothing may be employed. The conductance technique can give more accurate results, especially for MOS structure with relatively low interface - trap density (10^{10} $eV^{-1}cm^{-2}$) as in the thermally oxidized Si - SiO_2 system.

The simplified equivalent circuit (Fig.3, chapter 2) illustrates the principle of the MOS conductance technique. As suggested by Nicollian and Goetzberger[4] (leads to another reference), the admittance of the MOS structure is measured by bridge across the terminals. The oxide capacitance is measured in the region of strong accumulation. The admittance of the circuit is then converted in to impedance. The reactance of the oxide capacitance is subtracted from this impedance and the resulting impedance converted back in to admittance. This leaves C_p in parallel the series R_sC_s net work of the interface traps. The

capacitance and equivalent parallel conductance are given by Eq. 2.1.5(chapter 2). G_p does not contain C_o and depends only on the interface trap branch of the equivalent circuit. At a given bias, G_p/ω given by

$$G_p/\omega = \frac{C_s \omega\tau_s}{1 + \omega^2\tau^2} \qquad \ldots \quad 3.2.1$$

can be measured as a function of frequency. A plot of G_p/ω versus $\omega\tau$ goes through a maximum when $\omega\tau = 1$, and gives τ directly. The value of G_p/ω at the maximum is $C_s/2$. Thus, equivalent parallel conductance corrected for C_o gives C_s and τ ($=R_sC_s$) directly from the measured conductance. Once C_s is known, the interface trap density is obtained using the relation $D_{it} = \frac{C_s}{qA}$, where A is the metal plate area.

3.3 The DLTS method

DLTS method is also useful to determine interface traps in MOS capacitors. The method was first devised by Lang in 1974. It was first intended for studying bulk traps in Schottky diodes or pn junctions. The method turned out to be very efficient. It was soon after modified so that it

was fit to the investigation of interface states in MOS structures, too.

The measurement principle proceeds as follows: The sample is repetitively pulsed between accumulation and depletion (Fig. 2, Chapter 2) During that of the accumulation period the interface traps are filled with electrons. When the sample is pulsed into depletion, the capacitance follows the so called "pulsecurve" (or rather a CV curve close to the pulse curve). The pulse curve is a CV curve which is swept so fast that interface states are unable to respond. In the depletion period all traps above the Fermi level will release their electrons by thermal emission. The emission occurs simultaneously from all traps, however , with different time constants (Eqs. 1 and 2). The variation ofcharge in the depletion layer thus leads to a variation of the junction capacitance.

The emission becomes manifest in the transition of the pulse curve in to the normal steady state hf capacitance curve (Fig. 3). It is manifested in the following way. In this method the emission is recorded as a capacitance transient at a fixed bias voltage. When the emission is finished

for the most part, the MOS capacitor is reset to the the initial point in accumulation, and the cycle repeat again.

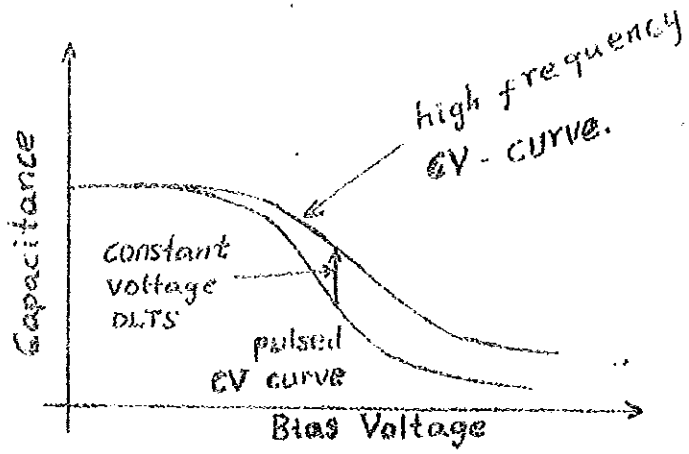


Fig. 2

The emission signal (capacitance transient) consists of a multitude of decaying exponentials, each of them is associated with one of the interface traps. These exponentials can be separated as to time constants by the "rate window technique"[4]. This technique can be implemented in different ways[4]. The approach using a box car averager is the most transparent to illustrate[3,5]:

the capacitance transient is sampled at two pre-assigned time t_1 and t_2 after each start of the depletion period, and the difference signal is formed

$$\Delta C = C(t_1) - C(t_2) \qquad \ldots \quad 3.3.1$$

This signal is termed the DLTS signal or correlation signal. Normalized DLTS signal, S(T) is defined as

$$S(T) = \frac{[C(t_1) - C(t_2)]}{\Delta C(\emptyset)} \quad \ldots \quad 3.3.2$$

where $\Delta C(\emptyset)$ is the capacitance change due to the pulse at $t = \emptyset$. Then for exponential transients we have

$$S(T) = \left[\exp(^{-t}1/\tau) - \exp(^{-t}2/\tau)\right] \quad \ldots \quad 3.3.3$$

temperature dependence of τ is given by

$$\tau = \frac{1}{\sigma \nu N_i} \exp(\frac{\Delta E}{KT}) \quad \ldots \quad 3.3.4$$

$$\Delta E = -(E_C - E_t)$$

The DLTS signal can be written as

$$S(T) = \exp(\frac{-t_1}{\tau})\left[1 - \exp(\frac{-\Delta t}{\tau})\right] \quad \ldots \quad 3.3.5$$

$$\Delta t = t_2 - t_1$$

The relation between rate window τ_{max} (τ_{max} - the value of τ at the maximum of $C(t_1) - C(t_2)$ vs T for a particular trap) and the positions of two gates, t_1 and t_2 is determined by differentiating S(T) w.r.t τ and setting the result equal to zero.

$$\tau_{max} = (t_1 - t_2)\left[\ln(\frac{t_1}{t_2})\right]^{-1} \quad \ldots \quad 3.3.6$$

Thus the emission rate corresponding to the maximum of a trap peak observed in a DLTS thermal scan is precisely defined quantity and may be used along

with the temperature corresponding to the maximum in constructing a semilog activation energy plot. The magnitude of the peak maximum can be related to $\Delta C(\emptyset)$ via Eqs. 3.3.5 and 3.3.6. And it can be used to determine trap concentration. This can be seen from the following relation that

$$\frac{\Delta C}{C} = \frac{\Delta N}{2N} \qquad \text{... 3.3.7}$$

$$N = \frac{\Delta N}{2} \cdot \frac{C}{\Delta C(\emptyset)}$$

(for abrupt semiconductor junction)

where N is trap concentration, ΔC is the capacitance change at $t = \emptyset$ due to a saturating injection pulse, C is capacitance of the MOS under quiescent reverse biased conditions, and ΔN is either the net acceptor or donor on the side of the junction where the traps are observed. On the other hand from Eq. 3.3.4 the trap level can be determined using τ_{max}.

CHAPTER 4

In this chapter sample specifications and apparatus used in our experiment are clearly described. Experimental procedure and techniques used are described, too. Experimental results are presented and their discussion is made.

.1 Sample specification

We did our work on three samples, sample number 6,8 and 12. Samples 6 and 8 were prepared by Solomon Tibebe. See Ref. 19 for their details (originally thery were stated as M-S contact, later they were found to be MOS structure). Sample 12 was prepared by Dr. P.S. Kashinje, a staff member of physics department of University of Dar-es-Salam. According to his information contact is Al(4000Å thick), metal plate - Al (100Å thick) and insulator is indium - Tin - Oxide (Stochiometric specification is not known) with thickness 1200Å, not annealed. Other necessary specifications are given below

Table 2

No	Type	Resistivity (Ωcm)	Orientation	Shape of metal plate (Upper contact
6	Al-SiO_2-pSi	100	<100>	Circular mask
8	Al-SiO_2-pSi	100	<100>	Cross grid
12	Al-InSnO-pSi	100	<100>	Cross grid

.2 Apparatus used

a) HP Model 4275 A Multi-Frequency LCR meter

The HP Model 4275A multi-frequency LCR meter is fully automatic instrument capable to measure various components of a given impedance in a relatively high frequency region. We used it to measure high frequency capacitance of our samples, Measurement can be done at ten different test frequencies selectable from 10kHz upto 10MHz in a 1-2-4-10 sequences. Its test signal level ranges from 1mv to 1v. It has basic accuracy of 0.1%. It can be controlled either using the front buttons or through computer (under remote controle).

b) HP Model 3478A Multi Meter.

HP Model 3478A Multi Meter is capable of dc and ac voltage, current and resistance (both 2 wire - ohms and 4-wire-ohms) measurement. We used it for sample bias measurement. It offers dc voltage performance from 100 nano volt sensitivity upto 300 volt (full scale); true RMS capability up to 300KHz It has basic accuracy of about 0.2% for 3½ digit mode (our working mode). One can communicate using front button or through computer. When under remote control, the 3478A has SRQ (service-request) interrupt capability that lets one to know precisely when the data is ready.

c) HP Model 4140B p^A METER/DC VOLTAGE SOURCE

The HP Model 4140B p^A Meter/DC voltage source comprises a high stability p^A meter with 10^{-15}A (Max) resolution coupled with two programmable DC voltage source. The p^A has a basic accuracy of 0.5% over wide measurement ranges ($\pm 10^{-12}$A ~ $\pm 1.999 \times 10^{-2}$A) One of the two programmable DC voltage source (V_A) can operate not only as programmable DC voltage source, but also as a unique staire case and accurate ramp(⟋, ⟋⎣)generator. It does quasistatic C-V characteristic measurements upto 2nF when the function is set to C-V, using precise ramp (⟋, ⟋⎣) waves. The capacitance value is calculated from the following formula.

$$C = \frac{I \text{ (measured current value)}}{dv/_{dt} \text{ (ramp rate)}} \qquad (4.2.1)$$

Its accuracy depends on the accuracy of I & $\frac{dv}{dt}$

d) HP Model 9000 series 310 computer

HP Model 9000 series 310 computer is used to control all instruments mentioned above. It sends necessary message through HP-IB (interface-bus) to the instrument and the instrument listens to the instruction and talks in response to it. It has memory capacity of 2 mega byts. Diagram of system arrangement interfaced with computer is shown below.

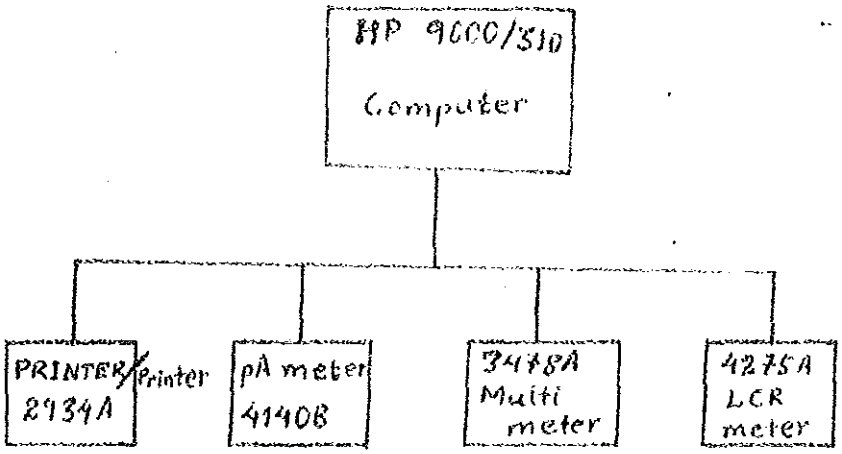


Fig. 1

Programs: The programs for instrument control were written in BASIC 4.03. The description of each program is given in appendix A.

e) Sample holder.

We used locally prepared sample holder. It schematic diagram is shown below

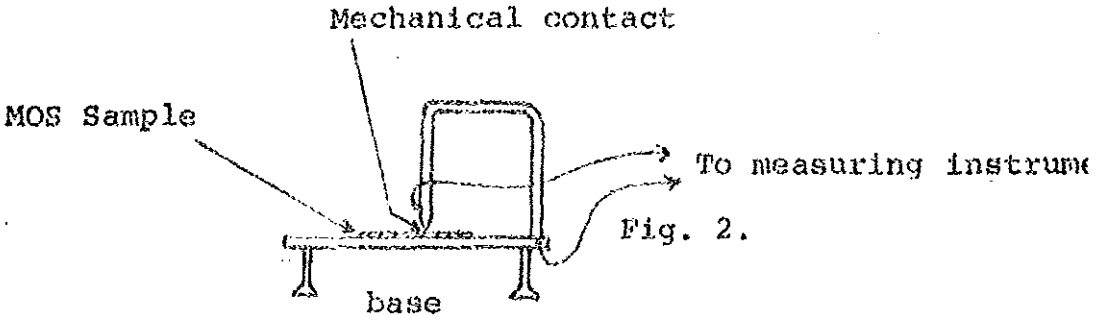


Fig. 2.

Table of residual capacitance of the holder at five different frequencies.

Table 3

Frequencey	Capacitance
10 KH_z	66.60 p^F
20 KH_z	64.04 p^F
200 KH_z	56.86 p^F
1 MH_z	53.05 p^F
4 MH_z	50.43 p^F

Switable contact between the holder and MOS sample was located using reverse bias of -5 volts. In the case there was no contact, capacitance reading was of the order of the value given in the above table.

4.3 Measurement technique used.

We focused our attention mainly on capacitance measurement. High grequency capacitance combined with low frequency capacitance measurement was used in addition to only high frequency capacitance measurement. The measurements were performed at room temperature. We were not able to apply conductance and DLTS measurement technique. For conductance measurement technique we need lower frequency values below 10 KH_z to cover the full dispersion range. For DLTS technique we need liquid nitrogen facility, which regulates the temperature of the sample. But we don't have necessary equipment for it.

.4. Experimental procedure.

Samples with cross grid (6,8) were of large area. It was necessary to break them into pieces to minimize the capacitance. Breaking into pieces was done to obtain capacitance below ∿ 2nF. The capacitance of 2nF is the upper limit of the p^A meter/Dc voltage source. Accordingly, the sample we used in our experiment after breaking into pieces are named 6F, 8a and 12c.

The samples were measured with the help of computer using programs described in Appendix A. The high frequency c-v were measured with in bias range -5v to 5v for all samples. Oxide capacitance was determined using procedure given in section 3.1.1A. The value of oxide capacitance was compared with the corresponding value obtained from the accumulation region(high revers bias). Flat-band voltage shift introduced in section 2.3.1 was determined by comparing with theoretical ideal MOS capacitance value, Eq. 1.3.12. Surface charge density Qss, was determined according to the step a,c,d, e and F as given in section 3.1.1A. From the value of Qss, the density of surface states Nss was found, step g, section 3.1.1A. Energy distribution of density of states Dit,Eq. 3.1.5,was determined by using combined high and low frequency capacitance values. Doping profile, N(w) was determined using equation 3.1.13. For the first four measurements oxide capacitance, flat-band voltage

shift , surface charge density and density of surface state we used a program "Osth-S" see appendix A.

Subprogram for C.V measurement is "Meas-C", subprogram for oxide capacitance determination is "Eval". The flat-band voltage shift, surface charge density and density of states are evaluated in the main program body. Energy distribution of density of states and doping profile are measured using program "DiCth".

4.5 Error analysis

All experimental data are loaded with errors. In our measurement the possible sources of errors are

i) Instrumental errors

ii) Systematic errors

iii) Random errors

i) According to HP company catalogues, the instrumental error for LCR meter is 0.1%, for digital multimeter 0.2% and for p^A meter 0.5%. They are small compared to random errors and they are neglected.

ii) Great care was paid to eliminate the systematic error.

iii) Random error.

Random error is said to be shown when repeated measurements of the same quantity give rise to different values. It requires statistical analysis. The equation we are using for oxide capacitance determination is

Eq. 3.1.11i It is a linear equation and can be written as

$$y = mx + b \qquad (4.5.1)$$

where

$$y = \left(-dc/dv\right)^{\frac{1}{2}}, \quad m \text{ (slope)} = -\left(e/2kTCo\right)^{\frac{1}{2}},$$

$$x = c$$

$$b = Co\ \left(e/2kTCo\right)^{\frac{1}{2}}$$

For this we used straight line fitting (Least squares) |21| i.e. linear regression analysis. We are interested on capacitance obtained from intercept (Coi) and linear relation between y and x. As such error in Coi is the same as standard error in x when y = 0. The standard error is given by the relation |21|

$$\Delta x = \frac{1}{\text{slope}} \sqrt{\frac{\Sigma \left| y_i - (mx_i + b) \right|^2}{n-2}} \sqrt{1 + 1/n + \frac{(y - \bar{y})^2}{\text{slope}^2\ \Sigma (x_i - \bar{x})^2}} \qquad (4.5.2)$$

at $y = \left(-\frac{dc}{dv}\right)^{\frac{1}{2}} = 0$

where n is number of mesurement

$$\text{Confidence interval} = t.\Delta x \qquad (4.5.3)$$

where t is the corresponding value of Student's distribution. Linearity between y and x is checked by evaluating pearson's correlation coefficient r. It is given by the relation |21|

$$r = \frac{\sum_{i}^{n} (x_i - \bar{x})\,(y_i - \bar{y})}{\sqrt{\left(\sum_{i} (x_i - \bar{x})^2 \sum_{i} (y_i - \bar{y})^2\right)}} \qquad (4.5.3)$$

r lies in the range + 1 (perfect direct linear correlation), through zero (no linear correlation), to -1 (perfect inverse linear correlation). From its value one can determine the approximate probability of r occuring by chance.

Oxide capacitance we used for calculation of necessary quantities is the average of oxide capacitance obtained from accumulation region and intercept. Error analysis for capacitance from accumulation region is done assuming Gaussian distribution. Confidence interval is given by the relation [22] ,

$$\text{Confidence interval} = t\,\frac{\sigma}{\sqrt{n}} \qquad (4.5.4)$$

where t is the corresponding value of student distribution, σ standard deviation and n number of reading.

Finally the error in each quantity is analysed using standared relations for errors.

4.6 Experimental result and discussion

Experiment was done on twelve samples. Only two of them show typical MOS high frequency c-v curves (sample 8a and 6F). One of the samples, with InSnO insulator layer (sample 12c) shows a c-v characteristic, similar to typical curves, but with two peaks on it. Description of

the curves and discussion of the result follows:-

Sample 8a

High frequency c-v curve for five different frequencies, under illumination and in the dark measurement are displayed in Fig. 3. From this a curve at 200 KHz which shows to some extent the theoretically expected characteristics is choosen for experimental analysis. Measurement is taken under illumination.

Results

Flat-band voltage shift is V_{BF} = -1.84v

Difference in work functions is ϕ_{ms} =-0.35v

Pearson's correlation coefficient is v = -0.88

Oxide capacitance from intercept, Coi = 3.03E-10F

Considering the confidence interval (95%), we have:

Coi = (3.03 $\pm$ 0.22) E-10 F

Line used in fitting y = -(6.89E+4)C + 2.09E-5

where $y = (-dc/_{dv})^{\frac{1}{2}}$, C is capacitance given in table 4.

Mean oxide capacitance from accumulation region

Col = 2.74E - 10F

Considering the confidence interval (95%)

Cos = (2.74 $\pm$ 0.02) E-10F

Mean oxide capacitance, Co = 2.89E-10F

Considering the confidence interval (95%)

Co = (2.89 $\pm$ 0.11) E-10F

Oxide charge density Qo = 2.35E - 8 $Coul/_{cm^2}$

Illuminated measurement

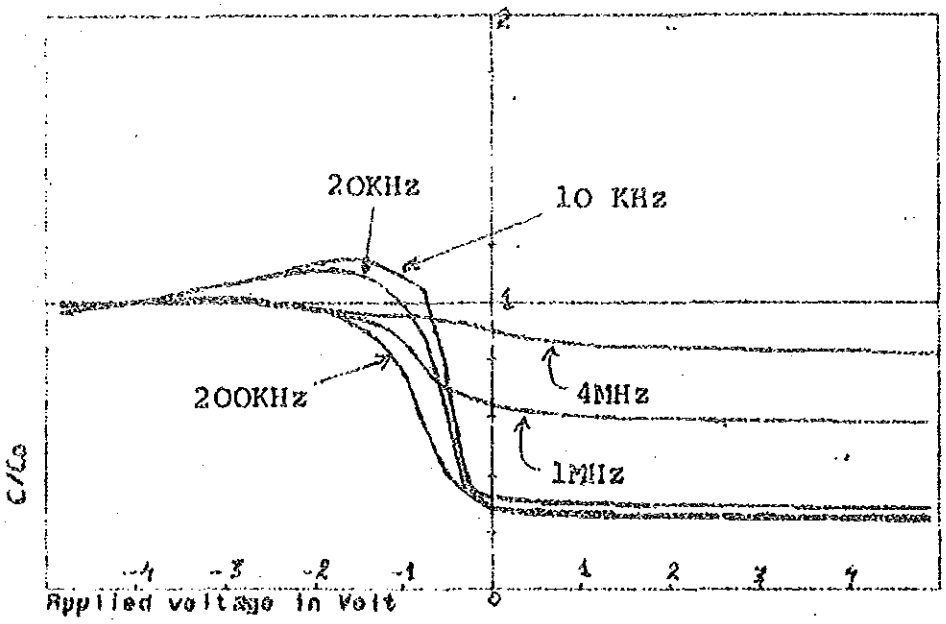


Fig 3a

Dark measurement

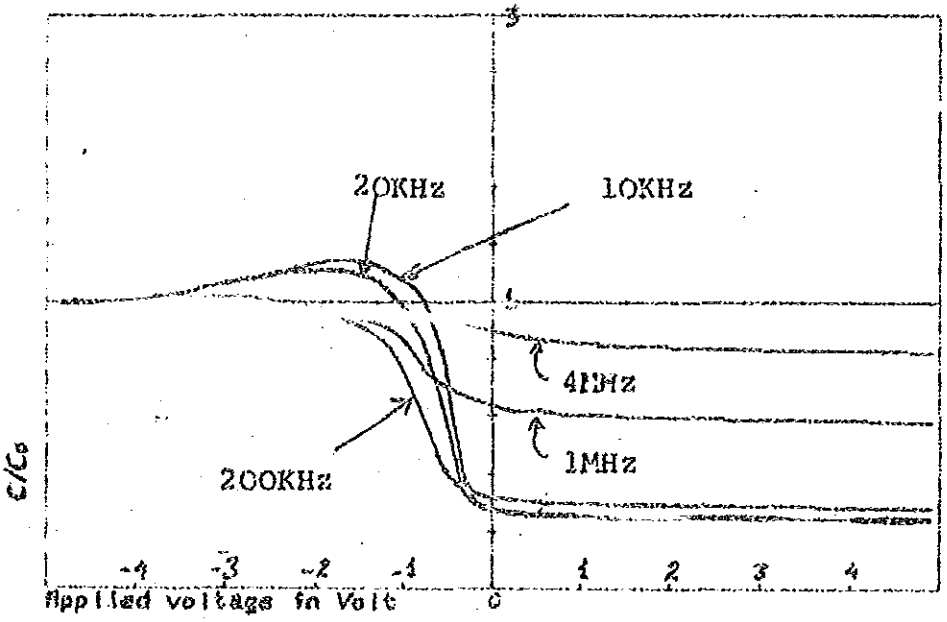


Fig. 3b

Fig. 3

At 200KHz

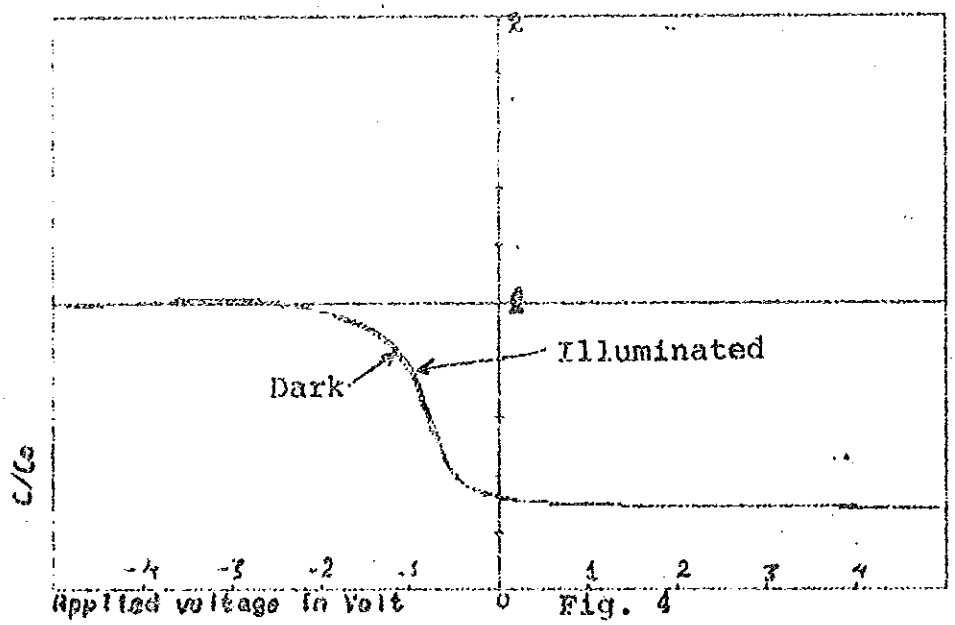


Fig. 4

Table 4

I	Voltage	Capacitance
1	-4.81	2.689E-10
2	-4.52	2.710E-10
3	-4.12	2.739E-10
4	-3.73	2.762E-10
5	-3.34	2.781E-10
6	-2.95	2.787E-10
7	-2.56	2.772E-10
8	-2.17	2.712E-10
9	-1.77	2.566E-10
10	-1.37	2.186E-10
11	-.96	1.442E-10
12	-.58	1.249E-10
13	-.18	1.082E-10
14	.23	9.405E-11
15	.63	8.914E-11
16	1.03	8.653E-11
17	1.43	8.471E-11
18	1.84	8.322E-11
19	2.24	8.198E-11
20	2.64	8.092E-11
21	3.04	7.979E-11
22	3.43	7.893E-11
23	3.84	7.826E-11
24	4.24	7.775E-11
25	4.65	7.728E-11

considering confidence interval (95%),

Q_o = 2.35E - 8 Coul/$6m^2$

Surface charge density, Qss = 1.97E - 8 Coul/cm^2

Considering confidence interval (95%),

Qss = (1.97 $\pm$ 0.22) E-8 Coul/cm^2

Surface state density, Nss = 1.20E + 11 per cm^2

Considering confidence interval (95%),

Nss = (1.20E $\pm$ 0.14) E + 11 per cm^2

Oxide thickness, d = 3.27E-5cm

Considering confidence interval (95%),

D = (3.27 $\pm$ 0.36) E-5cm.

Combined high and low frequency capacitance measurement technique yields density of states as a function of voltage and doping profile. The graph (Fig. 5) and numerical results are given in table 5.

Discussion.

Negative flat-band voltage shift without including effect of work function difference (-2.19v) shows the presence of net positive charge, with in the oxide and with in the interface region explained in section 2.2. We can not compare our result with another data, since we have found no values of Q_o in the literature. The value of Pearson's correlation coefficient (-0.88) shows very good inverse linear correlation, with probability of r occuring by chance less than 0.1% for 20 degree of freedom (we did 22 measurement) |22|

Density of states vs applied bias

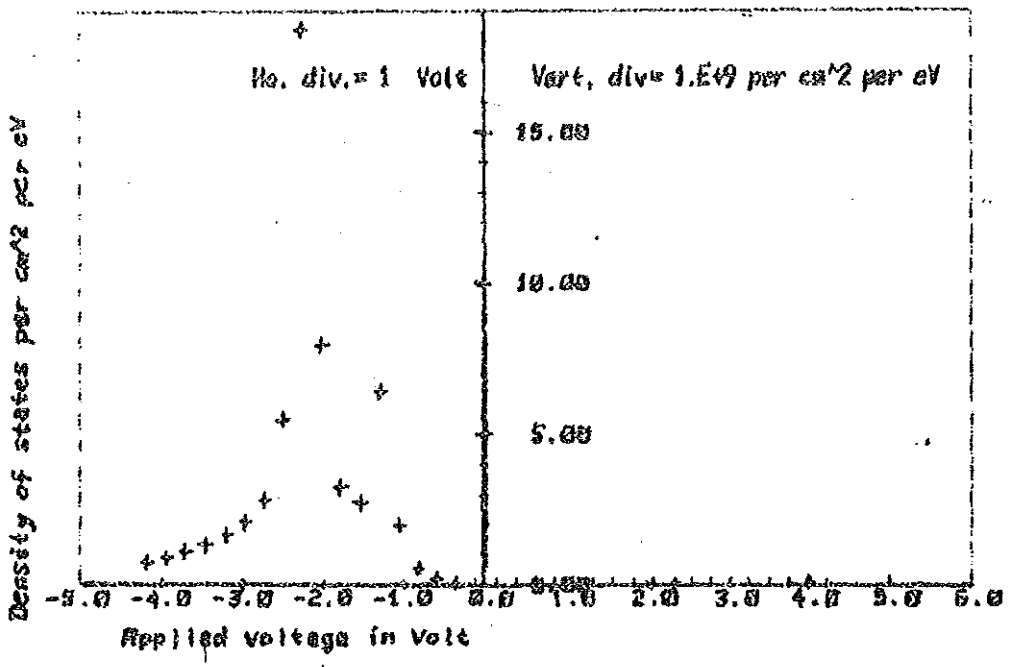


Fig. 5a

Doping profile

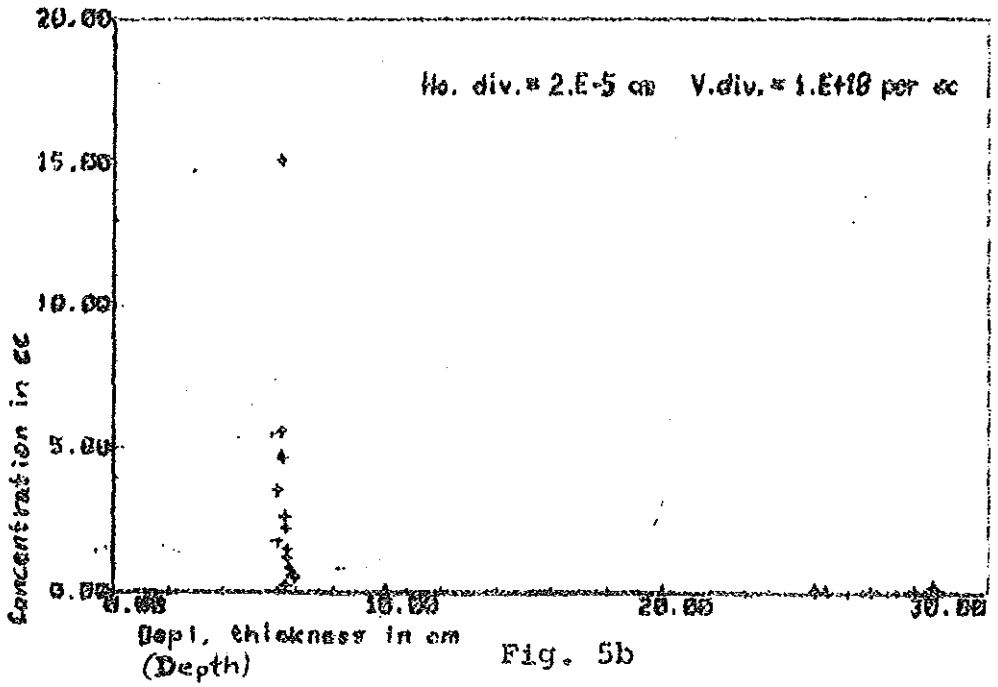


Fig. 5b

Fig. 5

Table 5

I	Voltage	Dens. of stats	concent	Depl.thickness
2	-4.34	9.000E+00	0.000E+00	0.000E+00
3	-4.10	1.299E+09	9.742E+17	6.368E-05
4	-3.86	1.734E+09	1.043E+18	6.299E-05
5	-3.62	2.791E+09	1.469E+18	6.223E-05
6	-3.38	1.004E+10	5.299E+18	6.133E-05
7	-3.14	9.601E+09	4.724E+18	6.058E-05
8	-2.90	2.800E+09	1.603E+18	5.975E-05
9	-2.66	1.906E+09	1.142E+18	5.902E-05
10	-2.42	1.327E+09	9.238E+17	5.837E-05
11	-2.18	1.095E+09	1.223E+18	5.782E-05
12	-1.94	1.023E+09	5.285E+18	5.759E-05
13	-1.70	1.040E+09	1.834E+18	5.765E-05
14	-1.46	1.197E+09	2.249E+18	5.808E-05
15	-1.22	1.208E+09	9.214E+17	5.811E-05
16	-.98	8.564E+08	4.117E+17	5.693E-05
17	-.74	7.430E+08	1.566E+17	5.631E-05
18	-.50	3.179E+10	8.616E+17	6.088E-05
19	-.26	1.495E+08	5.445E+14	8.417E-05
20	-.02	2.296E+07	1.777E+14	2.099E-04
21	.22	1.963E+07	8.624E+14	2.347E-04
22	.46	2.002E+07	4.765E+15	2.314E-04
23	.70	1.922E+07	1.493E+15	2.384E-04
24	.94	1.873E+07	1.646E+15	2.429E-04
25	1.18	1.816E+07	1.823E+15	2.484E-04
26	1.42	1.784E+07	2.771E+15	2.518E-04
27	1.66	1.761E+07	2.463E+15	2.542E-04
28	1.90	1.725E+07	3.429E+15	2.581E-04
29	2.14	1.720E+07	6.205E+15	2.587E-04
30	2.38	1.704E+07	3.105E+15	2.606E-04
31	2.62	1.678E+07	2.433E+15	2.636E-04
32	2.86	1.652E+07	4.272E+15	2.667E-04
33	3.10	1.649E+07	3.914E+15	2.670E-04
34	3.34	1.622E+07	3.481E+15	2.704E-04
35	2.58	1.616E+07	4.111E+15	2.712E-04
36	3.82	1.595E+07	3.726E+15	2.739E-04
37	4.06	1.586E+07	9.104E+15	2.750E-04
38	4.30	1.583E+07	5.214E+15	2.755E-04
39	4.54	1.566E+07	5.303E+15	2.777E-04

Numerical results for surface charge density and surface state density are of the order of 10^{-8} Coul/cm^2 and $10^{11}/cm^2$ respectively. On a clean surface (obtained by cleaving in ultra-high vacuum) the density of surface states was determined by Schockley et.al |6|, who obtained Nss of the order of $10^{15}/cm^2$. Thermal annealing in the presence of hydrogen can decrease this value to $10^{10}/cm^2$ |6|. It indicates that our sample, was annealed.

From the doping profile measurement we can conclude that the surface layer of the semiconductor is highly doped 10^{17} to 10^{18} impurity atoms per cm^3, while in the bulk the impurity concentration is 10^{14} to 10^{15} atoms per cm^3. Comparision with table in | 1 |gives 10^{14} Boron atoms per cm^3 (value corresponding to resistivity 100 Ωcm)

Sample 6F

High frequency c-v curve for five different frequencies under illumination and in the dark measurement are displayed in Fig.6. From this a 20KHz c-v curve (Fig. 7) is choosen for experimental analysis.

Results

Flat-band voltage shift is V_{FB} = 1.03v

Difference in work functions is ϕ_{ms} = -0.35v

Pearson's correlation coefficient is r = -0.64

Oxide capacitance from intercept, Coi = 2.18E-10F

Considering confidence interval (95%)Coi =

(2.18 ± 0.13)E-10F

Illuminated measurement

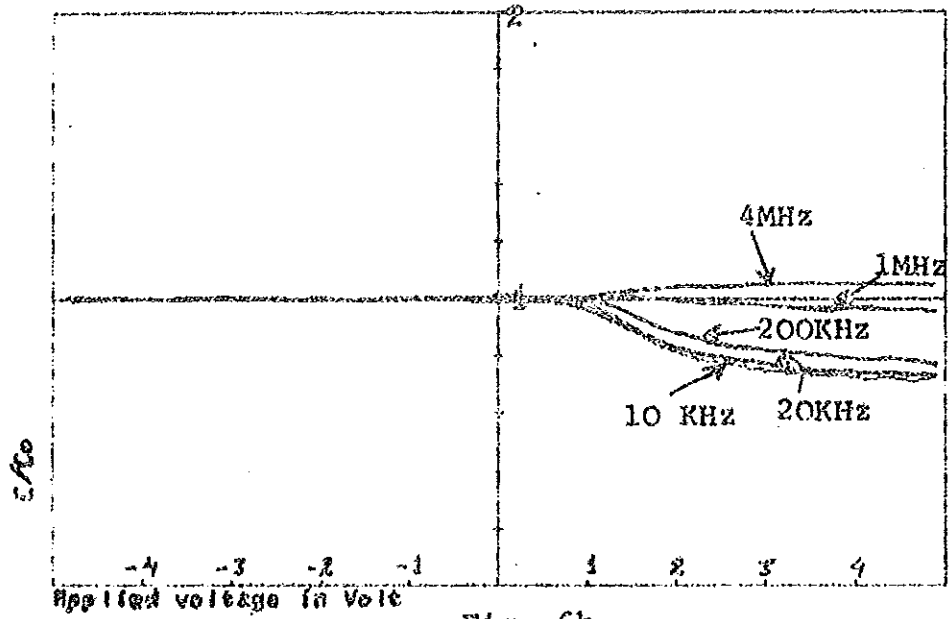


Fig. 6b

Dark measurement

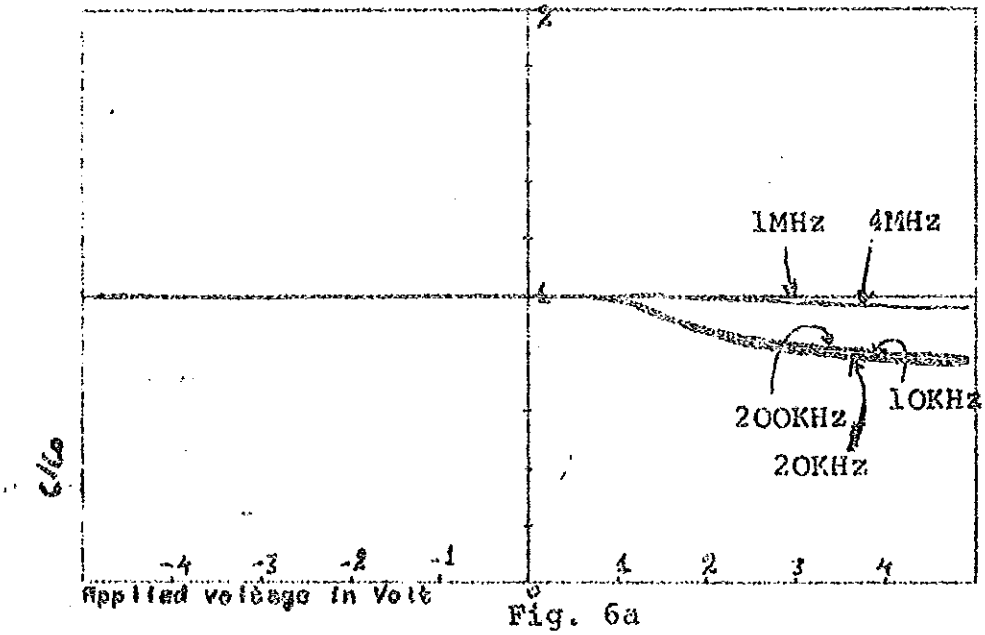


Fig. 6a

Fig. 6

At 20KHz

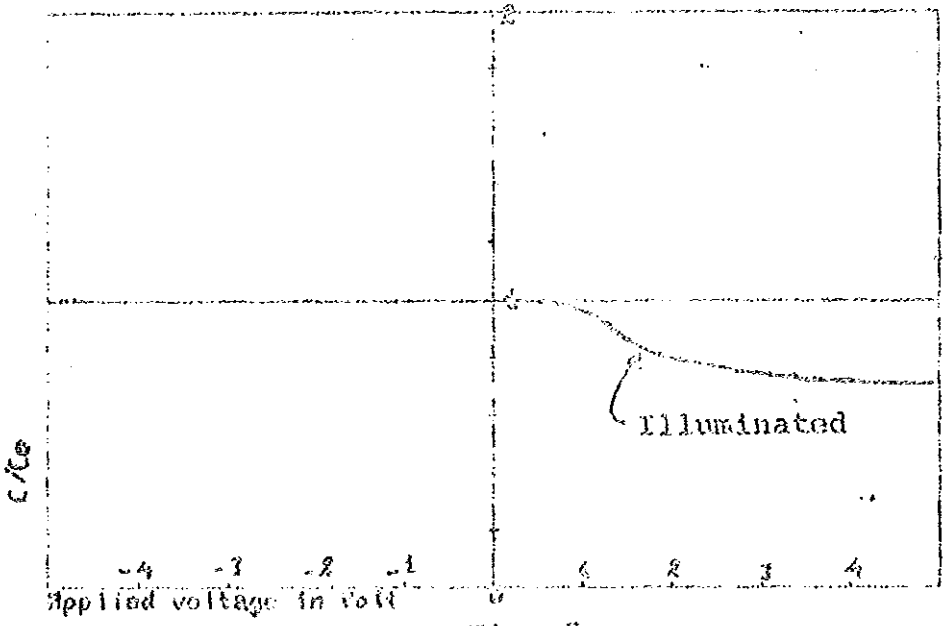


Fig. 7

Table 6

S	Voltage	Capacitance
1	-4.34	2.2[illegible]E-10
2	-4.60	2.[illegible]E-10
3	-4.20	2.2[illegible]E-10
4	-3.80	2.[illegible]E-10
5	-3.39	2.2[illegible]E-10
6	-2.99	2.241E-10
7	-2.60	2.240E-10
8	-2.19	2.[illegible]E-10
9	-1.80	2.[illegible]E-10
10	-1.39	2.[illegible]E-10
11	-.99	2.[illegible]E-10
12	-.59	2.237E-10
13	-.18	2.237E-10
14	.22	2.237E-10
15	.63	2.224E-10
16	1.03	2.151E-10
17	1.43	1.960E-10
18	1.83	1.823E-10
19	2.23	1.[illegible]E-10
20	2.64	1.711E-10
21	3.03	1.674E-10
22	3.43	1.650E-10
23	3.84	1.625E-10
24	4.23	1.611E-10
25	4.62	1.596E-10

Line used in fitting $y = -(3.68E + 5)C + 8.03 - 5$

Where C is capacitance given in table 6.

Mean oxide capacitance from accumulation region

$Col = 2.24E - 10F$

Considering confidence interval (95%), Col =

$Col = (2.23 \pm 0.00)\ E - 10F$

Mean oxide capacitance, $Co = 2.21E - 10F$

Considering confidence interval (95%),

$Co = (2.21 \pm 0.01)\ E-10F$

Oxide charge density $Qo = - 4.25E - 10$ Coul/cm^2

Surface charge density, $Qss = -6.50E-9$ Coul/cm^2

Considering confidence interval (95%),

$Qss = (6.50 \pm 0.18)\ E-9$ Coul/cm^2

Surface state density, $Nss = 4.10E + 10$ per cm^2

Considering confidence interval (95%)

$Nss = (4.10 \pm 0.11)E+10$ per cm^2

Oxide thickness, $d = 5.54E-5$ cm

Considering confidence interval (95%)

$d = (5.54 \pm 0.15)\ E-5$cm

We also tried to apply combined high and low frequency capacitance to this sample but the results were not physically acceptable.

Discussion

Positive flat-band voltage shift without including effect of work function difference (0.68v) shows the presence of net negative charge, with in the oxide and interface region. Again it is not possible to compare

our result with another data, since we have found no values of Qo in the literature. The value of Pearson's correlation coefficient (-0.64) shows fairly good inverse linear correlation with probability of r occuring by chance is between 0.1% and 1% for 20 degree of freedom [21]. Numerical results for surface state density and surface charge density are of the order of 10^{10} and 10^{-9} respectively. The result shows the annealing of the sample.

Sample 12c

High frequency c-v curve for five different frequencies under illumination and dark measurement are displayed from Fig. 8 upto Fig. 12. Capacitance - voltage values for 10KHz and 4MHz under illumination and dark measurement are given in table 7 upto 10.

As one can see, it shows great deviation from theoretical high frequency c-v curve. We have two peaks. One major peak near by accumulation region and the other minor peak in the depletion region. Both doesn't show shift in position. The peak decreases with frequency. We tried to interprete it in the following way.

We were informed that the oxide thickness is 1200Å. No information about dielectric constant is available. We tried to evaluate dielectric constant as follows. From accumulation region capacitance, capacitance of InSnO(insulator),

$$C_i = \frac{\varepsilon_o K_i A}{d} \qquad K_i = \frac{C_i d}{\varepsilon_o A}$$

At 10KHz

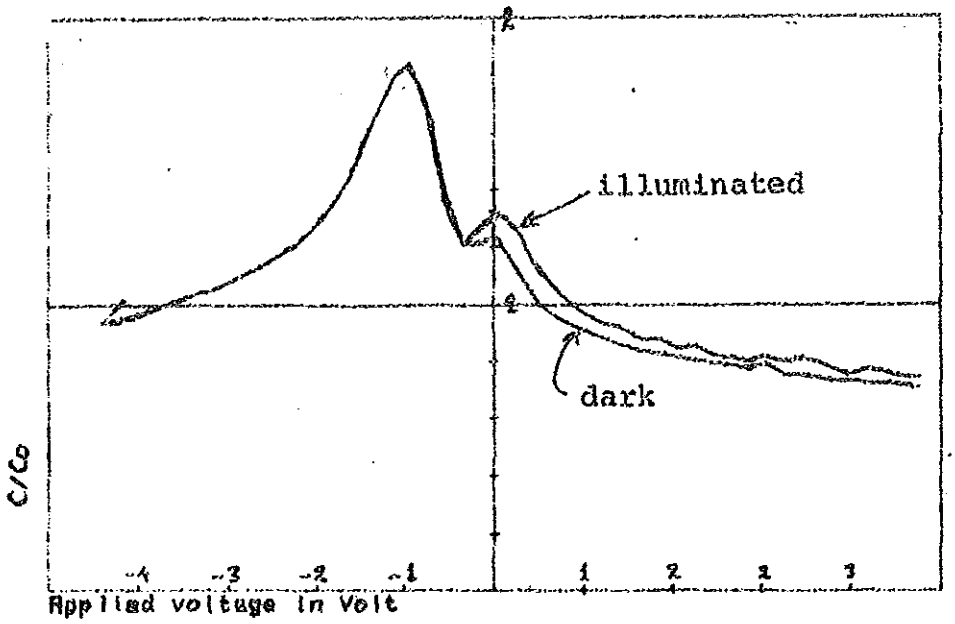


Fig. 8

Ato 20KHz

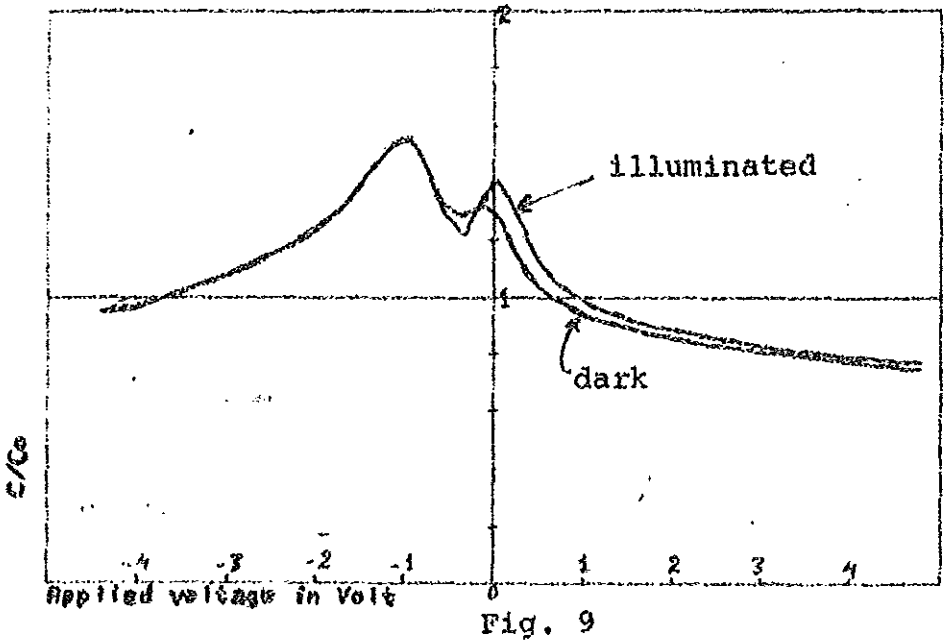


Fig. 9

At 200KHz

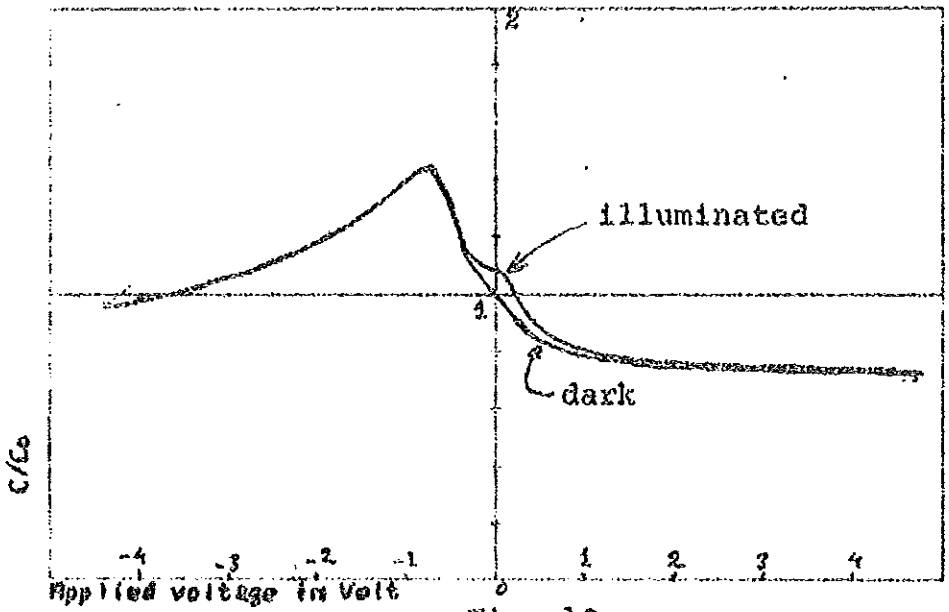


Fig. 10

At 1MHz

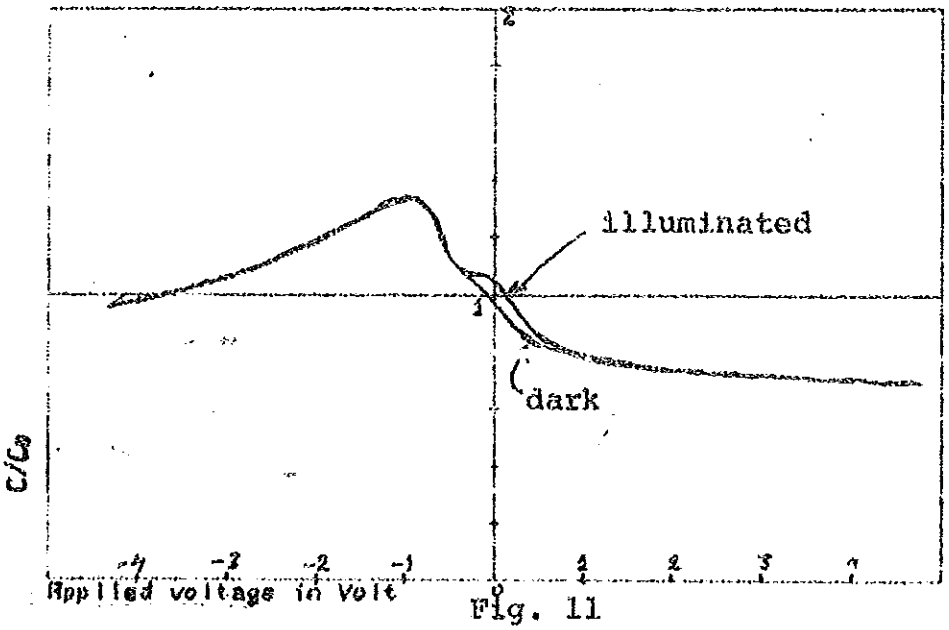


Fig. 11

At 4MHz

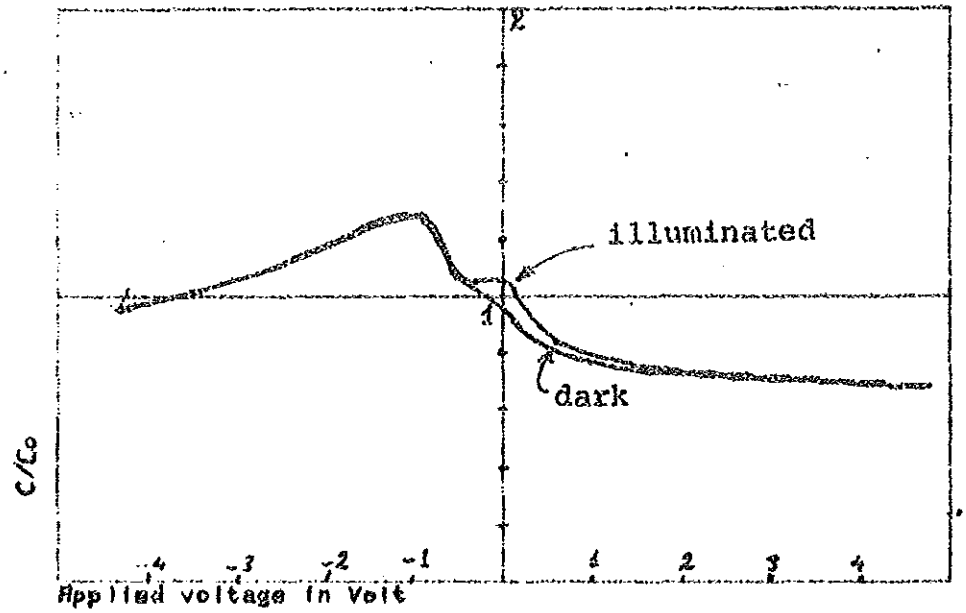


Fig. 12

Table 7. At 10KHz in dark

I	Voltage	Capacitance
1	-4.45	4.038E-10
2	-4.25	4.051E-10
3	-3.89	4.158E-10
4	-3.53	4.312E-10
5	-3.16	4.425E-10
6	-2.80	4.694E-10
7	-2.44	4.985E-10
8	-2.07	5.355E-10
9	-1.70	5.974E-10
10	-1.32	6.934E-10
11	-.95	7.459E-10
12	-.56	5.752E-10
13	-.18	5.191E-10
14	.22	4.776E-10
15	.62	4.115E-10
16	1.02	3.827E-10
17	1.41	3.649E-10
18	1.82	3.514E-10
19	2.21	3.423E-10
20	2.61	3.339E-10
21	2.99	3.268E-10
22	3.36	3.216E-10
23	3.76	3.148E-10
24	4.14	3.095E-10
25	4.53	3.044E-10

Table 8 At 10KHz illuminated

I	Voltage	Capacitance
1	-4.17	4.327E-10
2	-4.25	4.027E-10
3	-3.89	4.117E-10
4	-3.53	4.298E-10
5	-3.16	4.477E-10
6	-2.80	4.702E-10
7	-2.44	4.952E-10
8	-2.07	5.320E-10
9	-1.70	5.916E-10
10	-1.32	6.834E-10
11	-.95	7.310E-10
12	-.57	5.829E-10
13	-.18	5.448E-10
14	.22	5.506E-10
15	.62	4.447E-10
16	1.01	4.114E-10
17	1.41	3.810E-10
18	1.81	3.679E-10
19	2.20	3.535E-10
20	2.60	3.426E-10
21	2.99	3.430E-10
22	3.36	3.479E-10
23	3.75	3.231E-10
24	4.13	3.183E-10
25	4.52	3.207E-10

Table 9 At 4MHz illuminated

I	Voltage	Capacitance
1	-4.43	3.501E-10
2	-4.20	3.482E-10
3	-3.84	3.574E-10
4	-3.49	3.677E-10
5	-3.12	3.795E-10
6	-2.75	3.924E-10
7	-2.40	4.067E-10
8	-2.03	4.228E-10
9	-1.66	4.393E-10
10	-1.29	4.543E-10
11	-.92	4.571E-10
12	-.55	3.849E-10
13	-.17	3.857E-10
14	.23	3.376E-10
15	.68	2.978E-10
16	1.02	2.825E-10
17	1.42	2.743E-10
18	1.81	2.688E-10
19	2.20	2.653E-10
20	2.59	2.623E-10
21	2.99	2.597E-10
22	3.35	2.573E-10
23	3.74	2.547E-10
24	4.12	2.523E-10
25	4.51	2.498E-10

Table 10 At 4MHz in dark

I	Voltage	Capacitance
1	-4.25	3.723E-10
2	-4.20	3.478E-10
3	-3.84	3.571E-10
4	-3.49	3.673E-10
5	-3.12	3.790E-10
6	-2.76	3.918E-10
7	-2.40	4.060E-10
8	-2.03	4.220E-10
9	-1.66	4.383E-10
10	-1.29	4.533E-10
11	-.92	4.559E-10
12	-.55	3.822E-10
13	-.17	3.599E-10
14	.23	3.139E-10
15	.63	2.887E-10
16	1.03	2.771E-10
17	1.42	2.703E-10
18	1.82	2.659E-10
19	2.21	2.627E-10
20	2.60	2.604E-10
21	2.98	2.582E-10
22	3.35	2.559E-10
23	3.74	2.536E-10
24	4.12	2.513E-10
25	4.51	2.488E-10

where ki is dielectric constant of the insulator, d thickness. A crossectional area and ε_0 permitivity of free space. The result obtained is not physically acceptable. If we consider three of them, they are 0.797, 0.806 and 0.816. We also tried to evaluate from maximum peak it was around 1.1 in most measurement.

Remarks: In the accumulation region the capacitance slightly decreases with increase of reverse bias. To obtain its asymtotic value we would have applied high negative bias. It resulted in sample distruction. Our maximum bias was -15.

Discussion:

Possible sources of discrepancy: the maximum measuring error in A is 10% this yields also ki less than 1. What we can say about this is either the thickness or our measurement technique fails for this sample.

The objective of determination of dielectric constant was to calculate surface potential that corresponds to the peaks so as to analyse the traps.

What we can say about left peak is that there may exist parallel capacitance effect across the oxide that contributes to the total capacitance of the structure. It may be due to charges whose generation or recombination is enhanced for voltage bias near by -1v (the peak is around -1v). To explain the phenomenon sufficiently it is necessary to perform further investigation.

CONCLUSION

New experimental techniques to study MOS structure are established in our laboratory. Using the techniques we can determine the following quantities: Flat- band voltage shift, oxide charge density, surface charge density, surface state density, energy distribution of density of states, doping profile and oxide capacitance. The determination of the quantities is based on high frequency and combined high and low frequency c-v measurement.

The experiment found that samples 8a and 6f are MOS structures with oxide layer thickness of 3.27E-5cm and 5.54E-5cm. Numerical value of surface state density determined in sample 8a and 6f ($\sim 10^{11}$ and 10^{10} respectively) indicates that the samples were thermally annealed.

Effect of illumination was detected as a shift of c-v curves in depletion and inversion regions. There was no effect of illumination in accumulation region. And also effect of value of high frequency was observed. This effect has not been quoted in literature.

Sample 12c (with InSnO insulator layer) displayes specific c-v characteristic curves with one major and one minor peaks. The peaks are at a fixed bias values ~ -1v and ~ 0.12v, respectively. These values are independent of frequency. Effect of illumination similar to that of samples 8a and 6f, was observed.

Appendix A

Five main programs are used through out the thesis. Three of them are used for theoretical formula analysis and for demonstration purpose ("Sed_ Sp", "Sp_Ap_V" and "C_V_MOS"). Two of them are used in experiments for the instruments control ("Osth_S" and "DiClh"). A brief discoussion of the programs and subprograms is given below. The programs are written in BASIC 4.03 and have been prepared by ourselves.

Programs for demonstration purpose:

Program "Sed-Sp"

This program computes Space-Charge density as a function of surface potential with varying concentration or temperature. The results can be displayed in the monitor screen or plotted by the printer/plotter. Plotting is done in different colors for different concentration or temperature. Taking Fermi-level as the origin it draws vertical lines corresponding to valence band E_v, conduction band E_c and strong inversion energy (see Fig.5 p.15). Basic function computation is done in subprogram Cig. Main program contains 10 lines and subprogram Cig contains 89 lines, totally the program contains 99 lines.

Program "Sp-Ap-V"

This program computes surface potential as a function of applied voltage. It evaluates applied voltage as a function of surface potential with oxide thickness taken as a parameter. It performs plotting with labeling in different colors for different oxide thickness. Basic function computation and plotting is done in the main program. The program contains 70 lines.

Program "C-V-MOS"

This program computes low frequency capacitance of ideal MOS structure normalized with respect to oxide capacitance versus applied bias in volts. It evaluates applied voltage and MOS capacitance as a function of surface potential (oxide thickness was taken as a parameter). Plotting is done with labelling and different colors for different oxide thickness. All evaluation and plotting is done in the main program. The program contains 70 lines.

Programs for measurement purpose:

Program "Osth-S"

This program makes high frequency C-V

measurement, data analysis and plotting of C-V curve. It is also suitable for experimental location of a convenient contact. The program contains 4 subprograms; Sub Meas-c, Sub Eval and Sub Print.

In the main body of the program we have branching, after taking measured data and C-V plotting. It sets two options, either to print out the evaluated quantity or to go back to new measurement. The main body of the program contains 114 lines. Total number of lines in the program is 387.

Sub Meas-c (collecting data)

This subprogram sets digital multimeter (DMM) and LCR meter in to remote control. It enables selection of bias interval and frequency. After this it sets Data Ready SRQ mask in order to interupt the controller unless the data is ready. Data Ready SRQ part of the program is the following.

```
1460        OUTPUT 723 ; "KM01"     "K" CLEARS THE
                                    SERIAL POLL REGISTER,
                                    "M01" SETS MASK TO 01
```

```
1470 Data1: ON INTR 7 GOTO Data2
1480     ENABLE INTR 7 ; 2        7-HBIB INTERFACE,
                                  2-BIT 1 OF HBIB
                                  INTERUPT ENABLE
                                  REGISTER.
1490     GOTO Data1
1500 Data2: Sp = SPOLL (732)      RETURNS SERIAL POLL
                                  RESPONSE AS S
                                  (NOT USED) CLEARS SRQ
1510     STATUS 7, 4; Aa          RETURNS CONTENT OF
                                  INTERFACE STATUS
                                  REGISTER No. 4 AND
                                  CLEARS IT.
```

Then data is transfered to the computer's memory. After completing measurement, line No. 1580 sets bias zero to avoid sample damage. The subprogram contains 47 lines.

Sub C-V-plot (graph - plotting)

The subprogram selects VIEWPORT, sets WINDOW, scales the AXES and take the avarage of the first ten capacitance reading (capacitance in accumulation region). Then it plots capacitance normalized with respect to the above average versus

applied voltage. Plotting is done with labelling and different color for different measurement. The subprogram contains 40 lines.

Sub Eval (evaluation of some quantities and error analysis).

Transfering the measured capacitance and the corresponding applied bias values the subprogram performs numerical differentiation of capacitance with respect to applied bias. Then it takes the negative square root of it (see Eq. 3.1.11i, p.59). after this, Pearson's correlation coefficient, slope, oxide capacitance from intercept and their standard error is calculated. The subprogram contains 72 lines.

Sub Print (printing of the evaluated quantities and measured data).

The subprogram prints the evaluated quantities and measured data. Printing is done either in the screen or on a paper using PRINTER IS statement. Data is printed according to the format given. The subprogram contains 34 lines.

Program "DiClh"

This program performs combined high and low frequency C-V measurement. It does data evaluationand plotting of the quantities determined from evaluation. The program contains five subprograms; Sub Meas, Sub Eval, Sub Di- plot, Sub Nb - plot and Sub printer. The main body of the program contains 21 lines. Total number of lines in the program is 368.

Sub Meas (collecting data)

The subprogram sets DMM and LCR meter in to remote control. It takes the high frequency C-V measurement in the same way as explained in Sub Meas-c (p.98). After completing high frequency C-V measurement, the subprogram advices for the sample to be connected the special pA meter terminals. Then it sets pA meter in to remote control and to be ready for measurement. It enables selection of bias interval and ramp rate. Then low frequency C-V measurement data is taken. Sub Meas contains 87 lines.

Sub Eval (evalution)

First the metal plate area and oxide capacitance values are INPUTed. Then the subprogram evaluates energy distribution of density of states and doping profile (according to Eqs.3.1.5 and 3.1.12 respectively). Depth is evaluated using the followng relation.

$$X(\text{depth}) = \frac{\epsilon_{ss} A}{C_{h_f}}$$

, A metal plate area

C_{h_f} high frequency capacitance.

Sub Eval consists of 36 lines.

Sub Di- plot (plotting of Dit versus voltage)

The subprogram plots energy distribution of density of states versus applied voltage. Appropriate scaling is done using SELECT ... CASE, which provides conditional execution of one of several program segments. Plotting is done with labeling and cross sign (RPLOT). This subprogram contains 114 lines.

Sub Nb-plot (plotting doping profile)

This subprogram plots doping profile. Plotting is done in the same way as discussed in Sub Di-plot. This subprogram contains 114 lines.

Sub Printer (printing of evaluated values with applied bias).

This subprogram prints applied bias and the evaluated quantities according to the format given. The printing is done either in the screen or on the paper. This subprogram contains 17 lines.

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