



SIMULATION OF FIVE LAYER SOLID-STATE MEMORY CAPACITOR

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Table of Contents

Table of Contents	iv
List of Figures	v
Abstract	vii
1 INTRODUCTION	1
2 MEMCAPACITIVE SYSTEMS	6
2.1 Definition of memcapacitive, memrestive and meminductive systems . . .	6
2.2 Five layer solid-state memcapacitive system	8
2.2.1 Calculation of the memcapacitance	11
2.2.2 Derivation of the memcapacitance from the equivalent circuit model	12
2.2.3 Description of the internal charge dynamics of the system	14
2.2.4 A.C voltage operation of the memcapacitive system	15
3 METHODOLOGY	16
4 RESULTS AND DISCUSSION	18
5 SUMMARY AND CONCLUSION	28
5.1 Summary	28
5.2 Conclusion	29
APPENDIX	30
REFERENCES	33

List of Figures

2.1	The structure of a five layer solid-state memcapacitive system (non-periodic metamaterial system).	9
2.2	The structure of a five layer solid-state memcapacitive system (periodic metamaterial system).	10
2.3	The equivalent circuit model representation of a five layer solid-state memcapacitive system.	12
4.1	Simulation of a five layer memcapacitor. (a) The charge on the internal layers of the non-periodic memcapacitive system and memcapacitor plates as a function of time. (b) Applied voltage on memcapacitor as a function of time. This plot is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$	18
4.2	Simulation of a five layer memcapacitor. (a) The charge on the internal layers of the periodic memcapacitive system and memcapacitor plates as a function of time. (b) Applied voltage on memcapacitor as a function of time. This plot is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$	19
4.3	Simulation of a five layer memcapacitor. (a) The capacitance-voltage plot of the result from simulation (non-periodic) memcapacitive system. (b) The capacitance-voltage plot of the result from simulation (periodic) memcapacitive system. (c) capacitance-voltage plot of the experimental result of ionic memory capacitor [16] plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ and plot (b) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$	21

- 4.4 Simulation of a five layer memcapacitor.(a) The charge-voltage plot of the result from simulation (non-periodic). (b) Polarization-electric field plot of most ferroelectric memories [8]. (c) The charge-voltage plot of the result from simulation (periodic). (d) Polarization-voltage plot of an epitaxially grown $Pb(Zr,Ti)O_3$ ferroelectric memory [15]. plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$, and plot (c) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ 23
- 4.5 Simulation of a five layer memcapacitor.(a) The charge-voltage plot of the result from simulation at different frequencies (non-periodic). (b) The charge-voltage plot of the result from simulation at different frequencies (periodic) (c) Experimental result of the charge-voltage plot for voltage-controlled memcapacitor at different frequencies [16]. plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ and plot (b) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ 25
- 4.6 Simulation of a five layer memcapacitor.(a) Added/removed energy as a function of time (non periodic). (b) Added/removed energy as a function of time (periodic). plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ and plot (b) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ 26

Abstract

In this work we provided the simulation of a five layer charge-controlled memory capacitor in which periodic and non-periodic metamaterials are embedded between the plates of a regular parallel plate capacitor. The simulation result shows hysteretic, negative and diverging in capacitance-voltage behavior and pinched hysteretic charge-voltage properties in both periodic and non-periodic memcapacitive systems. Even though the charge-voltage hysteresis loops of both periodic and non periodic metamaterial memcapacitive systems are pinched, the hysteresis loop of the periodic system is relatively wider than that of the non-periodic and on the average the remnant polarized charge on the periodic memcapacitive system is higher than that of the non-periodic. This property of the periodic metamaterial memcapacitive system makes it a good candidate for non-volatile memory application over the non-periodic one.

Chapter 1

INTRODUCTION

memory devices

A memory material (memdevice for short) is a device used to record (store) information (data), retrieve information, or both [1]. The information stored in a memdevice may be in analog form (continuous range of values) in analog memory materials or in digital form (discrete/discontinuous values) in digital memdevices. Memdevices can be split into two main categories: volatile and non-volatile. Volatile memory loses any data as soon as the system is turned off; it requires constant power to remain viable. On the other hand, non volatile memory doesn't lose its data when the system or device is turned off [2].

History of memdevices

The development of modern computers that make our work so comfortable, easier and faster are intimately associated with the availability of suitable memdevices. Accordingly, the need of more efficient, reliable and compatible memdevices played a critical role on the development of memory technology. In the years (1940's-1950's) cathode ray tubes were used as early analog computer memories with storage capacity of 500-1000 bits of data [3]. However, since cathode ray tube memories have a number of shortcomings, such as low speed, large tube size, etc. they could not go further with the dynamically changing memory technology and were replaced by magnetic core memories in (1950's-1960's) which offered faster operation without the need of a large, expensive tube [3]. Magnetic core memories were capable of storing data bits based on the direction

of magnetic field polarity. The core contained and served until the dawn of semiconductor random access memory (SRAM) in the 1970's [3]. As technology advanced the need for memdevices became essential. Consequently, semiconductor memory materials are now being replaced by modern solid-state memories (ferroelectric, ferromagnetic, magneto resistive, phase change memories) and tomorrow's big future memory elements are believed to be memrestors (resistors with memory), memcapacitors (capacitors with memory) and meminductores (inductors with memory).

How do memory materials work?

The science behind the operation of memdevices is highly associated with the intrinsic properties of the materials from which the memdevices are made of, the architectural design and a number of parameters associated with the internal state of the system. The operation principle of some common memdevices are discussed below.

i) Semiconductor memdevices (SM)

Since the very first days of the mid 1960's when the potential of metal-oxide semiconductor(MOS) technology came in to advance semiconductor memories were realized with superior density and performance [4]. The basic operating principle of semiconductor non-volatile memory is the storage of charge in the gate insulator of a metal-oxide semiconductor field effect transistor (MOSFET). Based on the storage of charge on the gate insulator of a MOSFET non-volatile semiconductor memories can be divided in to floating gate memory and charge-trapping memory. If one can store charge in the insulator of a MOSFET, the threshold voltage of the transistor can be modified to switch between two distinct values conventionally defined as "0" or erased state and the "1" or written (programmed) state [5]. The information content of the device is detected by applying a gate voltage with a value between the two threshold voltages. In one state the transistor is conducting current, while, in the other the transistor is cutoff. When the power supply is interrupted, the charge should, of course remain stored in the gate insulator in order to provide a non volatile device [5].

ii) Magneto-resistive memdevices (MRM)

Each memory cell of a magneto-resistive memdevice is made up of a magnetic tunnel junction (MTJ), which in its simplest form of a metal-insulator-metal (MIM) structure with ferromagnetic electrodes [6]. Its operation principle is based on the tunnelling magneto-resistance (TMR) effect. By applying a small bias voltage between the electrodes a tunnel current can flow, where the tunnel resistance depends on the relative orientation of the magnetization vector of the ferromagnetic electrodes. If the magnetization vectors are parallel the tunnel resistance is small, while if the magnetization vectors are antiparallel the tunnel resistance is large. By exposing the MTJ to external magnetic field a hysteresis loop is formed, with the two stable states of the MTJ which correspond to a "0" or a "1" at zero magnetic field and the information stored in the memory cell is read by determining the tunnelling resistance of the MTJ [6].

iii) Phase change memdevices (PCM)

The PCM material is made from a thin film of chalcogenide alloy which is a glass containing one or more chalcogenide elements (Group 16 in the periodic table e.g. sulfur, selenium or tellurium) as a substantial constituent. This material can reversibly change between an amorphous (high impedance state) which is called the RESET state and a poly crystalline (low impedance state) called SET state. In a phase change memory the PCM material is placed between a top and a bottom electrode with a heating element that extends from the bottom electrode and establishes contact with the PCM, when current is injected between the junction of the material and the heating element it induces a phase change [7]. The basic operation principle is based on the reversible phase conversion between the amorphous and the crystalline state of the chalcogenide glass. Crystallizing the phase change material by heating it above the crystallization temperature (but below the melting temperature) i.e. the SET operation which is controlled by moderate power and long duration of electrical pulses returns the cell to a low impedance state logically stored as "1". Melt-quenching the material i.e. RESET operation makes the material

amorphous and is controlled by high power pulses which places the memory cell in high impedance state logically stored as "0". The data stored in the cell is retrieved by sensing the device resistance by applying very low power [7].

iv) Ferroelectric memdevices (FEM)

Ferroelectric materials are generally defined by reversible spontaneous polarization in the absence of electric field. The spontaneous polarization is generated from noncentrosymmetric arrangement of ions in unit cell which produces an electric dipole moment related to the unit cell. Adjacent unit cells are inclined to polarize in the same direction and form a ferroelectric domain. The ABO_3 perovskite unit cell of a ferroelectric material, where A atoms, B atoms and oxygen atoms occupy the corner site, the body center site, the face center site respectively. When electric field is applied to the ferroelectric material the B atom which has two thermodynamically stable positions inside the oxygen octahedra, is displaced relative to the oxygens upward or downward, depending on the polarity of the electric field. This displacement generates a dipole moment inside the oxygen octahedra, which is called saturation polarization ($\pm P_s$). When the applied field is removed the B atom remains in the displaced position and generates a residual polarization ($\pm P_r$) in the absence of electric field, which forms a hysteresis loop. Therefore the basic operation principle of a ferromagnetic memdevice is its ability to retain two stable states: $+P_r$ or logically "1" state and $-P_r$ or logically "0" state at zero electric field [8].

Since from 1940's when cathode ray tubes were used as early analog computer memories, memdevices have passed through significant progress following the development of memory technology. The memdevices discussed so far in this chapter contributed a great deal for the fabrication of modern high speed computers and other better electronic devices. However, recent experimental and simulation studies have sparked numerous investigations in the area of materials and systems that show history dependence in their current-voltage characteristics (memresistors) which also led to the investigation of memcapacitors and meminductors. Apart from the obvious use of these new emerging devices

in non-volatile memories several applications can be already envisioned for these systems, especially in neuromorphic devices to simulate learning, adaptive and spontaneous behavior. Therefore these memdevices promise new and unexplored functionalities in science and technology both individually and in combination.

Of these potential devices I focus only on memcapacitors particularly on the simulation of solid-state memcapacitor with five layer three dimensional metamaterials embedded as a dielectric between the regular plates of a parallel plate capacitor. The main objectives of this thesis work are :-

1. To show the possible realization of five layer solid-state memcapacitor using periodic and non-periodic metamaterials which have perfect electric conductor (PEC) layers.
2. Investigate which memcapacitive system (periodic or non-periodic) is best applicable for non-volatile memory application.

The rest of the work is summarized as follows. In chapter two the equations governing the general dynamics and the equivalent circuit model of a five layer solid-state periodic and non-periodic metamaterial memcapacitive system is addressed. In chapter three the method of simulation, in chapter four we put the input parameters and the result of the numerical simulation is explained. Finally summary and conclusion is given in chapter five.

Chapter 2

MEMCAPACITIVE SYSTEMS

Non-volatile memory is an essential part of every computer system and most electronic devices to store vital information so that the information will be kept even when the device is not powered [9]. Nowadays ferroelectric, ferromagnetic, shape memory alloys, and semiconductor materials are the building blocks of most of the available non-volatile memory devices. However, recent experimental and simulation studies have sparked numerous investigations in the area of materials and systems that show non-volatile memory effects by exhibiting pinched hysteresis loops (memrestors) which also led to the investigation of memcapacitors and meminductors [10]. These new memdevices (memcapacitors, memrestors, meminductors) offer a non-volatile memory storage within a simple device structure attractive for potential applications in electronics including the field of neuromorphic circuits which mimic the function and operation of a neural cell networks in biological systems [11].

2.1 Definition of memcapacitive, memrestive and meminductive systems

The definitions of memcapacitive, memrestive and meminductive devices (also called circuit elements with memory) are obtained from analyzing a circuit which has four fundamental variables which are charge, current, voltage and magnetic flux. The four different

variables lead to six different couples of variables: charge is related to current and magnetic flux is related to voltage (both by time derivative), current and flux are related by inductance, charge is related to voltage by a capacitor, voltage and current are related by resistance, while magnetic flux and charge are related by memrestor [11]. Quite generally if $\mathbf{x}$ denotes a set of n -state variables describing the internal state of the system $u(t)$ and $y(t)$ are any two complementary constitutive variables (i.e. current, charge, voltage or flux) denoting input and output of the system and g is a generalized response, we can define a general class of memory devices those described by the following relations [15]:

$$y(t) = g(\mathbf{x}, u, t)u(t) \quad (2.1.1)$$

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, u, t) \quad (2.1.2)$$

where $\mathbf{f}$ is a continuous n -dimensional vector function, $\dot{\mathbf{x}}$ is the time derivative of $\mathbf{x}$. We assume on physical grounds that given an initial state $u(t = t_o)$ at time t_o Eqs. (3.1.1) and (3.1.2) admit a unique solution. The generalization of the definition from Eqs. (3.1.1) and (3.1.2) yields port and state equations of current-controlled (CC), voltage-controlled (VC), charge-controlled (QC) and flux-controlled (FC) systems of memresistive, memcapacitive and meminductive natures. According to Eqs. (3.1.1) and (3.1.2) the systems are of n^{th} -order, meaning that $\mathbf{x}$ is a vector containing n -state variables i.e. $\mathbf{x} = [x_1, x_2, \dots, x_n]$ [12]. Here our focus is only on memcapacitive systems. Memcapacitive systems can be divided into two sub groups, namely, voltage-controlled and charge-controlled memcapacitive systems. The type of system control is derived from the subject which controls the time derivative of the system state. In our case the time derivative of the state of a charge-controlled memcapacitive system is derived from the charge accumulated in the memcapacitive port and that of a voltage-controlled memcapacitive system is derived from the voltage developed in the memcapacitive port. Thus, the n^{th} -order charge-controlled memcapacitive system and voltage-controlled memcapacitive system can be defined with

their respective port and state equations. Let the quantities C_M , V , q , and D_M denote memcapacitance, voltage, charge and inverse memcapacitance with units, *Farad*, *volt*, *coulomb* and *Farad*⁻¹, respectively. The n^{th} -order charge-controlled memcapacitive system is defined by the port equation

$$V = D_M(\mathbf{x}, q, t)q(t) \quad (2.1.3)$$

while

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, q, t) \quad (2.1.4)$$

is the state equation. Similarly the n^{th} -order voltage-controlled memcapacitive system is defined by port equation

$$q = C_M(\mathbf{x}, v, t)v(t) \quad (2.1.5)$$

while

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, v, t) \quad (2.1.6)$$

is the state equation [15].

2.2 Five layer solid-state memcapacitive system

Metamaterials can be engineered to provide properties, which may not be readily available in nature, and usually gain their properties from structure rather than composition. The hybrid metamaterial approach in which natural materials are integrated into the metamaterial composite, has been particularly successful in enabling frequency-agile metamaterials that respond to the application of voltage, external electric field, light and heat [13]. An electrically-controlled memory capacitive effect was achieved using a hybrid device composed of a resonant metamaterial (i.e. single layer gold split-ring resonator (SRR) and transition metal oxide (VO_2) [14]. Our five layer memcapacitive system shown in Fig.2.1 consists of five layer metamaterial characterized by long polarization/depolarization time

embedded between the regular plates of a parallel plate capacitor with separation d [14].

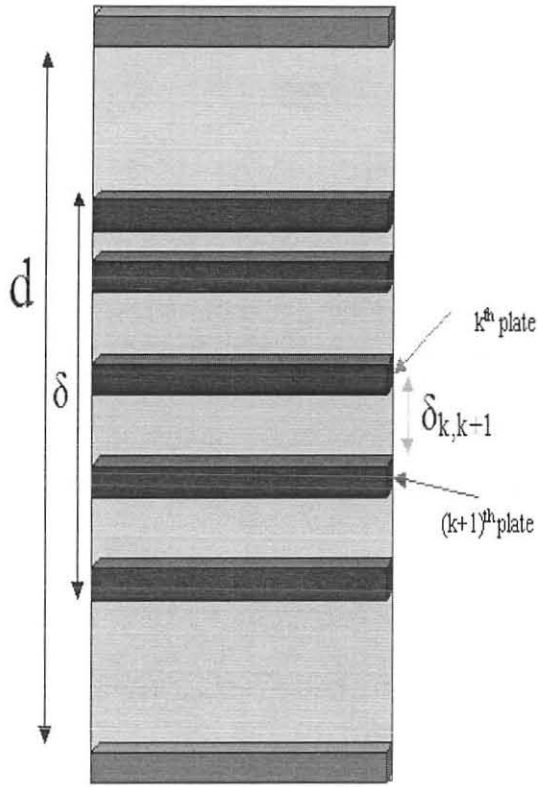


Figure 2.1: The structure of a five layer solid-state memcapacitive system (non-periodic metamaterial system).

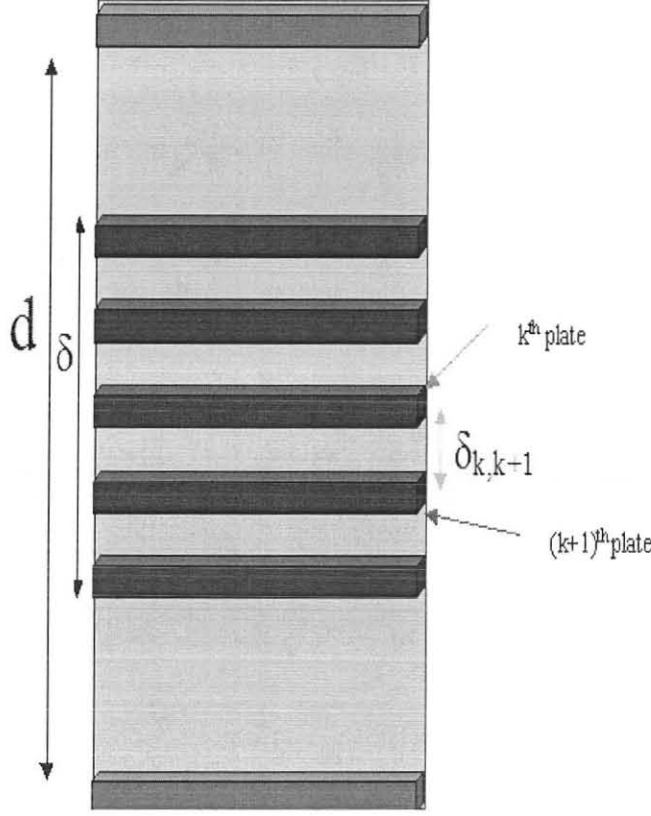


Figure 2.2: The structure of a five layer solid-state memcapacitive system (periodic meta-material system).

The metamaterial is structured from five identical perfect electric conductor (PEC) layers insulated by bakelite plastic and their unit cells have either octahedral (O_h) or pyritohedral (T_h) symmetry point group. In the simulation we assumed that the insulating material is the same as the one of regular capacitor and the memcapacitor is designed in such a way that there is no electron exchange between the external capacitor plates and those embedded (i.e. a higher potential barrier is generated between the external plates and those embedded). The memcapacitive effect of such a system functions if the spacing between the nearest neighboring layers is in the order of a few nanometers and largely based on the slow polarization of the medium between the regular capacitor plates (metamaterial) due to tunneling which is one of the physical mechanism that potentially

provide a slow polarization. As there is a higher potential barrier generated between the external plates and the embedded layers, charge is conserved in the metamaterial. Thus, the total charge in the metamaterial is given by the expression:

$$\sum_{k=1}^5 Q_k = 0. \quad (2.2.1)$$

When external potential difference is applied across the plates of the capacitor, the capacitor will get charged to a charge q . Consequently, the electric field developed by charges on the capacitor causes a charge redistribution among layers of the metamaterial and leads to polarization. The polarized metamaterial develops an internal electric field in opposite direction to the electric field of plate charges. Therefore, for a given amount of plate charge, the internal charge tends to decrease the plate voltage or, equivalently to increase the capacitance. Our simulation is based on calculating the internal charge distribution (internal charge dynamics), its consequent capacitance where the memcapacitor is connected in series with a resistor and an A.C voltage source.

2.2.1 Calculation of the memcapacitance

A charged plate creates a uniform electric field in the direction perpendicular to its plane of a magnitude $E = \frac{\sigma}{2S\epsilon_o\epsilon_r}$ where, $\sigma = \frac{q}{S}$ is charge density in the surface of area S , ϵ_o is the vacuum permittivity and ϵ_r is the relative dielectric constant of the insulating material.

Thus the external plate voltage V_c is given by

$V_c = 2dE_q + \delta E_1 + [\delta - \delta_1]E_2 + [\delta - 2(\delta_1 + \delta_2)]E_3 + [\delta - 2(\delta_1 + \delta_2 + \delta_3)]E_4 - \delta E_5$ where the electric field due to the charge q is $E_q = \frac{q}{2S\epsilon_o\epsilon_r}$ and the electric field at the k^{th} internal plate E_k is $\frac{Q_k}{2S\epsilon_o\epsilon_r}$, Accordingly one can express V_c as

$$V_c = \left(\frac{q}{C_o}\right)\left(1 + \Delta\frac{Q_1}{2q} + (\Delta - 2\Delta_1)\frac{Q_2}{2q}(\Delta - 2(\Delta_1 + \Delta_2 + \Delta_3))\frac{Q_4}{2q} - \Delta\frac{Q_5}{2q}\right) \quad (2.2.2)$$

where $\Delta = \frac{\delta}{d}$, $\Delta_k = \sum_{j=1}^i \frac{\delta_j}{d}$, $i=1, 2, 3$ and δ_j is the spacing between consecutive metal layers. $C_o = \frac{S\epsilon_o\epsilon_r}{d}$ is the capacitance of the system without metal layers.

Therefore, the capacitance of the whole structure (the memory capacitance) is $C = \frac{q}{V_e}$, then the simplified equation is give by;

$$C = \frac{2C_o}{2 + \sum_{k=1}^5 (\frac{Q_k}{q})(\Delta - 2\Delta_{k-1})} \quad (2.2.3)$$

where $\Delta_o = 0$

2.2.2 Derivation of the memcapacitance from the equivalent circuit model

The memcapacitance can also be derived from the equivalent circuit model. In the equivalent circuit model each insulator spacing between adjacent metal layers (including the regular capacitor plates) is represented by a separate capacitor as shown in Fig. 2.3 and to use non-linear resistors to mimic the electron tunneling between the layers and energy loss in the thermalization process accompanying the tunneling. In this model the top and bottom faces of each metal layer are considered as plates of adjacent capacitors while the metallic material of the layer (the region along the height direction) itself plays the role of a conductor connecting these capacitors.

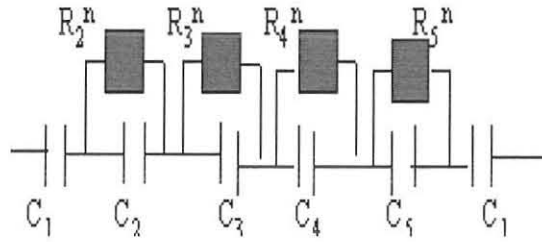


Figure 2.3: The equivalent circuit model representation of a five layer solid-state memcapacitive system.

Thus, the capacitance of each capacitor is calculated by

$$\begin{aligned}
C_1 &= \frac{\varepsilon_o \varepsilon_r S}{\left(\frac{d-\delta}{2}\right)} \\
&= \frac{2C_o}{1-\Delta} \\
C_2 &= \frac{\varepsilon_o \varepsilon_r S}{\delta_1} \\
&= \frac{\varepsilon_o \varepsilon_r S d}{d\delta_1} \\
&= \frac{C_o d}{\delta_1}
\end{aligned}$$

Similarly,

$$C_3 = \frac{\varepsilon_o \varepsilon_r S d}{d\delta_2}$$

$$C_4 = \frac{\varepsilon_o \varepsilon_r S d}{d\delta_3}$$

$$\text{and } C_5 = \frac{\varepsilon_o \varepsilon_r S d}{d\delta_4}$$

Accordingly, the total voltage drop is given by

$$\begin{aligned}
V_c &= \frac{2q}{C_1} + \frac{Q_1 \delta_1}{C_o d} + \frac{Q_2 \delta_2}{C_o d} + \frac{Q_3 \delta_3}{C_o d} + \frac{Q_4 \delta_4}{C_o d} \\
&= \frac{2q}{\frac{2C_o}{1-\Delta}} + \frac{1}{C_o d} \sum_{k=1}^4 Q_k \delta_k \\
&= \frac{q(1-\Delta)}{C_o} + \frac{1}{C_o d} \sum_{k=1}^4 Q_k \delta_k \\
1 &= \frac{q(1-\Delta)}{V_c C_o} + \frac{1}{V_c C_o d} \sum_{k=1}^4 Q_k \delta_k \\
1 &= \frac{C(1-\Delta)}{C_o} + \frac{C}{q C_o d} \sum_{k=1}^4 Q_k \delta_k \\
1 &= \frac{C}{C_o} \left[(1-\Delta) + \frac{1}{d} \sum_{k=1}^4 \frac{Q_k}{q} \delta_k \right]
\end{aligned}$$

$$C = \frac{C_o}{(1-\Delta) + \frac{1}{d} \sum_{k=1}^4 \frac{Q_k}{q} \delta_k} \quad (2.2.4)$$

Note that Eqs. 3.2.3 and 3.2.4 are equivalent. From the two equations of the memcapacitance (Eqs. 3.2.3 and 3.2.4) unlike conventional capacitor, there may be instants of time in which C can be *diverging* when the electric field by the internal layers completely screen the electric field of the plates, despite the presence of finite charge q on the outer plates of the capacitor and also C may be *negative* at another instant of time where the electric field of the internal layers over-screen the external electric field.

2.2.3 Description of the internal charge dynamics of the system

Charge dynamics is essentially determined by the distance between the layers and the potential energy barrier between adjacent layers. The potential difference between the k and $k + 1$ metal layers is defined by $v_k = -E_{k,k+1}\delta_k$ where, $E_{k,k+1}$ is the electric field between two neighboring layers and it is obtained by adding the electric field due to the charges at all layers including the external plates.

$$E_{k,k+1} = -2E_q - E_1 - E_2 \dots - E_k + E_{k+1} + E_{k+2} \dots + E_N$$

$$E_{k,k+1} = \frac{-2q - (Q_1 + Q_2 + \dots Q_k) + (Q_{k+1} + \dots Q_N)}{2S\epsilon_o\epsilon_r} \quad (2.2.5)$$

The dynamics of the charges at a metal layer k is determined by the currents flowing to and from that layer. Thus:

$$\dot{Q}_k = I_{k,k-1} - I_{k,k+1} \quad (2.2.6)$$

where $I_{k,k+1}$ is the tunneling electron current flowing from layer k to layer $k + 1$, by considering the layer charges Q_k as state variables our system is definitely a charge-controlled memcapacitive system described by the following two equations.

$$V = D_M(Q_k, q, t)q(t) \quad (2.2.7)$$

$$\dot{Q}_k = I_{k,k-1} - I_{k,k+1} \quad (2.2.8)$$

where $\dot{Q}_k$ is the time derivative of Q_k . Let $\alpha_1 = \frac{Se}{2\pi h\delta_k^2}$, $\beta_1 = \frac{-4\pi\delta_k\sqrt{2m}}{h}$, $\alpha_2 = \frac{Se^3v_k^2}{4\pi h u\delta_k^2}$, $\beta_2 = \frac{-4\pi\delta_k\sqrt{mu}^{\frac{3}{2}}}{h}$. If u is the potential barrier height between two neighboring metal layers the tunneling current induced by the potential difference V_k between the two can be calculated by

$$I_{k,k+1} = \alpha_1 \left[\left(u - \frac{ev_k}{2}\right) e^{(\beta_1 \sqrt{u - \frac{ev_k}{2}})} - \left(u + \frac{ev_k}{2}\right) e^{(\beta_1 \sqrt{u + \frac{ev_k}{2}})} \right] \quad (2.2.9)$$

if $ev_k < u$ and

$$I_{k,k+1} = \alpha_2 \left[e^{\left(\frac{\beta_2}{ev_k}\right)} - \left(1 + \frac{2ev_k}{u}\right) e^{\frac{\beta_2}{ev_k} \sqrt{1 + \frac{2ev_k}{u}}} \right] \quad (2.2.10)$$

if $ev_k > u$

2.2.4 A.C voltage operation of the memcapacitive system

When a sinusoidal voltage $v(t) = V_o \sin(2\pi ft)$ of amplitude V_o and frequency f is applied to a memcapacitance C connected in series with a resistor R , then the RC circuit is described by

$$v(t) = R \frac{dq}{dt} + \frac{q}{c} \quad (2.2.11)$$

The theoretical backgrounds that define and lead to realization of a five layer solid-state memcapacitor is discussed sofar in this chapter. In addition, we have also derived the memcapacitance using the equivalent circuit model. In chapter three we put the method of simulation that lead to the realization of our system.

Chapter 3

METHODOLOGY

So as to simulate the memcapacitive effect of a five layer periodic and non-periodic memory capacitor we simplified and developed the dynamical equations for a five layer charge-controlled memcapacitor from the quite general model of a circuit with memory described by Eqs.2.1.1 and 2.1.2. After we simplified and developed the dynamical equations for a five layer solid state charge-controlled memory capacitor which are described by Eqs. 2.2.3 or 2.2.4, 2.2.5, 2.2.7, 2.2.8 and 2.2.11 we put the appropriate parameters such as potential energy barrier height and separation between the layers. Then, we developed the mathematica code that solves Eq. 2.2.3 or 2.2.4 together with Eqs. 2.2.5, 2.2.7, 2.2.8 and 2.2.11 and we analyzed, compared and contrasted the result with previously done experimental and simulation studies. The program code is given in the appendix and the input parameters are given below some of the parameters are taken from reference 10.

dielectric constant of the bakelite insulator $\epsilon_r = 5$

Separation between the external capacitor plates $d=100\text{nm}$

Amplitude of the applied A.C voltage, $V_o = 7.5V$

The potential barrier height between two neighboring metal layers, $u = 0.33eV$

Frequency of A.C voltage, $f = 10KHz$

Thickness of the embedded metamaterial, $\delta = 0.5d$

Surface area of each mettall layer of the metamaterial and capacitor plates, $S = 10^{-6}m^2$

Separation between layers:- non-periodic $\delta_1 = 0.05\delta$, $\delta_2 = \delta_3 = \delta_4 = 0.13\delta$ and periodic:-

$$\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$$

$$\text{Electron charge, } e = 1.6 \times 10^{-19}C$$

$$\text{Planck's constant, } h = 6.62 \times 10^{-34}Js$$

$$\text{Mass of electron, } m = 9.1 \times 10^{-31}Kg$$

$$\text{Resistance } R = 1\Omega$$

$$\text{Applied voltage, } V(t) = V_o \sin(2\pi ft)$$

$$\text{Capacitance without metamaterial, } C_o = \frac{S\epsilon_0\epsilon_r}{d}$$

Chapter 4

RESULTS AND DISCUSSION

The detailed theoretical framework and equations that govern the dynamics of a solid-state memcapacitor in general and five layer solid-state memcapacitor in particular is discussed sofar in chapter two. In this chapter the results of the numerical simulation are presented below.

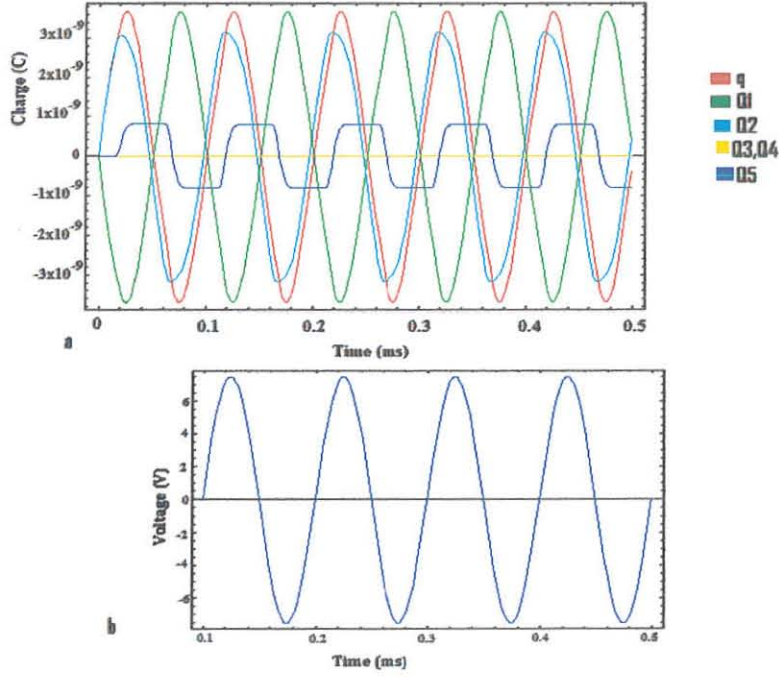


Figure 4.1: Simulation of a five layer memcapacitor. (a) The charge on the internal layers of the non-periodic memcapacitive system and memcapacitor plates as a function of time. (b) Applied voltage on memcapacitor as a function of time. This plot is obtained using the parameter values $\delta_1 = 0.05\delta$, $\delta_2 = \delta_3 = \delta_4 = 0.13\delta$

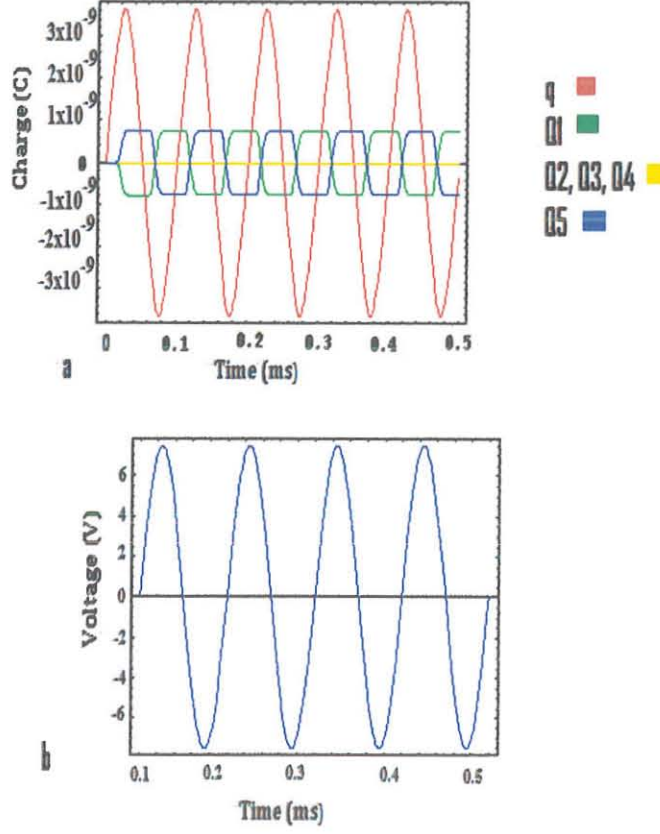


Figure 4.2: Simulation of a five layer memcapacitor. (a) The charge on the internal layers of the periodic memcapacitive system and memcapacitor plates as a function of time. (b) Applied voltage on memcapacitor as a function of time. This plot is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$.

The plots shown in Figs.4.1 and 4.2 represent the numerical simulation result of the charge dynamics of the five layer solid-state memcapacitive system for two different structures which are respectively non-periodic and periodic arrangement of the layers that make up the embedded metamaterial. The time evolution of the internal charge distribution

among the layers of the metamaterial starts when an external voltage in our case (sinusoidal voltage) is applied across the plates of the regular parallel plate capacitor and induces a charge $\pm q$ on the plates. The electric field created by these plate charges will cause electron tunneling between the neighboring metal layers of the metamaterial resulting in a charge redistribution on it. In turn this develops an internal electric field oppositely directed to the electric field of the plate charges. As it is clearly shown from the result in Figs. 4.1 and 4.2 above the time evolution of the internal charge distribution is different for the two structures. For our case we considered a metamaterial with separation between its first and second layers smaller than the separation between the other equally spaced layers as a prototype of memcapacitive system with a non-periodic metamaterial. For this system as shown in Fig. 4.1 starting at zero charge at time $t = 0$ the internal charge dynamics (charge distribution) is accompanied by induction of negative value of Q_1 and positive values of Q_2 and Q_5 . The amplitude of the induced charges on the first and second layer is high compared to the amplitude of the late induced charge Q_5 . This is because the thickness of the tunnel junction between the first and second layer is very small. Concerning the charge on the third and fourth layer it is essentially close to zero. This is explained by tendency of maximum charge separation in such type of devices. In the periodic memcapacitive system as shown in Fig. 4.2 starting at zero charge at time $t = 0$ positive half cycle of $V(t)$ induces negative value of Q_1 and positive value of Q_5 whereas the charge on the second, third, and fourth layer is suppressed nearly to zero values enhancing tendency of maximum charge separation. Neglecting charge transport by any other means such as thermal excitation, the only mechanism in which the layers of the metamaterial show richer charge dynamics is by electron tunneling between the neighboring layers. Starting at zero charge ($Q_k = 0$), when a sinusoidal voltage is applied to the external plates of the capacitor it induces a charge $\pm q$ on the outer plates. The electric field developed by these charges has nearly uniform magnitude in the metamaterial and equally perturb the charges on the surface of each metal layer

composing the metamaterial. Hence for a periodic metamaterial memcapacitive system in which the thickness of the tunnel junction is uniform the tunneling current entering in to and leaving the internal layers of the metamaterial is equal as a result of inelastic co tunneling. Consequently, unlike a non periodic metamaterial memcapacitive system the net charge in all of the internal metal layers is nearly zero or zero and finite on the outer layers of the metamaterial.

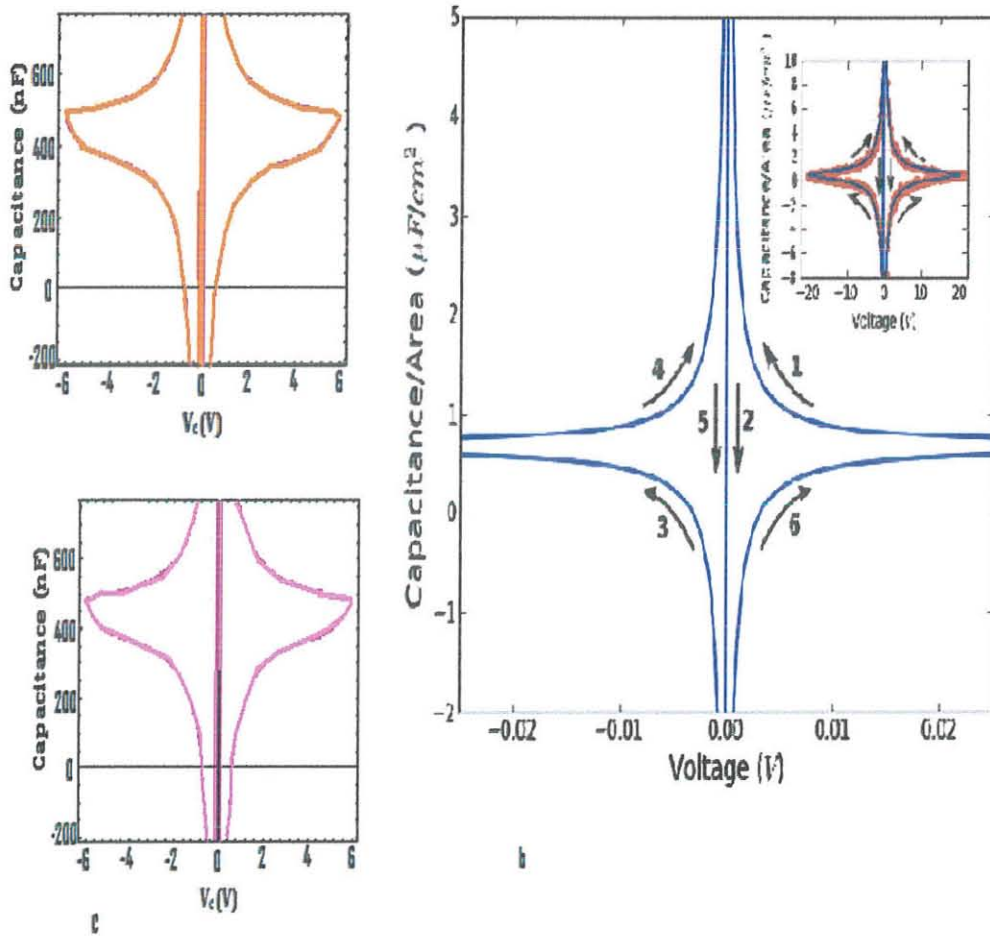


Figure 4.3: Simulation of a five layer memcapacitor. (a) The capacitance-voltage plot of the result from simulation (non-periodic) memcapacitive system. (b) The capacitance-voltage plot of the result from simulation (periodic) memcapacitive system. (c) capacitance-voltage plot of the experimental result of ionic memory capacitor [16] plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ and plot (b) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$

Fig. 4.3 shows the capacitance-voltage behavior of our non-periodic and periodic memcapacitive system respectively. From a microscopic point of view a change in capacitance occurs in two ways [11]; i) Due to a geometrical change of the system (e.g. a variation in its structure), or in ii) quantum mechanical properties of the system (carriers and bound charges of the system composing the capacitor e.g. a history dependent permittivity ε) or both. Our memcapacitive system gains its properties from its structural architecture in turn which brought its quantum mechanical properties. In both periodic and non-periodic metamaterial memcapacitive systems the capacitance-voltage plot shows both diverging and hysteretic behavior which are compatible with experimental results as shown in Fig.(4.3) and this is a quite important and unique characteristic of capacitors used for non-volatile memory application. This property arises from the fact that there may be instants of time in which the electric field created by the polarization of the metamaterial completely screens the electric field by the external plates, despite the presence of a finite charge on the external capacitor plates. At another instant of time the internal electric field may over-screen the electric field of the plate charges which results in a negative capacitance. Hence from our simulation result, our memcapacitive system made from periodic and non-periodic metamaterial is definitely a memory capacitor by ref [16].

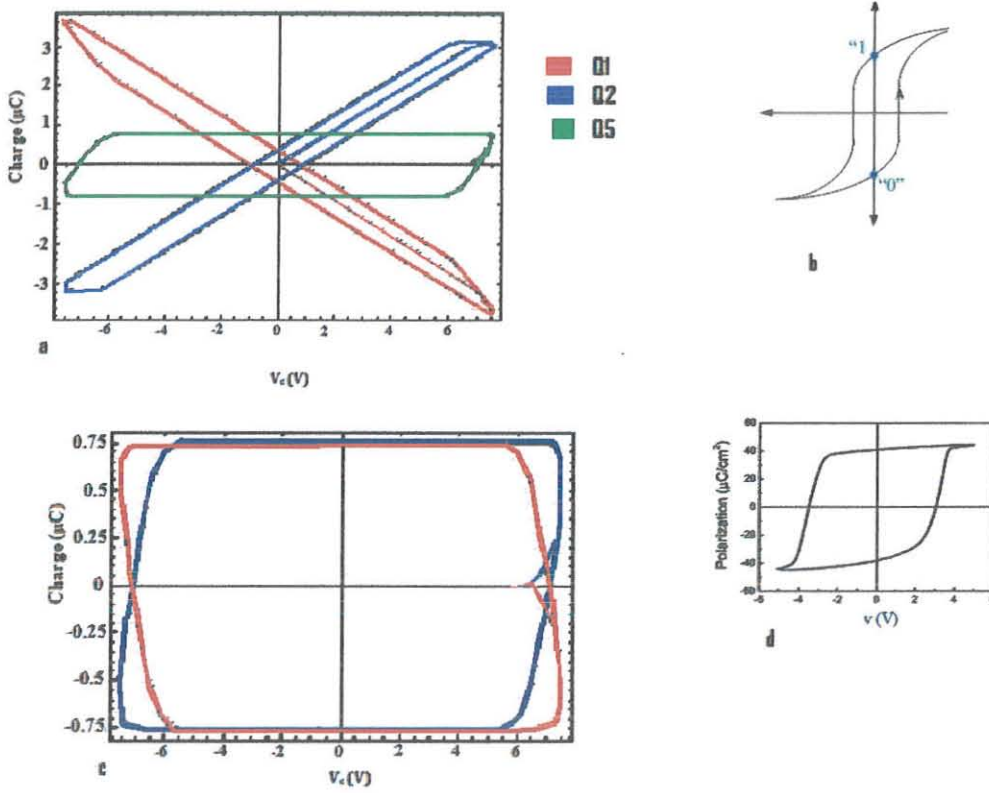


Figure 4.4: Simulation of a five layer memcapacitor. (a) The charge-voltage plot of the result from simulation (non-periodic). (b) Polarization-electric field plot of most ferroelectric memories [8]. (c) The charge-voltage plot of the result from simulation (periodic). (d) Polarization-voltage plot of an epitaxially grown $Pb(Zr, Ti)O_3$ ferroelectric memory [15]. plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta$, $\delta_2 = \delta_3 = \delta_4 = 0.13\delta$, and plot (c) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$

Hysteresis is the main characteristic of systems that have memory, where the effect of the input (stimulus) to the system are experienced with a certain delay in time. In our case as shown the charge in the metamaterial Q_5 in Fig. 4.1 and Q_1 and Q_5 in Fig 4.2 is zero until some finite value of the applied voltage, thus the effects of the input are delayed by some time behind the sinusoidal input and cause slow polarization as expected. In both periodic and non-periodic memcapacitive systems when an internal polarization is present, this polarization can create a non zero voltage drop on the memcapacitive system even at zero plate charge q . On the other hand when the internal electric field

completely screens the electric field of the plates we can get zero voltage drop on the memcapacitive system, despite the charge on the external plates is non zero. This is the reason why the charge-voltage hysteresis loop is non-pinched which is a quite usual behavior of most memdevices. Even though the hysteresis loops of both periodic and non-periodic systems are similar (i.e. non-pinched) their shape is different. The hysteresis loop of the non-periodic system is narrow which is on the average characterized by a relatively low retentivity, coercivity and remnant polarization. This hysteresis loop is similar to the hysteresis loop of most ferroelectric memdevice as shown in Fig (4.4)b [8]. The hysteresis loop of the periodic memcapacitive system is wide and nearly rectangular which is characterized by a relatively higher retentivity, coercivity, remnant polarization and constant threshold operation voltage. This hysteresis loop is similar to the hysteresis loop of an epitaxially grown $Pb(Zr,Ti)O_3$ ferroelectric memory as shown in Fig (4.4)d [15]. From this difference in hysteresis loop properties of the periodic and non-periodic memcapacitive system it is possible to indicate that the periodic memcapacitive system is more recommended for a non-volatile memdevice than the non-periodic one. From the above Figs.(4.4)a and c we have calculated also the following parameters for non-periodic and periodic memcapacitive systems. Average area of the hysteresis loop (work done by the voltage source in polarizing the medium) (non-periodic)=24.46J and 20.25J (periodic), average remnant polarization charge= $0.52\mu C$ (non-periodic) and $0.75\mu C$ (periodic) and the average depolarization voltage is -2.67V for the non periodic and -7V for the periodic one.

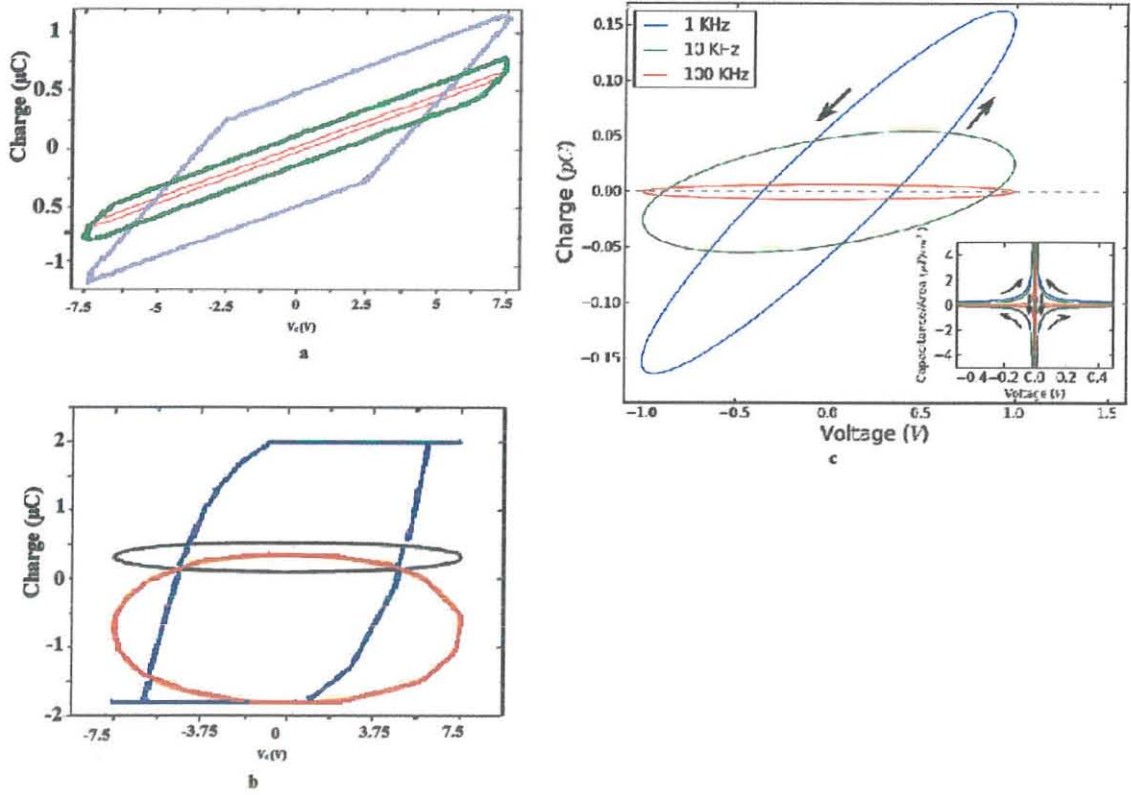


Figure 4.5: Simulation of a five layer memcapacitor. (a) The charge-voltage plot of the result from simulation at different frequencies (non-periodic). (b) The charge-voltage plot of the result from simulation at different frequencies (periodic) (c) Experimental result of the charge-voltage plot for voltage-controlled memcapacitor at different frequencies [16]. plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ and plot (b) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$

Finally it is worth pointing out that the simulation result of the charge-voltage hysteresis loop of our system (both periodic and non-periodic) shrinks at higher frequencies, which is in a good agreement with experimental results as shown in Fig. (4.5) [16]. This is because at higher frequencies in which the A.C voltage quickly changing its polarity does not considerably change the internal charge distribution so that the system has not enough time to remember its past states as it is governed by slow polarization time. This is a quite important feature of memdevices because of the fact that the internal degrees of freedom of a memory device have not enough time to respond to the external perturbation.

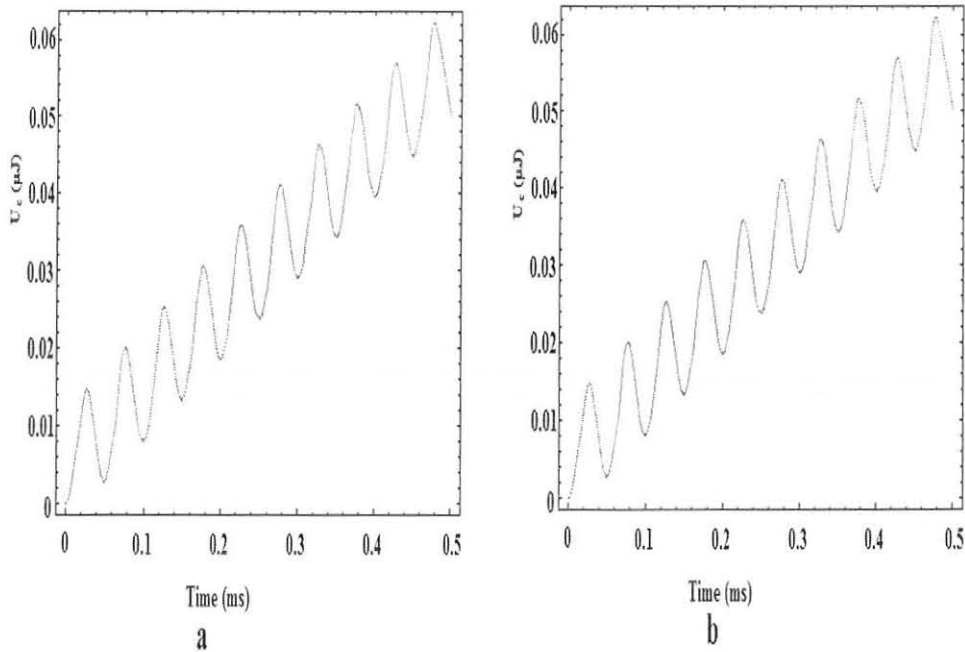


Figure 4.6: Simulation of a five layer memcapacitor.(a) Added/removed energy as a function of time (non periodic). (b) Added/removed energy as a function of time (periodic). plot (a) is obtained using the parameter values $\delta_1 = 0.05\delta, \delta_2 = \delta_3 = \delta_4 = 0.13\delta$ and plot (b) is obtained using the parameter values $\delta_1 = \delta_2 = \delta_3 = \delta_4 = 0.13\delta$

It is already addressed that change in capacitance can occur in two ways. In either case, inelastic (dissipative) effects may be involved in changing the capacitance of the system upon application of the external control parameter. These dissipative processes releases energy in the form of heating of the material composing the capacitor. On the other hand there may be situations in which energy not from the control parameter but from sources that control the equation of motion for the state variables, is needed to vary the capacitance of the system (e.g. in the form of elastic energy, or via a power source, say, the permittivity of the system via a polarization field). This energy will then be released in the circuit, thus amplifying the current. Therefore memcapacitive systems could, in principle, describe both dissipative and passive devices.

The energy added to or removed from a memcapacitive system is defined as:

$$U_c = \int_0^t V_c(\tau) I(\tau) d\tau \quad (4.0.1)$$

A memcapacitive system is said to be passive if $U_c = 0$ and dissipative if $U_c > 0$. From Fig. 4.9 it is clear that our memcapacitive system is dissipative in both periodic and non-periodic case since $U_c > 0$. This is due to the fact that electron tunneling between internal layers is accompanied by energy dissipated in thermalization process due to the different electrochemical potential energies of metal layers in addition to local heating which is not avoidable in real systems.

The application of a five layer memcapacitor for non-volatile memory device is discussed so far, however, for realizing the system under consideration, reading its state is the most important question that should be answered. The memcapacitor state is read by a single voltage pulse [10]. Small amplitude or short voltage pulses are not suitable for reading the memcapacitor state because they do not change the charge distribution on the internal layers of the metamaterial. Consequently, the measured value of the capacitance, using small amplitude or short pulses would always be equal to the capacitance in the absence of metamaterial. Hence, in order to read the memcapacitive state the applied single voltage pulse should have large enough amplitude and should be sufficiently long.

Chapter 5

SUMMARY AND CONCLUSION

5.1 Summary

Since 1940's when cathode ray tubes were used as early analog memories, memdevices passed through significant improvements following the development of memory technology. Modern efficient, compatible ferroelectric, ferromagnetic, shape memory and semiconductor memdevices played their own role for the fabrication of high speed computers. However recent experimental and simulation studies have sparked new investigations in the area of materials and systems that show non-volatile memory effects. These are memrestors, memcapacitors and meminductors. These circuit elements which can store information with out the need of a power source would represent a paradigm change in electronics, allowing for low power computation and storage. In addition if that information spans a continuous range of values analog computation may replace the present digital one. Such a concept is also likely to be at the origin of the working of the human brain and possibly of any other mechanisms in living organisms so that such circuit elements may help us understand adaptive and spontaneous behavior, or even learning.

Of these potential memdevices we suggested the possible realization of a five layer charge-controlled solid-state memcapacitor in an easy way of fabrication in which periodic and non-periodic metamaterials are embedded between the regular plates of a parallel plate capacitor. The functioning of this device is based on slow polarization of the medium

due to electron transfer between neighboring metal layers of the metamaterial across the insulating tunnel junction via tunnelling. Unlike conventional capacitors the capacitance of this device is memory-dependent (i.e it depends on the state and history of the system). The capacitance diverges in the limit of zero voltage and acquires negative values within a certain voltage range. In addition this device shows pinched hysteresis loop in the two constitutive variables that define it (i.e. charge-voltage). Moreover the hysteresis loop of this memcapacitor shrinks at higher frequencies which is a quite usual feature of memory devices.

5.2 Conclusion

From the result of our numerical simulation, we have shown the possible realization of a five layer memory capacitor by embedding metal layers arranged periodically and non-periodically where the metals are separated by an insulator. even though the hysteresis loops of both the non-periodic and periodic memcapacitive system are similar in that they are pinched their shape is different. The hysteresis loop of the periodic metamaterial memcapacitive system is wider than that of the non-periodic and nearly rectangular in shape that makes the system under consideration a good candidate for non-volatile memory application over the non-periodic one. In addition to this obvious non-volatile memory application, memcapacitors in general open up new and unexplored functionalities in electronics and I believe that the time is ripe for new and exciting innovations in electronics. I hope this work will motivate people to do more experimental and theoretical investigations on solid-state memcapacitors.

APPENDIX

The simulation mathematica code is given below

PARAMETERS

$$\epsilon_r = 5;$$

$$\epsilon = \epsilon_r(8.85 \times 10^{-12});$$

$$d = 100nm;$$

$$S = 1 \times 10^{-6}m^2;$$

$$c_o = S\epsilon/d$$

$$\Delta = 0.5;$$

$$\delta = \Delta d$$

$$V[t] = 7.5 \sin 2\pi f t$$

$$f = 10KHz$$

$$R = 1\Omega$$

$$e = 1.6 \times 10^{-19}C$$

$$h = 6.6 \times 10^{-34}Js$$

$$m = 9 \times 10^{-31}Kg;$$

$$U = 0.33eV$$

$$T = 5/f;$$

$$n = 5;$$

=====:

(*[VARIABLES, TIMES ...]*)

```

Table[δδ[k] = 1, k, 1, n - 1];
δδ[1] = 0.05;
total = ∑l=1n-1 δδ[1]
Table=[Rδ[k] =  $\frac{\delta\delta[k]}{total}$ , [k, 1, n - 1]
Table=(*[Rδ[k] =  $\frac{1}{n-1}$ , [k, 1, n - 1]*)
Λ[0] = 0;
TableΛ[k]= δ ∑l=1k Rδ[1], (k, 1, n - 1)];
variables=[Table[q[t], Q[k, t], (k, n)]]
[Voltage[k] =  $\frac{\Delta R\delta[k]}{2c_o}(2q[t] + \sum_{m=1}^k Q[m, t] - \sum_{m=k+1}^n Q[m, t]), (k, 1, n - 1)];$ 
i[0, t] = 0;
i[n, t]= 0;
j1[k, v]= $\frac{eS}{2\pi h\delta^2 R\delta[k]^2} ((V_o - \frac{ev}{2})Exp[-\frac{4\pi\sqrt{2m}\delta R\delta[k]}{h}\sqrt{V_o - \frac{ev}{2}}] - (U - \frac{ev}{2})Exp[-\frac{4\pi\sqrt{2m}\delta R\delta[k]}{h}\sqrt{U + \frac{ev}{2}}])$ 
j2[k, v]= $\frac{Se^3 v[v]}{4\pi h U \delta^2 R\delta[k]^2} (Exp[-\frac{4\pi\sqrt{m}\delta R\delta[k]U^{\frac{3}{2}}}{he[v]}) - (1 + \frac{2e[v]}{U})Exp[-\frac{4\pi\sqrt{m}\delta R\delta[k]U^{\frac{3}{2}}}{he[v]}}(1 + \frac{2e[v]}{U})]$ 
ii[k, v]= UnitStape[v](j1[k, v](1 - UnitStape[v - U/e]) + j2[k, v]UnitStape[v - U/e]
+j2[k, v](1 - UnitStape[v + U/e]))
Table[i[k, t] = ii[k, Voltage[k]], (k, 1, n - 1)];

=====

(*DYNAMICAL SYSTEM (CHARGES AND CAPACITANCE)*)
DEquation = [q'[t]==  $\frac{V[t]}{R} - \frac{\sum_{k=1}^n (\Delta - 2\Lambda[k-1])Q[k, t] + 2q[t]}{2RC_o}$ ], q(0) == 10-20,
Table[(D[Q[m, t], t] == -i[m, t] + i[m - 1, t], Q[m, 0] == 0), (m, n)], Simplify;
qq = NDSolve[DEquation, variables, (t, 0, T), MaxSteps → 20000];
Plot[Evaluate[[variables, 10-12V[t]]/.qq], (t, 0, T), PlotRange → All]
(*TotalQ = ∑k=1n Q[k, t];
plot[Evaluate[TotalQ/.qq], (t, 0, T)]*)
C =  $\frac{2C_0}{2 + \sum_{k=1}^n (\Delta - 2\Lambda[k-1])\frac{Q[k, t]}{q[t]}}$ ;
(*Plot[Evaluate[(c, 10-10V[t])/.qq], (t, 0, T), PlotRange → {(-5x10-9, 5x109)}, PlotStyle →
Thick]*)

```

(*Plot[Evaluate[(Q[1, t] + Q[2, t] + Q[3, t] + Q[4, t] + Q[5, t])/.qq], (t, 0, T)]*)

=====

(*PHASE DIAGRAMS*)

$$V_C = \frac{q[t]}{C};$$

ParametricPlot[Evaluate[(VC, 10⁸c)/.qq], (t, 1/f, T), PlotRange → (All, (-15, 15)),

PlotStyle → Thick]

(*Show[Table[ParametricPlot[Evaluate[(VC, 10⁹Q[i, t])/.qq], (t, 0, T), PlotRange →
(All, All)], {i, 1, n}]]*)

$$Current = \frac{V[t]}{R} - \frac{\sum_{k=1}^n (\Delta - 2\Lambda[k-1])Q[k, t] + 2q[t]}{2RC_o},$$

Plot[Evaluate[Current/.qq], (t, 0, T), PlotRange → All]

(*ParametricPlot[Evaluate[(VC, 10⁸Current)/.qq], (t, 0, T), PlotRange → (All, (-20, 20))]*)

ParametricPlot[Evaluate[(VC, 10¹¹q[t])/.qq], (t, 1/f, T), PlotRange → (All, All), PlotStyle →
Thick]

(*Plot[NIntegrate[Evaluate[VCCurrent/.qq], (t, 0, a)], (a, 0, T), PlotStyle → Thick]*)

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 [Cond-mat.mes-hall] 23 June 2009.

This thesis is my original work, has not been presented for a degree in any other University and that all the sources of material used for the thesis have been dully acknowledged.

Name: Eyob Kebede

Signature:

A handwritten signature in black ink, appearing to be 'Eyob Kebede', written in a cursive style.

Place and time of submission: Addis Ababa University, July 2010

This thesis has been submitted for examination with my approval as University advisor.

Name: Dr.Mulugeta Bekele

Signature:

A handwritten signature in black ink, appearing to be 'Mulugeta B.', written in a cursive style.