ADDIS ABABA UNIVERSITY
Addis Ababa Institute of Technology (AAiT)

School of Electrical and Computer Engineering

Integration of Electronics and Photonics on Monolithic Silicon to Improve the Performance of Conventional Electronic Devices

A thesis submitted to the School of Graduate Studies of Addis Ababa University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering (Microelectronics)

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Declaration

The work presented in this thesis was carried out in the school of Electrical and Computer Engineering, Addis Ababa University. The work has not been submitted for any other degree in the University or elsewhere, and unless stated otherwise, I, the undersigned, declare that this thesis is my original work performed under the supervision of Dr. Eng. Getachew Alemu and that all sources of materials used for the thesis have been correctly acknowledged.

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The thesis has been submitted with my approval as advisor.

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Dedication

To the memory of my mother Amlisha H. not alive today.

Abstract

Conventional electronics have shown dramatic improvement in dimensions and performances over the last four decades and plays a great role in computing, storing, transmitting and retrieving data in all electronic devices. However, chip-to-chip and on-chip interconnect which have affected by a parasitic load became the real performance bottleneck due to its extremely reduced cross section dimension along with moore's law. Now, there are metal (copper) interconnections and dielectric materials in IC fabrications that faces great challenges for the future in the electronics, imposing problems of interconnect that the performance and functionality of conventional electronic devices are leading their physical limit in speed, bandwidth, power consumption (heating) and electromagnetic interference.

In contrary, photonic devices have advantages like large bandwidth, lower power consumption (low heating) and immune to electromagnetic interference. So an integrated electro-photonic interconnect have seen an alternate solution for the future technology nodes due to their special physical characteristics. Therefore in order to overcome these electronic limitations have been faced, an integrated electronics and photonics on monolithic silicon substrate has been proposed as a potential solution by merging the advantage of both technologies, electronics for data processing and storing while photonics for both on-chip and off-chip interconnection to obtain a future supper computing device.

To study the integration of electronics and photonics on monolithic silicon substrate to improving the performance of conventional electronic devices, two experimental set up were prepared on laboratory at device level. The first experimental set up was integrated electronic and photonic interconnect. Its components were connected with waveguide or glass rod and represented by electrophotonic interconnect. The second experimental set up was conventional electronic circuit. Its components were connected by copper wire (Cu). Both experiments had similar three different **lengths** (30, 10, and 5) cm of **Cu wire** and **waveguide** at ϕ of 1mm and 1cm respectively for both **voltage** and **current** output measurements from the system. And both experiments had again similar three different **diameters** ϕ (13, 9, and 6) mm of **Cu wires** and (1, 0.5, and 0.2) mm of **waveguides** at equal length of 25cm for **delay** and **power** measurements in the system at different **clock frequencies** (50, 75 and 100) kHz. Comparisons were made and based on the result found electrophotonic interconnect performed better than that of the Cu interconnect in terms of delay and power. Therefore, delay and power dissipation on Cu interconnect was higher than electrophotonic interconnect by 62.8% and 60% respectively.

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List of acronyms and abbreviations

IC	Integrated Circuit
ϕ	Diameter
RC	Resistor Capacitor
I	Current
V	Voltage
E	Electric field
EM	Electromagnetic
EMI	Electromagnetic Interference
UV	Ultraviolent
IR	Infrared
SOI	Silicon on Insulator
B	Bandwidth
WDM	Wavelength Division multiplexer
TIR	Total Internal Reflection
Si	Silicon
Ge	Germanium
Ga	Gallium
As	Arsenide
Al	Aluminum
λ	Wavelength
SPP	Surface Plasmon Polariton
CMOS	Complementary metal oxide semiconductor
B	Bandwidth
Cu	Copper
ITRS	International technology Roadmap for semiconductor
VCSEL	Vertical cavity surface emitting laser
n	refractive index
Tx	transmitter
Rx	Receiver
TRx	Transceiver
PIC	Photonic Integrated Circuit
I/O	Input/ Output
Tz	Transistor
Int	Interconnect
f	frequency
EP	Integration of Electrophotonics
VEP	Voltage in Electrophotonics
IEP	Current in Electrophotonics
TM/TE	Transverse Magnetic/Electric
IT	information technology
IBM	international business machine

CHAPTER 1: INTRODUCTION

1.1 Background

1.1.1 Electronics

In the 21st century we are enjoying well developed electronics in which the era of human history revolutionized in data processing, communicating and storing information in silicon integrated circuit (IC). And electronic devices have made it possible to manufacture a wide array of electronic consumer, medical equipments, industrial, and military products. The field of electronics was born in 1883 when Thomas Edison discovered an electron tube. The prolific American inventor, Thomas Edison is often credited with the invention of the incandescent lamp. Edison was able to achieve his success by placing his filament (made of carbonized sewing thread) inside of a clear glass bulb from which the air had been forcibly removed. In this vacuum, the filament could glow at white-hot temperatures without being consumed by combustion. In the course of his experimentation, Edison placed a strip of metal inside of an evacuated (vacuum) glass bulb along with the filament. Between this metal strip and one of the filament connections he attached a sensitive ammeter. What he found was that electrons would flow through the meter whenever the filament was hot, but ceased when the filament cooled down. The white-hot filament in Edison's lamp was liberating free electrons into the vacuum of the lamp, those electrons finding their way to the metal strip, through the galvanometer, and back to the filament.

Next, In 1906 Lee De Forest, an American engineer developed a type of vacuum tube that was capable of amplifying radio signals (first electronic amplifier) based on Thomas Edison principle. He made a startling discovery by placing a metal screen or grid between the glowing filament and the metal strip (which by now had taken the form of a plate for greater surface area), the stream of electrons flowing from filament to plate could be regulated by the application of a small voltage between the metal screen and the filament. A negative voltage applied to the grid with respect to the filament would tend to choke off the natural flow of electrons, whereas a positive voltage would tend to enhance the flow. In operation, the anode in such a vacuum tube is given a positive potential (positively biased) with respect to the cathode, while the grid is negatively biased. A large negative bias on the grid prevents any electrons emitted from the cathode from reaching the anode; however, because the grid is largely open space, a less negative bias permits some electrons to pass through it and reach the anode. Small variations in the grid potential can thus control large amounts of anode current. The vacuum tube permitted the development of radio broadcasting, long-distance telephony, television, and the first electronic digital computers. These early electronic computers were, in fact, the largest vacuum-tube systems ever built. Perhaps the best-known representative is the ENIAC (Electronic Numerical Integrator and Computer), completed in 1946.

Vacuum tubes are fragile and ultimately wear out in service. Failure occurs in normal usage either from the effects of repeated heating and cooling as equipment is switched on and off (thermal fatigue), which ultimately causes a physical fracture in some part of the interior structure of the tube, or from degradation of the properties of the cathode by residual gases in the tube. Vacuum tubes also take time (from a few seconds to several minutes) to "warm up" to operating temperature—an inconvenience at best and in some cases a serious limitation to their use. The vacuum tube looks and behaves very much like a light bulb; it generates a lot of heat and has a tendency to burn out. Also, compared to the transistor it is slow, big and bulky. When engineers tried to build complex circuits using the vacuum tube, they quickly became aware of its limitations. The first digital computer ENIAC, for example, was a huge monster that weighed over thirty tons, and consumed 200 kilowatts of electrical power. It had around 18,000 vacuum tubes that constantly burned out, making it very unreliable. These shortcomings motivated scientists at Bell Laboratories to seek an alternative to the vacuum tube and led to the development of the transistor. The invention of the transistor in 1947 by John Bardeen, Walter H. Brattain, and William B. Shockley, the transistor revolutionized the field of electronics, and paved the way for smaller and cheaper radios, calculators, and computers, among other things. The invention of the transistor of the Bell research staff provided the first of a series of new devices with remarkable potential for expanding the utility of electronic equipment. With the small and effective transistor at their hands, electrical engineers of the 1950s saw the possibilities of constructing far more advanced circuits than before. However, as the complexity of the circuits grew, problems started arising. When building a circuit, it is very important that all connections are intact. If not, the electrical current will be stopped on its way through the circuit, making the circuit fail. Before the integrated circuit, assembly workers had to construct circuits by hand, soldering each component in place and connecting them with metal wires. Engineers soon realized that manually assembling the vast number of tiny components needed in, for example, a computer would be impossible, especially without generating a single faulty connection.

Another problem was the size of the circuit interconnecting with discrete transistors required large board. A complex circuit, like a computer, was dependent on speed. If the components of the computer were too large or the wires interconnecting them too long, the electric signals couldn't travel fast enough through the circuit, thus making the computer too slow to be effective. Since computers employed hundreds of thousands of transistors each, size of circuit was large and interconnecting these components became difficult to troubleshoot the complex circuit. After World War II, with this fact, together with the need for compact, lightweight electronic missile-guidance systems, led to the invention of the integrated circuit (IC) independently by Jack Kilby of Texas Instruments Incorporated On September 12, 1958 and by Jean Hoerni and Robert Noyce of Fairchild Semiconductor Corporation in 1959 [1].

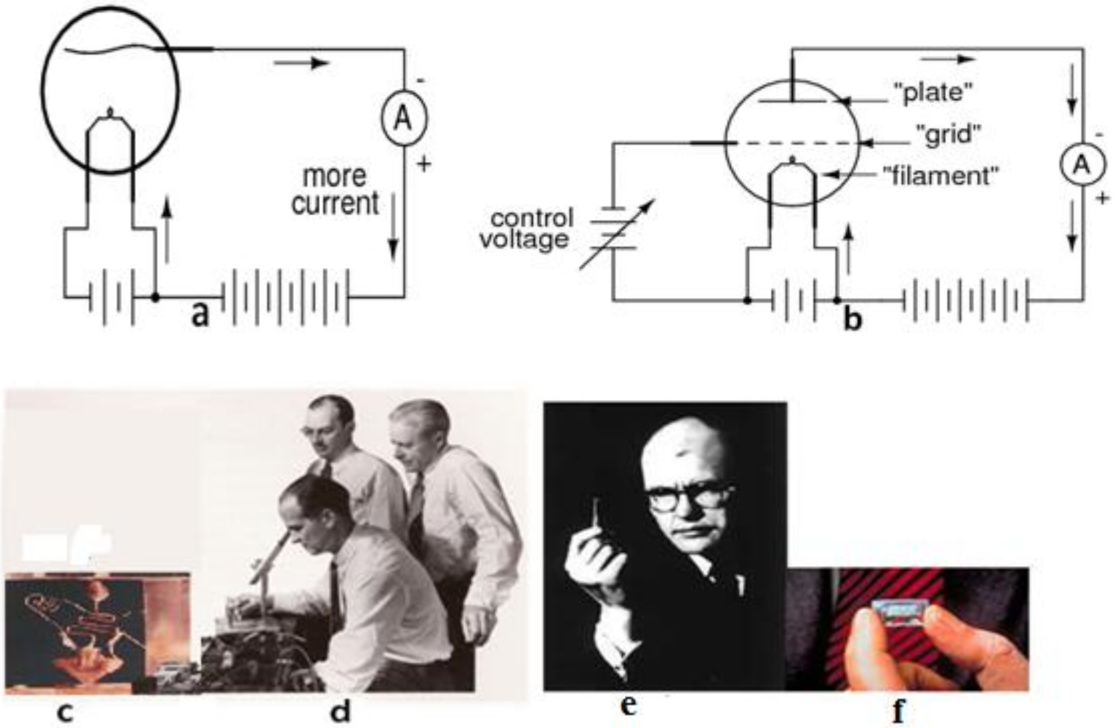


Figure 1 (a) Electron tube (b) Vacuum tube (c) First Transistor (d) Inventors of transistor (e) Kilby and (f) First IC [1].

In 1965 Gordon Moore predicted that the number of components on a silicon chip would double every year. This he later revised to a doubling every 18 months [2], which is a rate that still holds true even today. Early ICs contained about 10 individual components on a silicon chip 3 mm (0.12 inch) square. By 1970 the number was up to 1,000 on a chip of the same size at no increase in cost. Late in the following year the first microprocessor was introduced. The device contained all the arithmetic, logic, and control circuitry required to perform the functions of a computer's central processing unit (CPU).

This type of large-scale IC was developed by a team at Intel Corporation, the same company that also introduced the memory IC in 1971.

As scaling down size of transistors based on moore's law, the cost is reduced per transistor in turn this allowing more transistors to be fabricated on the same amount of silicon chip. The smaller transistors can also operate at higher frequency and power required per transistor decreases. However, there is an increase in total power dissipation on the chip from the smaller and more abundant passive metal interconnect layers which are used for data transmission, signaling and clocking. As the clock speed is increased this leads to more heating in the IC due to copper wire because scaling transistors with interconnect, increasing resistance of the wires leads to $I^2 R$ (I is the current and R resistor) power dissipation in the form of heat. As the chip features are scaled down, the number of transistors is increased and the total size tends to stay constant. The propagation delay per unit length will increase as the wires get smaller in cross-section [3]. The propagation delay in a single large processor will begin to cause problems as the frequency is increased due to RC delay increased. In order to limit the impact of propagation delay processor fabrication has now shifted from a single large processor running at high clock speeds to multiple independent cores running at moderate clock speeds. Increases in performance required for continued expansion are found through the addition of more cores to a processor.

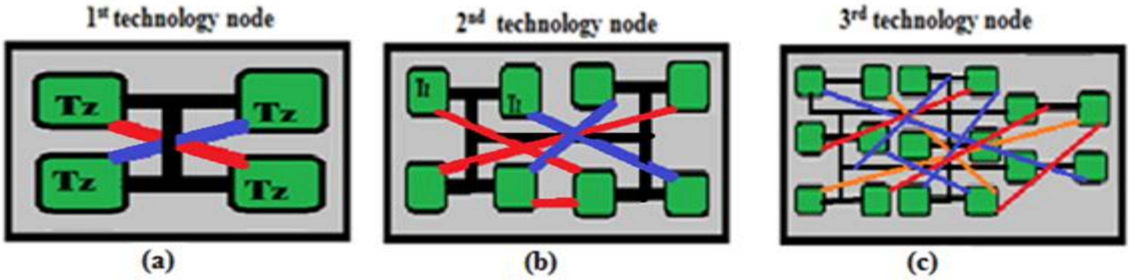


Figure 2 Technology node & number of transistor (Tz) based on Moore's law (a) 4 (b) 8 (c) 16.

Multi Core System

Having multi core processors in a chip lowers the maximum distance a signal needs to travel within a clock cycle reducing the length of interconnects. While the shift towards multi-core processors alleviates the interconnect problems in the short term, in order to satisfy timely growing user demand of complex function required high processing device as more and more cores are added the interconnect problem will return again.

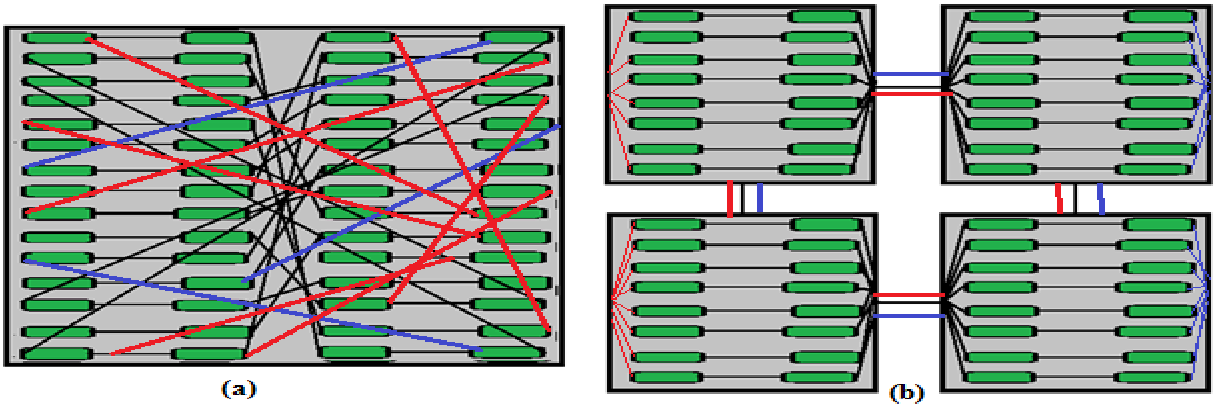


Figure 3 Interconnections in IC (a) Single core (b) Multi-core system.

Therefore, the conventional electronics faced with problems of high energy requirement, high power dissipation in the form of heat, speed limited, electromagnetic interference and limited bandwidth.

1.1.2 Photonics

The history of photonics was started from optics. Optics can be defined as the branch of physical science which deals with light and its behavior, propagation and interaction with matter. Light, the main subject of optics, is electromagnetic (EM) radiation in the wavelength range extending from the vacuum ultraviolet (UV) at about 50 nanometers to the far infrared (IR) at 1 mm. The first revolutionary event in modern optics was, no doubt, the invention of the laser by T.H. Maiman in 1960 at Hughes Research Laboratories in Malibu [4], which allowed the availability of coherent light sources with exceptional properties, such as high spatial and temporal coherence and very high brightness. A second major step forward came with the development of semiconductor optical devices for the generation and detection of light, which permitted very efficient and compact optoelectronic devices. The last push was given by the introduction of new fabrication techniques for obtaining very cheap optical fibers, with very low propagation losses. As a result of these new developments and associated with electronics, new disciplines have appeared connected with optics: **optoelectronics and waveguide technology**, etc. Thus, classical optics, initially dealing with lenses, mirrors, filters, etc., has been forced to describe a new family of modern optics which is much more complex devices such as semiconductor lasers, detectors, waveguides, etc. The operation of these devices must be described in terms of optics as well as of electronics, giving birth to a mixed discipline called **photonics**.

Photonics is the technology associated with signal generation, processing, transmission, and detection where the signal is carried by **photons** (i.e., light). And where spatial confinement considerably modifies light propagation and light–matter interaction. This includes different photonics devices like waveguide, laser light source, detector, multiplexers/demultiplexers and modulators have shown that these devices can be fabricated on silicon. If the last century was the era of electronics, the twenty-first century is probably the era of photonics. If **electronics** can be considered as the discipline that describes the flow of **electrons**, the term **photonics** deals with the control of **photons**.

1.1.3 Integration of electronics and photonics

Integration of components refers to the fabrication of multiple devices within a single discrete package. In contrast to discrete, integration has many benefits including increased performance, smaller size, high speed, lower cost, reliability and greater utility. Components that are monolithically integrated are made on the same substrate with common processing steps. While for hybrid integration, multiple substrates are processed separately and the components are assembled afterwards. To be monolithically integrated with standard electronic and photonic devices must be fabricated in single silicon substrate with fully compatible with CMOS.

Although photonics are supposed to be efficient in terms of power consumption, speed, free of electromagnetic interference and bandwidth, the existing silicon photonic technologies involve problems limiting their efficiency when it is reduced the dimension of devices. Because Optical interconnections are based on the total internal reflection (TIR) principle that a light field can usually be confined in the best case to the size comparable to its wavelength due to the diffraction nature of light. In the fig.4 below (a) electrical pulse drive the laser and light emitted by the laser propagated based on TIR through glass rod to light detector. (b) Multi-wavelength rays propagated in single waveguide (glass rod) by wavelength division multiplexing (WDM).

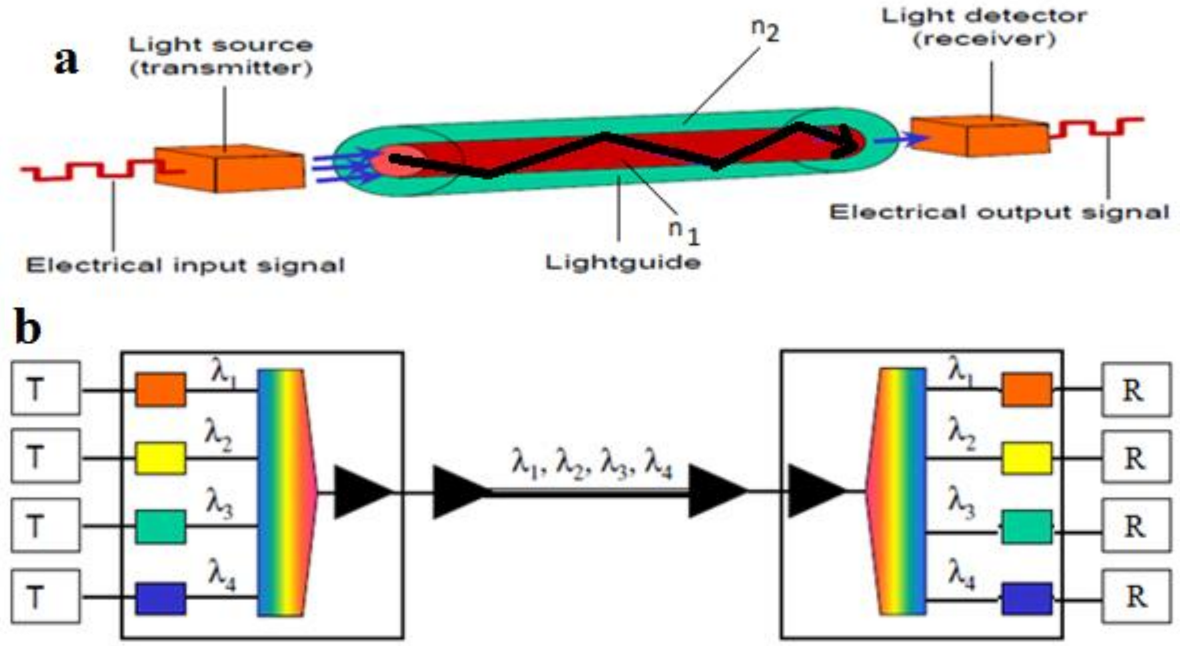


Figure 4 Diagram of (a) fiber optic system and (b) WDM [19].

However, during integration TIR photonic waveguides encounter an obstacle, so minimizing this to the nano-scale and keeping the same functionality is difficult. This limitation is that light waves cannot be confined in a region with a dimension less than half their wavelength in the material; this phenomenon is called the diffraction limit.

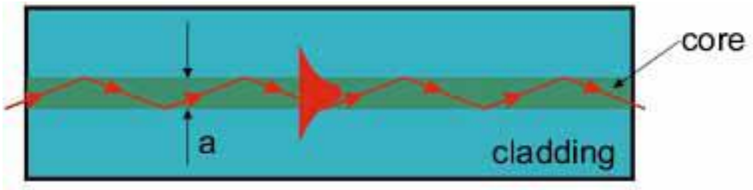


Figure 5 Relationship of wavelength and cross sectional area of a waveguide [20].

In order to conform to the diffraction limit, the core transverse dimensions d_x and d_y of a dielectric waveguide cross sectional dimension should be $d_x, d_y \geq \frac{\lambda}{2n_{core}}$, Where λ is the free space wavelength, and n_{core} is the core refractive index [20]. This diffraction limit represents a critical barrier to nanophotonic chip technology. However optical interconnects such as fiber optic cables can carry digital data with a capacity > 1000 times that of electronic interconnects. Unfortunately, fiber optic cables are ~1000 times larger compared with electronic components, and the two technologies are difficult to combine on the same circuit [21]. Microelectronic circuits can be fabricated at dimensions below 100 nm. On the other hand, the wavelength of light used in photonics circuits is on the order of 1000 nm. When the dimensions of an optical component become close to the wavelength of light, the propagation of light is obstructed by optical diffraction [21], which therefore limits the minimum size of optical devices. Optical components however, are notoriously difficult to scale down due to the diffraction (limit) barrier restricting dimensions to half of the effective wavelength [22]. To overcome this problem another technology for wave guiding, it is possible to confine the light field below the diffraction limit in a surface Plasmons (SP) of plasmonic waveguide.

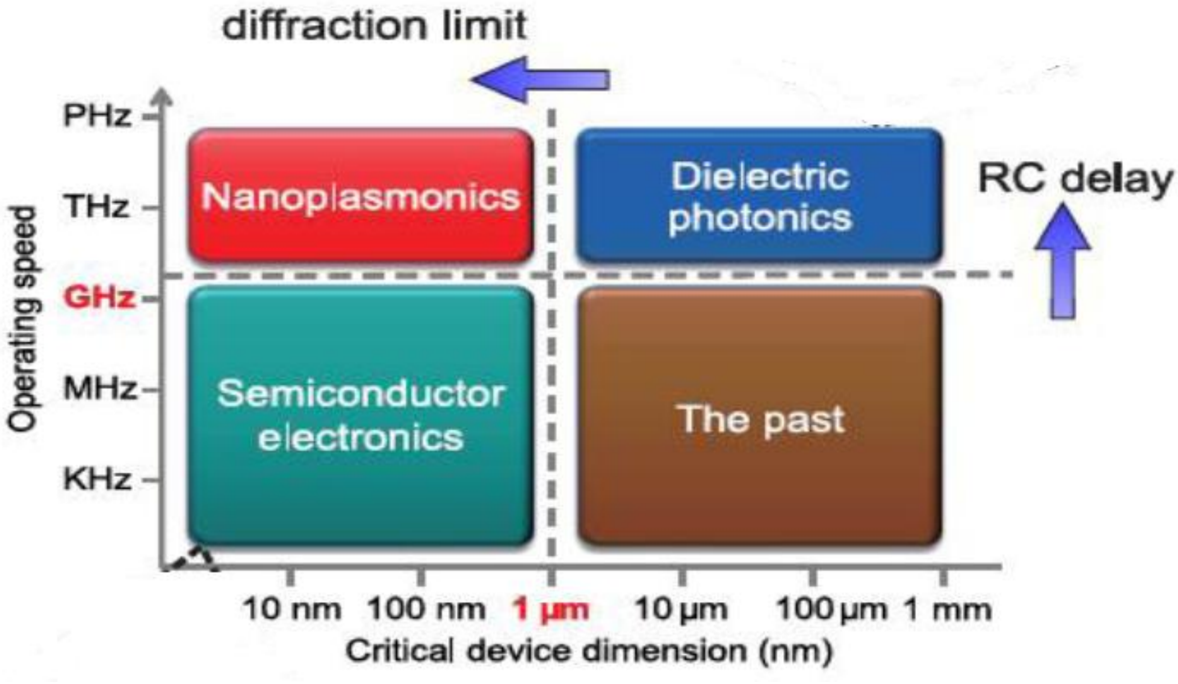


Figure 6 Limitations in the operation speed and dimension of current communication technologies [25].

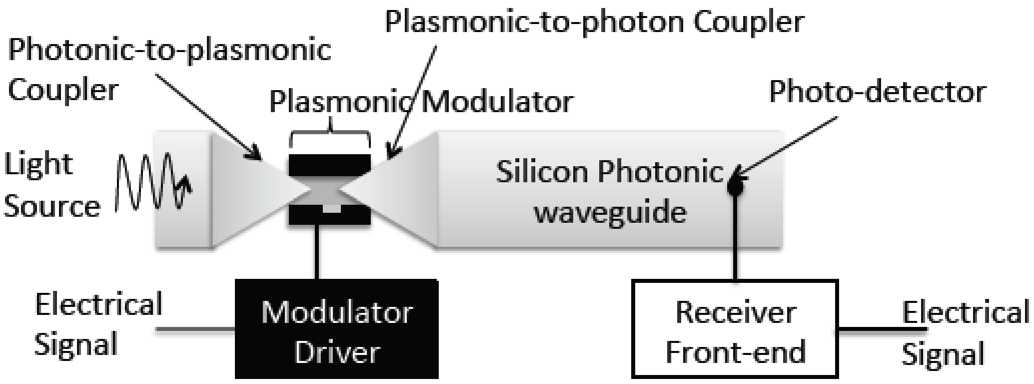


Figure 7 Plasmonic modulator and waveguide, Convert photons into SPP and vice versa [26].

1. 2 Problem Statement

Modern electronic devices in semiconductor technology have led us to current era of big data and super-computing that the whole society is unprecedentedly connected and computerized. However, conventional electronic devices have been faced great challenges by a parasitic load for current and future technology nodes with scaling down of IC. The thesis's problem statement was pointed out from what actually happened on all electronic devices during multi program execution. These electronic devices like data servers, smart mobile phones, and desktop (laptop) computers) are suffering of excessive **power dissipation in the form of heating** and **slowing down of its speed** (sometimes under busy condition) during simultaneous program executions. These two problems can be visualized easily when the devices are ordered by the user to operate with number of instructions such as word processing, playing movies, connecting people together through chat, voice and video calls through Internet. When computers or mobile phones will increase data processing with above listed applications, the processor will also increase its clock frequency to process all user functions simultaneously to satisfy user demand. The resistances of the Cu wire on the devices become increase in line to the operating clock frequency. Thereby the following problems are observed on the devices.

The first problem will be seen that a huge power dissipation especially in the passive metal interconnect (Cu wire) in the form of **heating** on the device. For this reason, **electric fans** will be installed on computers and data servers during device fabrication for ventilating. And this addition of ventilator will incur additional cost, space and weight to the device fabrication. Second, the **speed** of the device will be slowly decreased with increasing computer tasks and then the computer might be in a busy condition during simultaneous program executions. The delay in computer is caused by resistance of Cu wire and capacitance of dielectric material on IC. Therefore, as increasing computer applications, it demands higher clock frequency for processing of these instructions. This frequency again increases resistance of the wires that leading to increase the RC delay to retard the speed of the computer. Heating and delay become a real challenges as scaling down of IC along with increasing operating clock frequency, increasing dielectric materials (reducing thickness) and reducing cross sectional area of Cu wires with moore's law. Therefore, these are the main problems that limit the proper operation of current and future electronic devices. In general, the performance and functions of conventional electronic devices have been limited by clock frequency, resistive of wires and capacitive of dielectric materials of ICs.

The basic physical reason is that while scaling transistors improves their switching speed, but scaling metal interconnection does not increase their data carrying capacity. For a wire of length ℓ and cross-sectional area A, the resistive loss in electrical lines, the bandwidth (B) on electrical lines is limited to the maximum capacity of the electrical interconnect can be written as: B $\alpha \frac{1}{RC}$ or B = $B_0 \frac{A}{\ell^2}$ (bit/s) [34] where Bo ~ 10^{16} bits/s for an typical RC line (on chips), and Bo ~ 10^{15} bits/s for a typical LC line (chip-to-chip). Moreover, for an electrical communication link, the minimal energy (E) required to transmit one bit of information is achieved when the electrical line is charge, and is thus related to the line capacitance C_ℓ and applied voltage V as $E \geq C_\ell V^2$ [28]. And the power dissipation (P) on this copper interconnect is $P \geq C_\ell V^2 f$ with estimated to consume about 2% of the overall electricity worldwide, with about 15%–30% of this power spent on interconnects [29]. It is also predicted that Cu interconnects are responsible for nearly 70 to 80% of the signal delay in high-speed systems [30]. And electrical interconnects performance degrades at frequencies above 1 GHz due to ringing, increased signal time delay due to the inherent RC time, reflection, crosstalk or electromagnetic interference between those wires, resistive heating due to copper wire and frequency dependent attenuation [31].

1.3 Methodology and Measurement Set Up

1.3. 1 Description about integrated electronics and photonics

To study the integration of electronics and photonics on silicon substrate to improve the performance of conventional electronics (in speed, bandwidth, power and interference), different components and interconnects were employed on experimental set up for taking measurements. The components employed for taking measurements were electronic and photonic devices with their interconnects. And these components included electronic modulator or oscillator circuit, Cu wire, glass rod, laser, detector, RC circuit and detector. Using these devices, delay and power were compared experimentally. The experimental set up had two interconnects. For the convectional electronic, components were interconnected by **copper wire.** And for the integrated electrophotonic, components were interconnected by **waveguide** (glass rod).

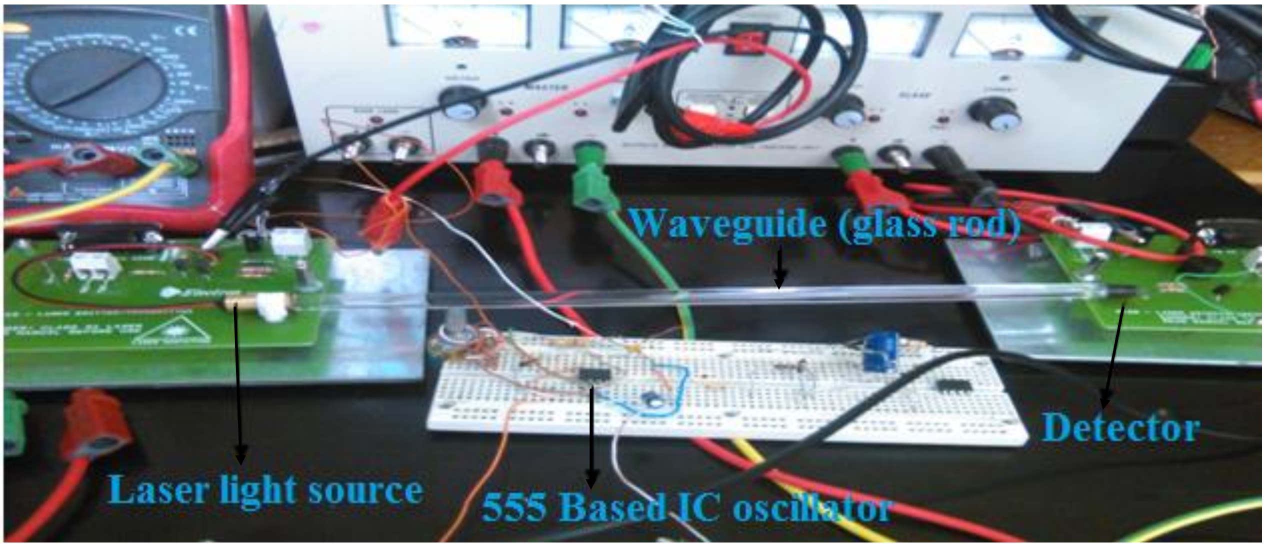


Figure 8 Full experimental set up of integrated electrophotonic interconnect.

In the fig.8 shown above, an integrated electrophotonic interconnect that contained 555 based (50, 75 & 100) KHz oscillator which built on breadboard to drive the laser light source. The oscillator acted as modulator that continuous laser light has converted to optical bit patterns (equivalent to electronic bit pattern). This pulsed laser light was propagated through the waveguide (glass rod) to laser detector. The detector converted back to electric bit pattern. Notice that the picture of conventional electronic interconnect was not depicted as integrated electrophotonic interconnect as seen above in fig.8 because conventional electronics is common known connecting of two electronic devices by Cu wire.

1.3.2 Method

The method used how to extract data was based on experimental set up in laboratories. The comparison was made in both interconnects of integrated electrophotonic and conventional electronic interconnects with the core parameters like current, voltage drop, power dissipation, and delay by varying their length, cross sectional area and operating clock frequency. As described above, the experimental set up consisted of two parts. One was conventional electronic interconnects (copper) and the second was integrated electrophotonic interconnect (waveguide or glass rod). The two interconnects had used similar parameters on similar platforms to be suitable for comparison.

For **voltage** and **current** output measurement from the given system, each experiment had three different length of copper wires (30cm, 10cm and 5cm) with diameter 1mm for conventional electronic interconnect and three different lengths of waveguide (glass rods) (30cm, 10cm and 5cm) with diameter of 1cm for integration of electrophotonic interconnect to measure the voltage and current output (obtained) from a system at equal input of voltage and current set at the input port.

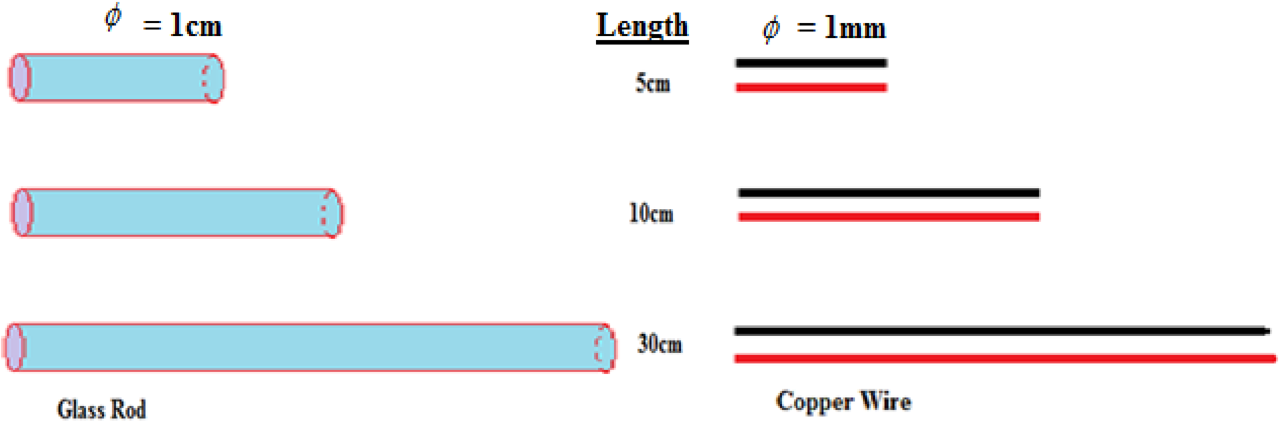


Figure 9 Comparing voltage and current output from the system of electronic & electrophotonic interconnect.

Procedure 1 for voltage and current output measurement from the systems

- Prepared three different lengths of glass rods and Cu wires as shown in fig.9
- Prepared and built the two interconnects as shown in fig.11 below both interconnect
- Set equal input of voltage and current to both interconnects (their corresponding circuits (ckts))
- Put the glass rods and Cu wires to their ckts at a time then measured as shown in table 2 & 3
- Compared both interconnects as shown in fig.45 & 46 in graph form

And for **delay** and **power** measurements in the systems of both interconnect (copper wire and waveguide) were used at fixed 25cm length but varying in their cross sectional area and clock frequency of both interconnects. The diameters of both interconnects (Cu wire and glass rod) were ϕ (1mm, 0.5mm and 0.2mm) and ϕ (13mm, 9mm and 6mm) respectively and measured the power dissipation and delay in the system. To be clear let's see the following schematic diagrams below in the fig.11 & fig.12 how the measurements for comparisons were done for power and delay.

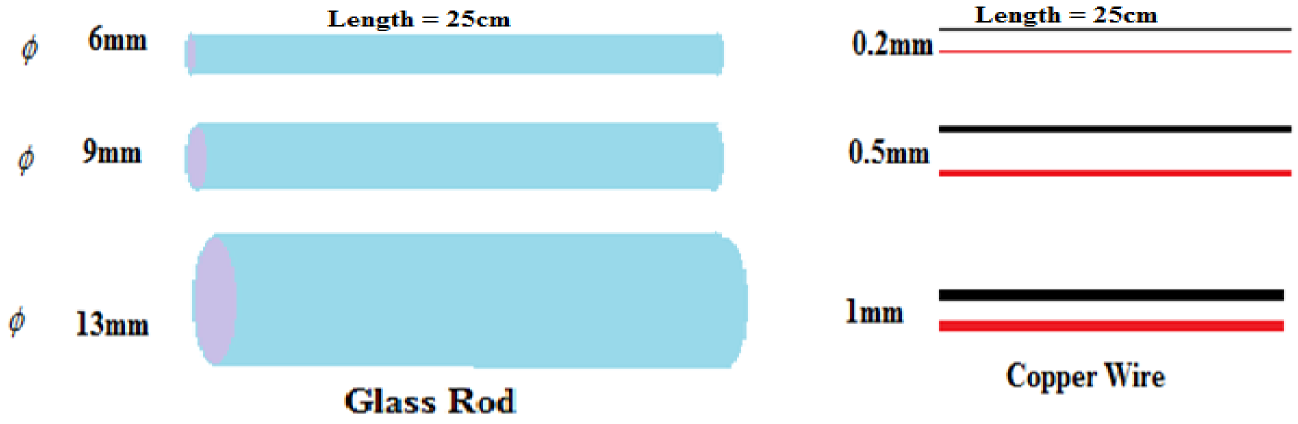
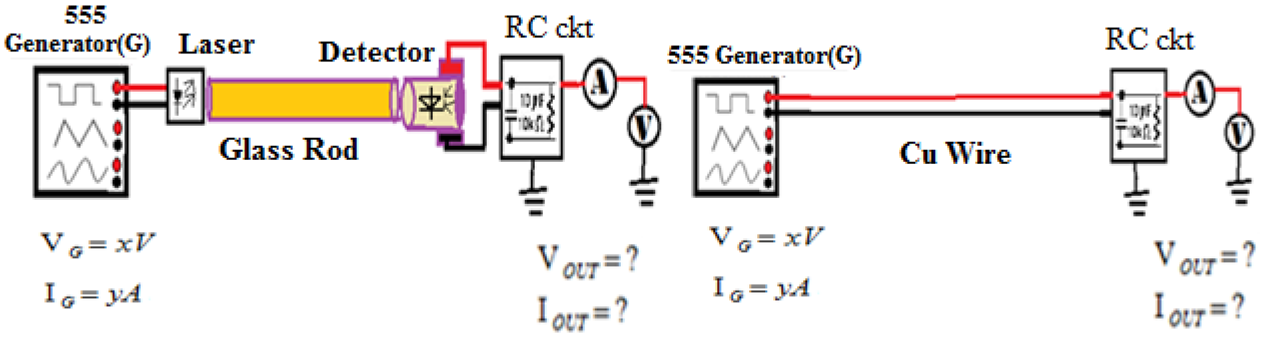


Figure 10 Interconnects used for Comparing delay and power in the system.



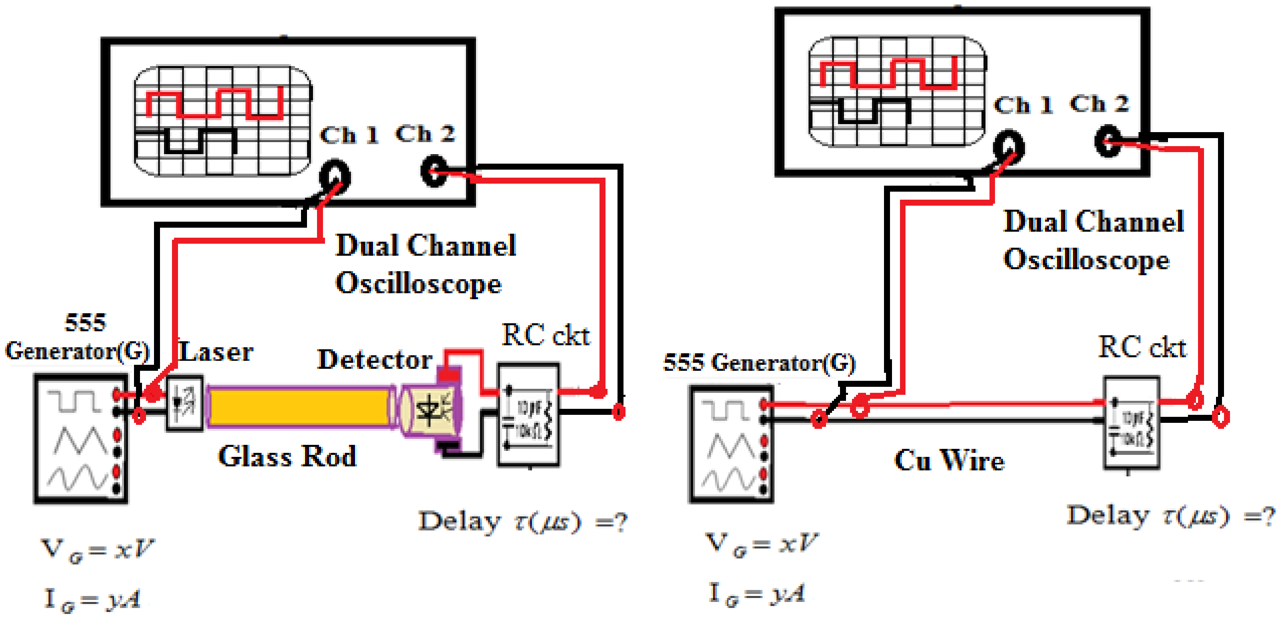
(a) Integration of Electrophotonic Interconnect

(b) Electronic Interconnect

Figure 11 Interconnections for (Voltage and Current) output from the system and (Power dissipation in the system).

Procedure 2 for delay and power dissipation measurement in the systems

- Prepared three different lengths of glass rods and Cu wires as seen in fig.10
- Prepared and built both interconnect as shown in fig.11 for power and fig.12 for delay
- Set equal input of voltage and current to both interconnects
- Put the glass rods and Cu wires at a time then measured as shown in from table 4-to-29
- Compared both interconnects as shown from fig.49 -to-58



(a) Integration of Electrophotonic Interconnect

(b) Electronic Interconnect

Figure 12 Interconnections for Delay measurement using dual channel (ch1 and ch2) oscilloscope.

1.3.3 Materials and Equipments

The experimental set up consisted of electronic and photonic devices like oscilloscope, signal generator circuit (555 timer IC, resistors, and capacitors), DC power supply, laser light source, waveguides (different lengths and diameters of glass rods), copper (different lengths and diameters of wires), light detector circuit, multimeter, voltmeter, and ammeter.

1.4 Objectives

1.4. 1 General Objective

- To investigate the performance improvement of integrated electrophotonic (waveguide interconnect) by comparing with conventional electronic (copper interconnect) based on experimental set up with the core parameters (Voltage, Current, power dissipation, delay, length, interconnect cross sectional area and operating clock frequency).

1.4.2 Specific Objectives

- To measure and compare both interconnects (integrated electrophotonic and conventional electronic) for various core parameters.
- To give theoretical description about conventional electronic interconnects.
- To give theoretical description about integrated electrophotonic (silicon waveguide + plasmonic waveguides) interconnects.
- To understand the monolithic fabrication techniques of both electronics and photonics devices on silicon substrate with similar tools.
- To show the merit of Monolithic Integration IC over discrete and hybrid IC.

1.5 Literature Review: Integration of Electronics and photonics

Monolithic fabrication of laser light on silicon facilitates for integration of ectrophotonic components and has been demonstrated in the fig.13 below. Direct growth of III-V materials hasn't approached application stage due to material mismatch. Under such a context, this is monolithic integration of III-

V lasers on Si platforms using Ge as intermediate layer for regulating material variability. For this reason, Ge is choosing as buffer layer. The laser of our choice is vertical cavity surface emitting lasers (VCSELs). VCSELs are very suitable as output devices for optical interconnects on Si platforms. The advantages of VCSELs include high-density two-dimensional array fabrication, low-cost testing and packaging, easy fiber coupling and low power consumption. Fig.13 shows a possible optoelectronic integrated circuit (OEIC) design which could fully explore the unique merits of VCSEL as array light source [32] and [33].

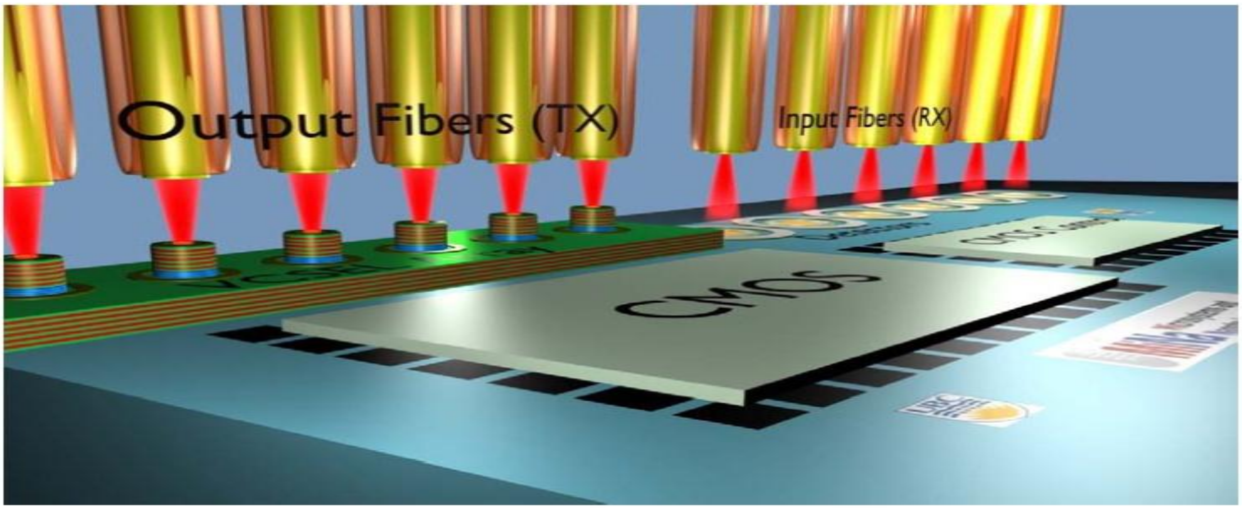


Figure 13 Optoelectronic integrated circuit (OEIC) design using VCSEL array as light source [33].

New photonic integration scheme, a single-chip photonic transceiver has demonstrated on monolithic-integrated vertical-illumination type Ge-on-Si photodetectors (Ge V-PDs) and direct-modulation light sources, vertical-cavity surface emitting lasers on a bulk silicon substrate (III-V group VCSELs-on-Si). The integration of Ge V-PDs is based on CMOS-compatible process on a bulk-Si wafer, and that of VCSELs-on-Si is based on the transplanted epitaxial film and the device fabrication on the same bulk Si wafer as the Ge V-PDs. Fig.14 shows a schematic diagram of monolithic-integrated vertical Transmitter-Receiver (TRx) devices on a bulk silicon substrate, which can be used as a photonic I/O platform for optical interconnects, applicable to electronic chips based on bulk silicon, the design of the vertical photonic TRx devices integrated on a bulk silicon substrate, chip fabrication processes, and characterizations of the integrated devices [34].

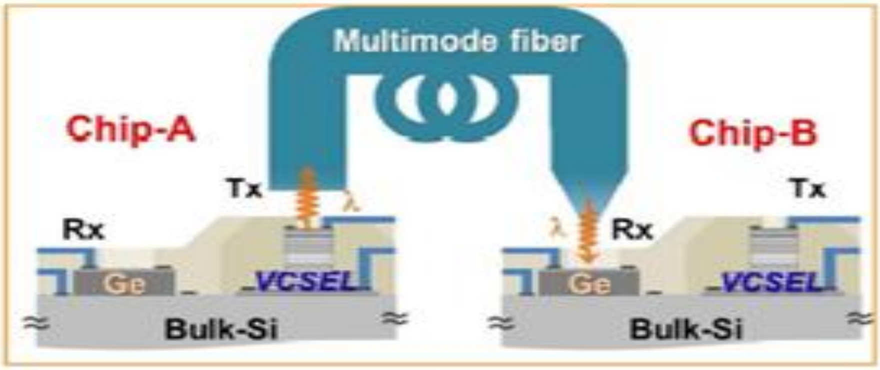


Figure 14 photonic interconnect laser (III-IV – VCSEL), detector (Ge-VPD) on Si chip [34].

In recent years, the Photonics group at IBM Research – Zurich has developed an integrated optical interconnects on printed circuit board in order to reduce the energy consumption of future IT systems. For the first time, IBM engineers have designed and tested a fully integrated wavelength multiplexed silicon photonics chip, which will soon enable manufacturing of 100 Gb/s optical transceivers [35].

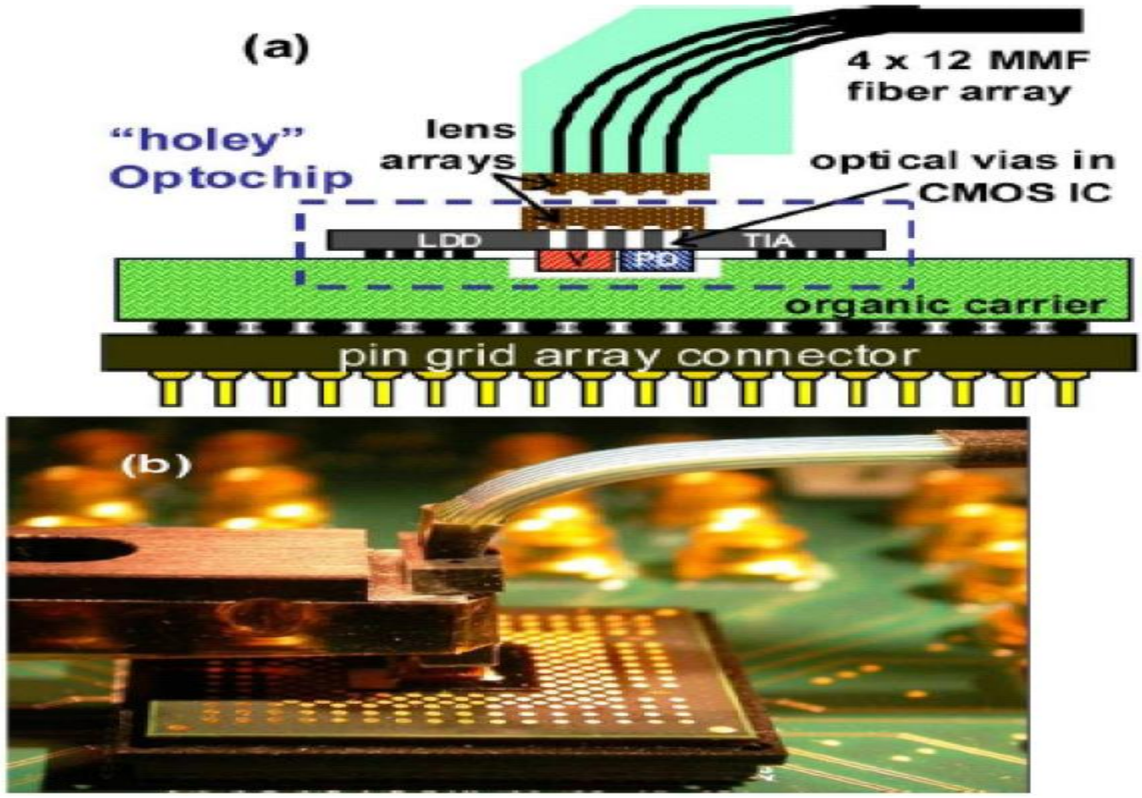


Figure 15 (a) Schematic and (b) 100Gb/s silicon photonic interconnect by the IBM Photonics Group [35].

Intel researchers have created a prototype of 50G-bps silicon photonic transmit module for chip to chip interconnects. Optics significantly wins over electrical interconnects, especially at long transmission lengths [36].

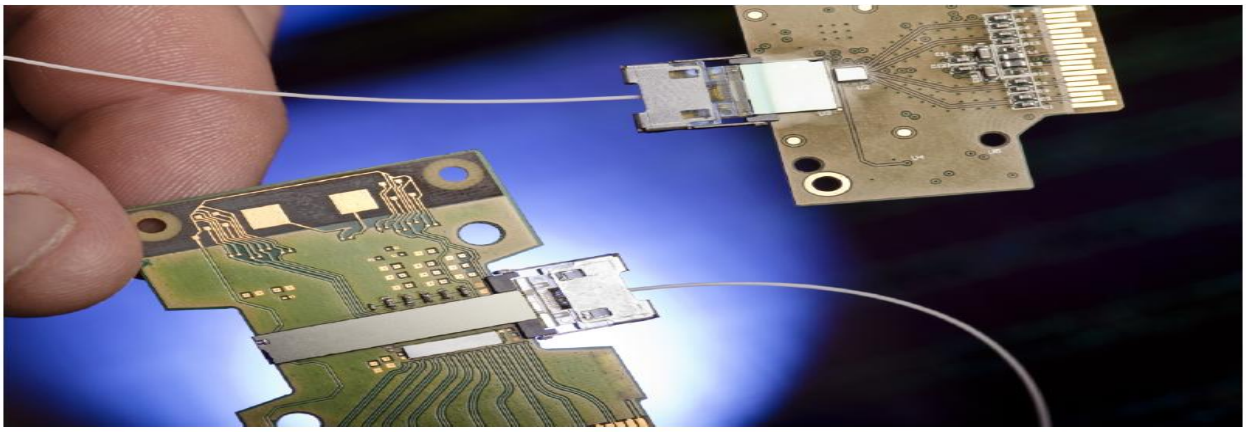


Figure 16 50Gb/s silicon photonic interconnect recently achieved by the Intel Photonics Group [36].

1.6 Organization of the thesis

The thesis is divided into 5 chapters. Chapter 2 gives detail description about photonic and its components. Chapter 3 gives about lithography for integrated circuit fabrication of electronic and photonic devices. Chapter 4 gives results and discussion about the data obtained from the experiment and its interpretation. Chapter 5 gives conclusion and recommendation for future work.

CHAPTER 2: PHOTONICS

2.1 History of Integrated Photonics

For 30 years after the invention of the transistor, the processing and transmission of information were based on electronics that used semiconductor devices for controlling the electron flux. But at the beginning of the 1980s, electronics was slowly supplemented by and even replaced by optics, and photons substituted for electrons as information carriers. Nowadays, photonic devices based on integrated photonic circuits have grown in such a way that they not only clearly dominate long-distance communications through optical fibers, the first optical waveguides, fabricated at the end of the 1960s, were bi-dimensional devices on planar substrates. In the mid-1970s the successful operation of tridimensional waveguides was demonstrated in a wide variety of materials, from glasses to crystals and semiconductors. For the fabrication of functional devices in waveguide geometries, lithium niobate **($LiNbO_3$)** was rapidly recognized as one of the most promising alternatives, at the beginning of the twenty-first century the data transfer created by computer-based business processes and by Internet applications is growing exponentially, which translates into a demand for increasing transmission capacity at lower cost, which can only be met by increased use of optical fiber and associated advanced photonic technologies.

Electrical telegraphy, first commercially used in 1839, revolutionized communication and found widespread use quickly, leading to the first commercially successful transatlantic cable in 1858. The telephone was invented in 1876; however, transatlantic telephone communication had to wait until 1927, when radio waves started to be used for that purpose. The first transatlantic telephone cable (which only had 36 channels) was deployed in 1958. The invention of the fiber optic cable offered a tremendous capacity. The first transatlantic fiber optic cable was deployed in 1988 with 40,000 channels, which provided a 10-fold increase over the previously available capacity at that time. The utilized capacity of optical fibers is expected to increase in the future [51].

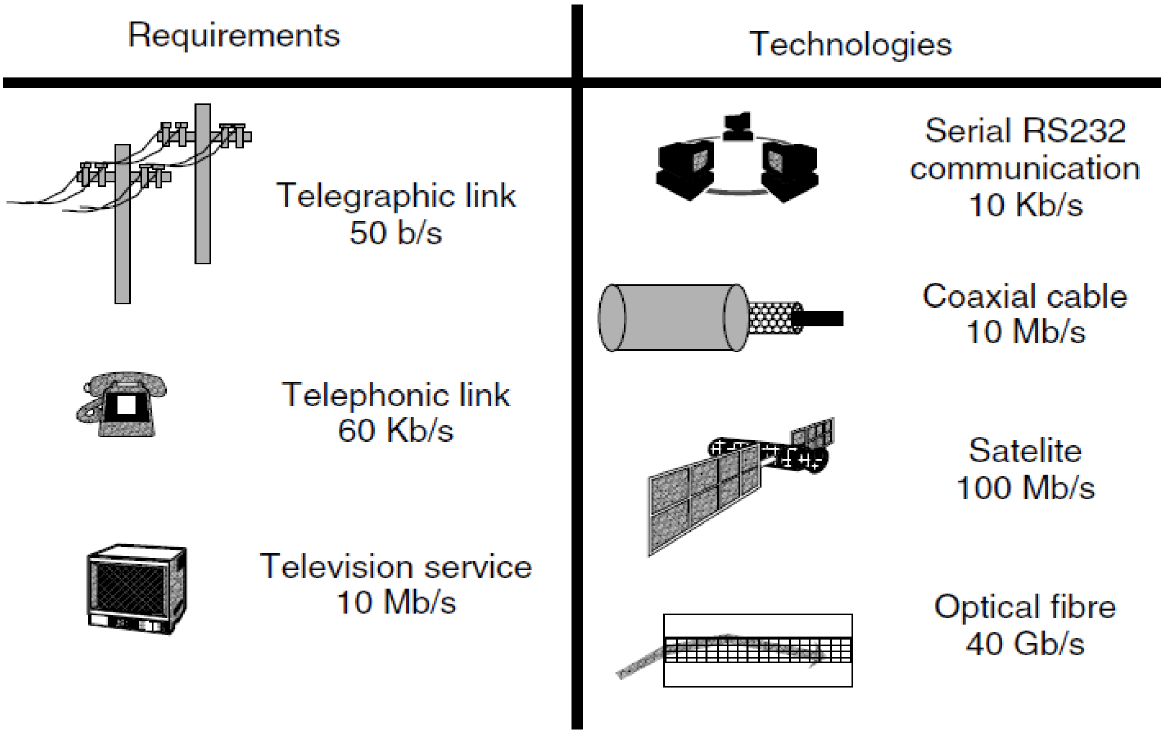


Figure 17 Requirements for data transfer and available technologies [51].

2.2 Photonic Devices

2.2.1Photonic Waveguide

2.2.1.1 Silicon waveguide

Structures that can guide and confine electromagnetic waves in two dimensions while allowing them to propagate along the third dimension are called photonic waveguides. The mechanism of controlling light within these structures depends on the core and cladding refractive indices and the incident angle of electromagnetic waves into the core. Light can be confined within the core when the core refractive index is higher than the cladding index and when the total internal reflection (TIR) principle occurs, which can be understood easily from Snell's law. Light beam can propagate along a layer of material between two different media. When an EM wave is traveling in a dielectric medium, the oscillating electric field polarizes the molecules of the medium at the frequency of the wave. Speed of light in free space to its speed in a medium is called the refractive index n of the medium [5].

$$n = \frac{C}{V} = \sqrt{\varepsilon_r}$$

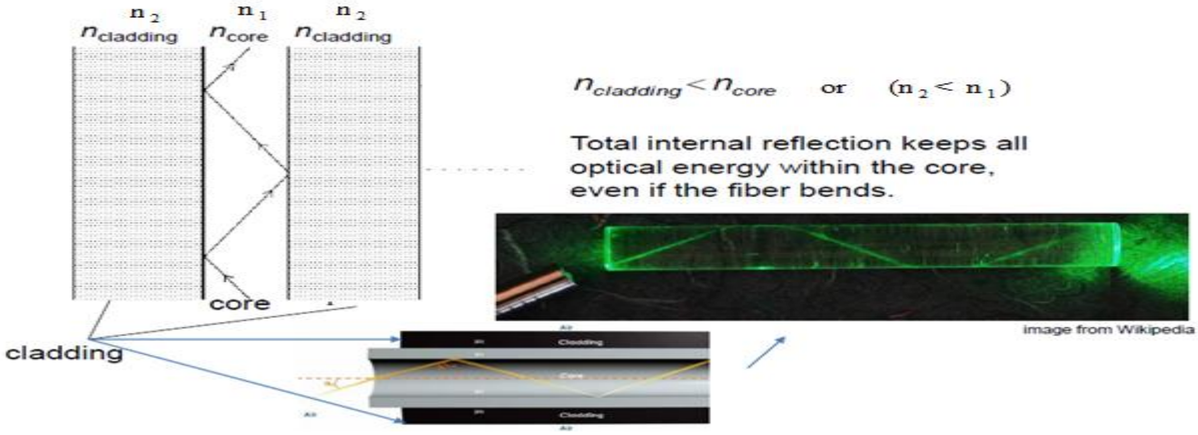


Figure 18 Light Wave propagation on two mediums with refractive index ($n_1 > n_2$) [6].

A silicon waveguide demonstrated with refractive index n_1 is surrounded by silicon dioxide n_2 regions both of refractive index ($n_2 < n_1$). The region of higher refractive index (n_1) is called the core and the region of lower refractive index (n_2) sandwiching the core is called the cladding. If k is the wave vector ($k = 2\pi/\lambda$) and λ is the wavelength, both in free space, then in the medium $k_{medium} = nk$ and $\lambda_{medium} = \lambda/n$. By employing, e.g., silicon (Si; refractive index: 3.5) as a core and silica (SiO_2; refractive index: 1.46) or air (refractive index: 1.0) as a cladding, can be fabricated a waveguide on silicon [19].

Waveguide (optical fiber) made of silicon and silicon dioxide has attenuation minima and transparent at range of wavelength from 1300 nm - 1550 nm. An SOI wafer contains an insulating layer sandwiched between two Si layers. Any thickness for the layers can be chosen. A standard material for the insulating layer is SiO_2 which has a refractive index of 1.47 for 1550 nm light (much lower than Si which is 3.48 at 1550 nm) [7].

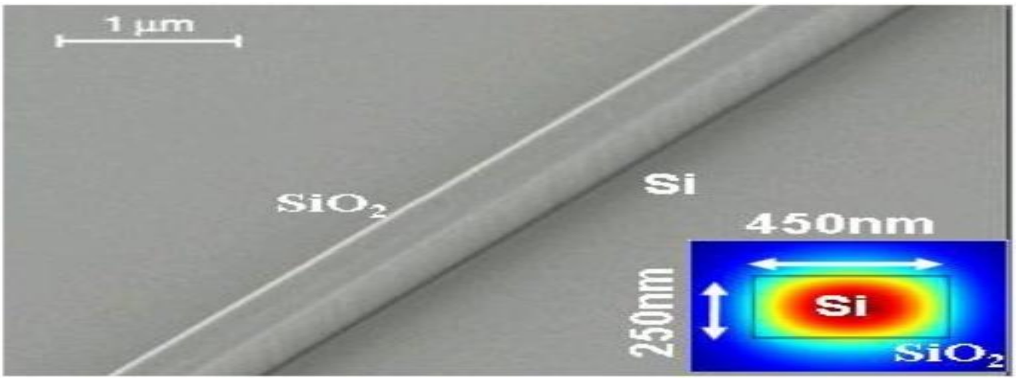


Figure 19 Silicon waveguide and its supporting mode at 1550nm wavelength [7].

2.2.1.2 Plasmomonic Waveguide

Plasmonics is an emerging field of nanophotonics in which light is controlled and guided beyond the diffraction limit by exploiting the unique optical properties of metal-dielectric interfaces. Surface plasmons (SPs) provide the opportunity to confine light to very small dimensions (at nano scale). SPs are light waves that occur at a metal/dielectric interface, where a group of electrons is collectively moving back and forth [21]. These waves are trapped near the surface as they interact with the plasma of electrons near the surface of the metal. When electromagnetic waves are incident at such an interface, the light will be coupled to electron density oscillations at the surface, thereby forming electromagnetic waves that propagate along the surface called surface plasmon polaritons (SPPs) [24].

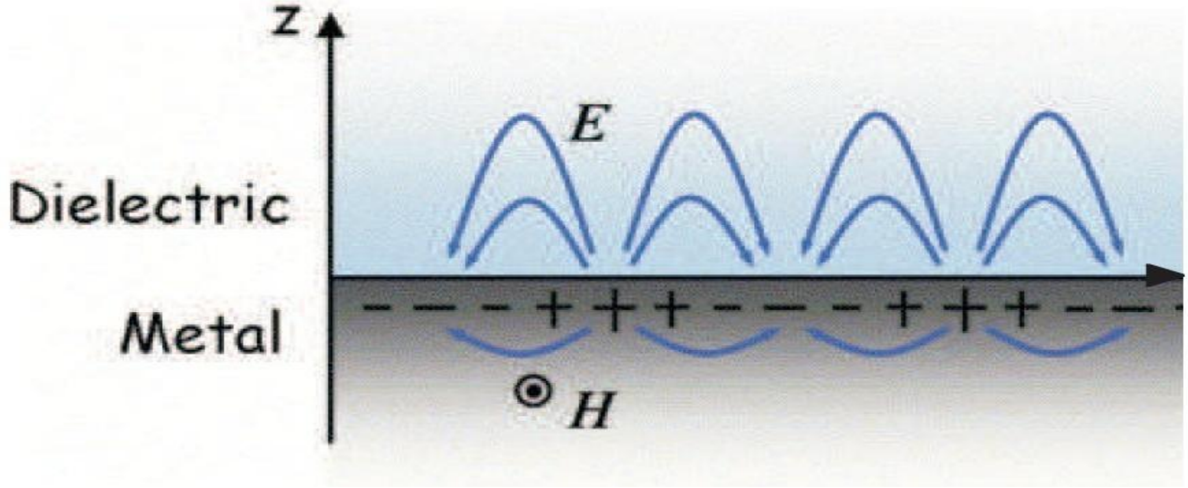


Figure 20 Electric and magnetic field with SPPs propagating along the metal and dielectric interface [22].

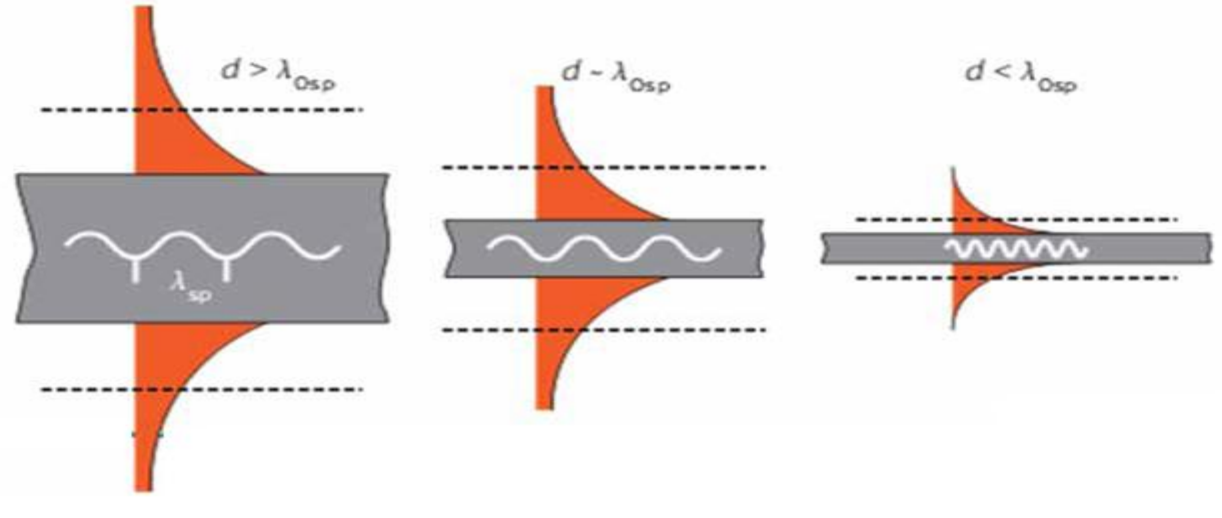


Figure 21 Confining of light on plasmonic waveguide [23].

Fabrication of multiple (electronic and photonic) devices in a single package to form electrophotonic components that are made monolithically integrated on the same substrate with common processing steps. Therefore, monolithic integration of electronics for processing and photonics for data interconnection will give us low power, high clock speed, large bandwidth and free from crosstalk. The comparison of operating speeds and critical dimensions of different chip-scale device technology of plasmonics may offer a solution, because plasmonics has both the capacity of photonics and the miniaturization of electronics.

When light is shine to metal-dielectric interface, electrons are oscillating on the surface of the noble metals like gold, silver, aluminum and copper. The oscillating group of electrons couple with the incident of electromagnetic light that produced new electromagnetic wave propagating along the interface [46] and [47].

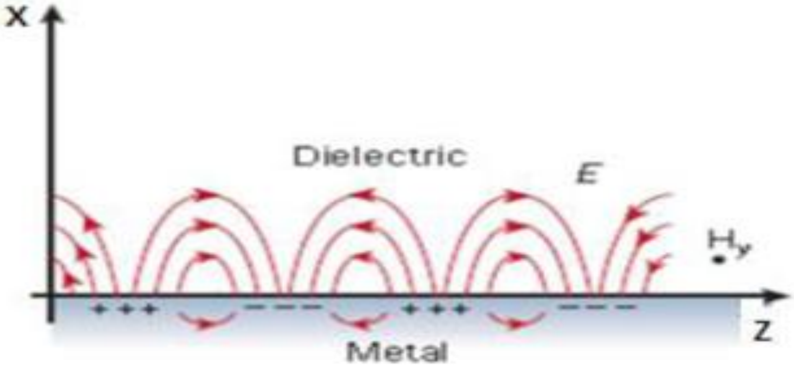


Figure 22 SPPs at the interface of metal and dielectric materials [46].

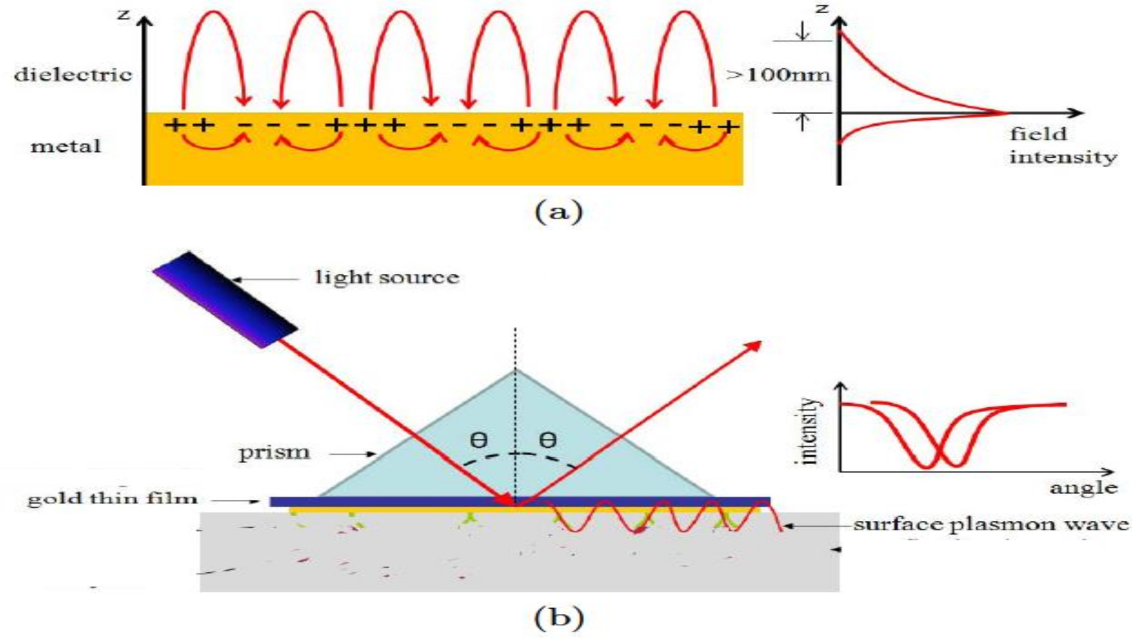


Figure 23 Schematic of (a) surface plasmon wave and (b) conventional surface plasmon resonance [47].

2.2.2 Detector

Due to the large bandgap Si is transparent to wavelengths greater than 1100 nm (1300 nm - 1550 nm). Germanium vertical photodetector (Ge V-PD) is used as a monolithic-integrated chip-level photonic receiver (Rx) on a bulk silicon substrate. The Ge V-PD, as a photonic Rx in a silicon chip, is based on a simplified structure and a selective expitaxial growth. In the fig. 24 below the Ge V-PDs are designed in array form and placed on the left side of a chip, leaving the right side of the chip dedicated to the process area for the integrated direct-modulation light source [8].

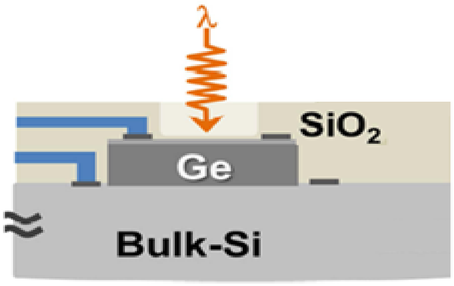


Figure 24 monolith-integrated Receiver devices on bulk silicon wafer [9].

2.2.3 Laser

Laser is abbreviated form of light amplified by stimulated emission of radiation. In optical communication the ability to emitting, modulating, guiding and detecting is very crucial. Two semiconductor materials were of particular interest due to their ability to produce active layers that emitted light at wavelengths especially suitable for transmission in silica optical fibers; GaAs and InP. The reason for this is that the optical fiber made of silicon and silicon dioxide has attenuation minima and transparent at optical range. By the combination of semiconductors with different band gaps in what is called hetero-structures. Vertical cavity surface emitting laser light (VCSELs) are based on III-V compound semiconductors such as GaAs and AlGaAs. GaAs and AlGaAs have very close lattice constants ($\Delta a/a<0.13\%$), however their lattice constants differ from Si lattice constant by 4.2%, and the thermal expansion coefficient of GaAs differs from that of Si by almost 50% (Table 1). It results in unacceptably high densities of dislocation defects in the active region of GaAs-based devices grown directly on Si [10].

Table 1 Lattice constants and thermal expansion coefficients of Si, Ge, GaAs and AlAs [10].

Material	Si	Ge	GaAs	AlAs
Lattice constant at 300k	5.4307	5.6575	5.6532	5.6622
Linear coefficient	2.49	5.8	5.4	3.5

Monolithic Integration of VCSEL on Si is the technique greatly reduces the defect density to meet device quality requirement, but it needs more than 10 µm thickness between Si and GaAs, which has similar problem of hybrid integration. The large transition SiGe buffer layer thickness is not desirable for high density integrated chip and it is hard to reduce without increasing dislocation due to the 4.2% lattice mismatch between Ge and Si. Most VCSELs are based on GaAs/AlGaAs or GaAs/InGaAs material systems In this work, the double brag reflectors (DBRs) are super lattices of $Al_x Ga_{1-x} As/ Al_y Ga_{1-y} As$ with different composition for efficient light reflection, and the layers with different compositions are shown with different colors in Fig. 25 below for a laser device to lase, light needs to travel back and forth between two reflectors with high reflectance, smooth surfaces in the designed wavelength window, such that stimulated emission can be turned on and reach enough amplification to dominate over spontaneous emission [11].

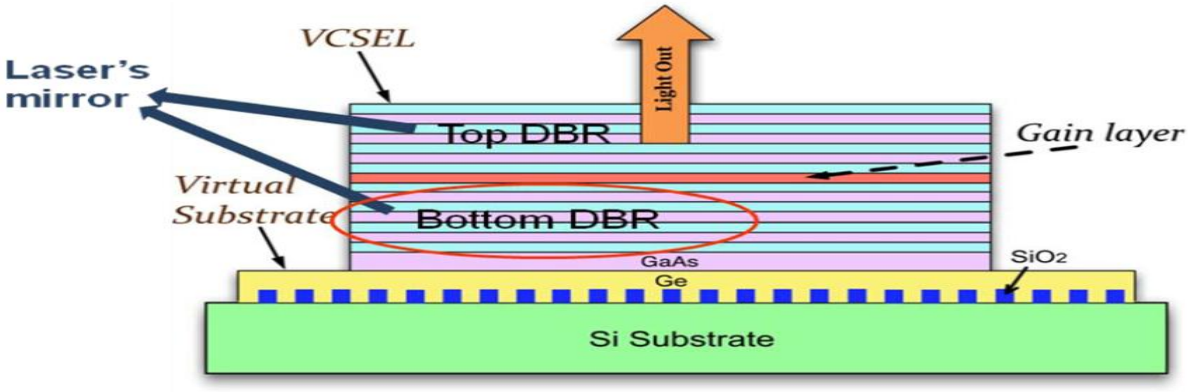


Figure 25 Monolithic integrated VCSEL grown on Ge/Si substrate with GaAs buffer layer [11].

2.2.4 Modulator

Modulation is the process of converting or encoding the continuous laser source based on electrical bit patterns in to optical pattern. Modulating light using an electrical signal is an important functionality in any interconnects platform. Optical modulation can be applied to silicon photonic interconnects platform by changing the refractive index in three ways: Thermal-Optical Effect, Electric Field Effects and Plasma dispersion effect (free carrier injection or depletion) [12].

2.2.4.1 Mach-Zehnder (MZ) modulators

MZ modulators operate by diverting two beams of light through two different waveguides and then combines the two beams together. As the beams are propagating, one of the optical beams traverses a waveguide whose refractive index changes on application of a bias voltage. When the two optical beams combine together, they either intersect constructively or destructively with each other, causing an on or off modulation. As the light is split between two waveguide arms, one of which has an electrically tunable phase shift. The two light beams recombine constructively or destructively depending on the phase difference between the arms. Modulating the phase difference modulates the intensity of the output signal. In the fig.26 below the photonic crystal waveguide is formed on the top silicon layer of a silicon-on-insulator wafer [13] and [14].

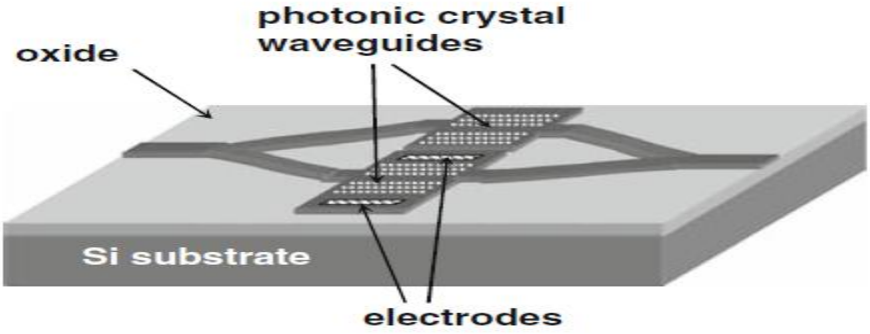


Figure 26 Schematic of a photonic crystal modulator on a silicon-on-insulator substrate [14].

2.2.4.2 Micro-ring resonators

Micro-ring resonators are the most common devices used to encode data onto an optical signal and will only couple light into waveguide/fiber if the incoming light satisfies the relation $\lambda * m = n_{eff} * 2\pi R$, where R is micro-ring resonator radius, n_{eff} is the effective refractive index of the micro-ring resonator circular waveguide, m an integer and λ is the resonant wavelength. By changing n_{eff}, the resonant wavelength of the micro-ring resonator can be changed, enabling it to function as an optical modulator (on/off keying) [15].

From fig.27 below shows the two different operations of a micro-ring resonator. When a voltage is applied, free-carriers are injected into the micro-ring resonators waveguide through a process called free-carriers plasma dispersion. These free-carriers change the effective index of the waveguide that causes the resonance wavelength to shift. In Fig.27 (a), the voltage V is switched off resulting in a shift in the resonant frequency which allows the light to pass through. In Fig.27 (b), the voltage V is switched on, resulting in the incoming light to be in resonance with the micro-ring resonator, which allows the light to be shifted to the drop port. By controlling the voltage V we can use micro-ring resonators as modulators, filters, etc [16], [17], and [18].

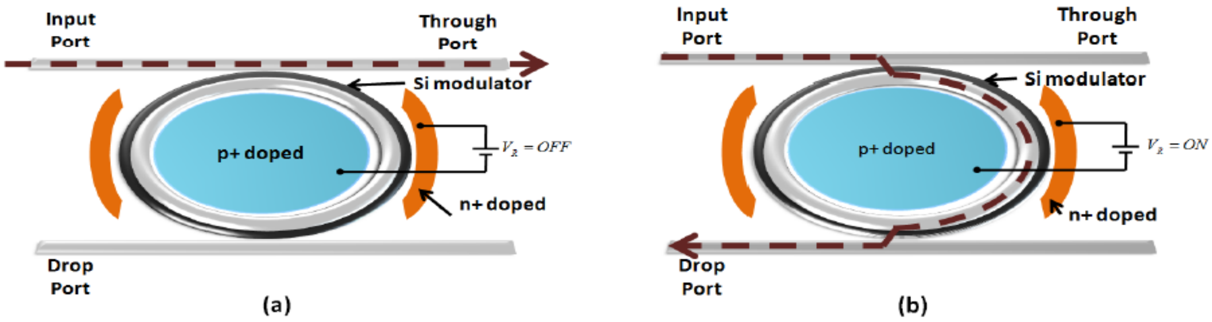


Figure 27 Micro-ring resonator operation (a) when V = V and (b) when V = V [16].

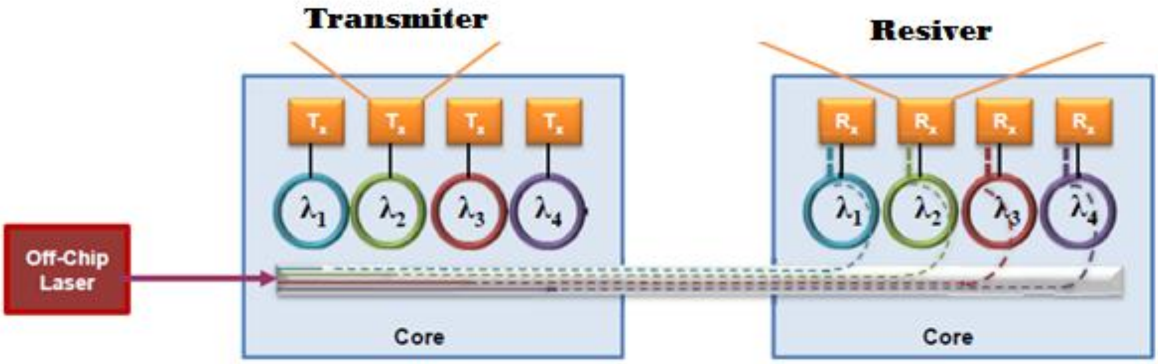


Figure 28 Photonic interconnect that consists of laser, modulator, detector and optical guiding [15].

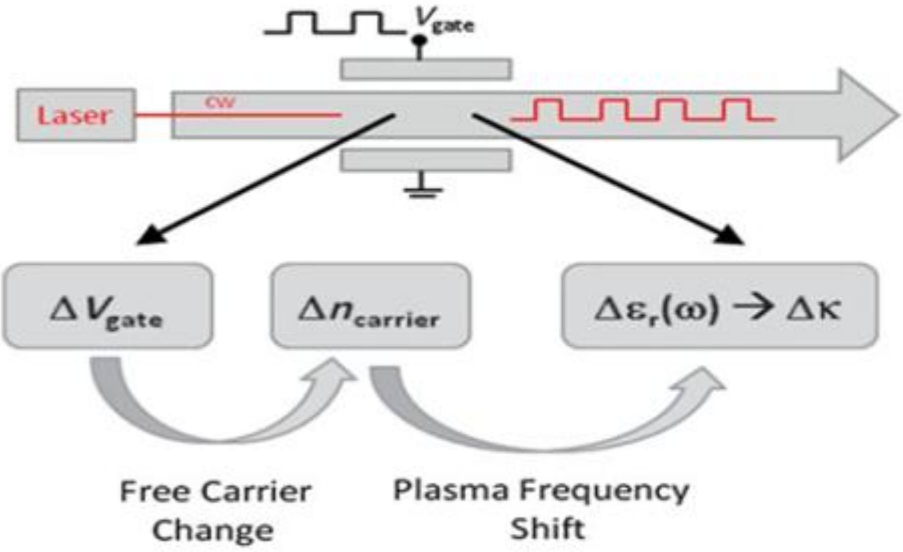


Figure 29 Optical Modulation of data switching for integrated circuits (electro-optic modulator) [18].

CHAPTER 3: IC FABRICATION

3.1 Lithography

The word lithography comes from Greek lithos, meaning stone, and graphia, meaning to write. It means quite literally writing on stones. In the case of semiconductor lithography (also called photolithography) our stones are silicon wafer and our patterns are written with a light sensitive polymer called a photoresist. Photolithography is a process of transferring of designer generated pattern or informations (device placement and interconnection) to an actual IC structure using masks (reticle) image to the surface of the wafer. To build the complex structures that make up an electronic, photonic and many wires that connect the millions of components to a circuit, lithography and etching pattern steps are repeated many times. When a sample of crystalline silicon is covered with silicon dioxide, the oxide-layer acts as a barrier to the diffusion of impurities, so that impurities separated from the surface of the silicon by a layer of oxide do not diffuse into the silicon during high-temperature processing. For transistor a p-n junction can thus be formed in a selected location on the sample by first covering the sample with a layer of oxide [oxidation step] removing the oxide in the selected region, and then performing a predeposition and diffusion step. The selective removal of the oxide in the desired area in electronic and photonic components is performed with photolithography. Thus, the areas over which diffusions are effective are defined by the oxide layer with windows cut in it, through which diffusion can take place. The windows are produced by the photolithographic process.

Photolithography utilizes light sensitive polymers know as photoresists in order to transfer a pattern from a photomask to the substrate. The two main categories of photoresist are distinguished by their tone which can be either negative or positive. Both types of resist were used for the fabrication of devices, primarily Shipley Microposit S1818 positive photoresist and AZ2070 negative photoresist [37].

Development

In the negative photoresist is used in which the areas of the photoresist that are exposed the ultraviolet radiation become polymerized. This makes the resist tougher and makes it essentially insoluble in the developer solution. In positive photoresist. Exposure to UV radiation results in depolymerization of the photoresist. This makes these exposed areas of the photoresist readily soluble in the developer solution, whereas the unexposed areas are essentially insoluble. The developer solution will thus remove the exposed or depolymerized regions of the photoresist, whereas the unexposed areas will remain on the wafer. Standard developer is 1% solution of either Sodium Carbonate Monohydrate ($Na_2CO_3.H_2O$), or Potassium Carbonate (K_2CO_3) [37].

Oxide Etching

The remaining resist is hardened and acts as a convenient mask through which the oxide layer can be etched away to expose areas of semiconductor underneath. These exposed areas are ready for impurity diffusion. For etching of oxide, the wafers are immersed in or sprayed with a hydrofluoric [HF] acid solution. This solution is usually a diluted solution of typically 10: 1, H_2O: HF, or more often a 10: 1 NH_4F [ammonium fluoride]: HF solution. The HF solutions will etch the SiO_2 but will not attack the underlying silicon, nor will it attack the photoresist layer to any appreciable extent. The wafers are exposed to the etching solution ion enough to remove the SiO_2 completely in the areas of the wafer that are not covered by the photoresist [37].

Photoresist Removal (Stripping)

Following oxide etching, the remaining resist is finally removed or stripped off with a mixture of sulphuric acid and hydrogen peroxide and with the help of abrasion process. Finally a step of washing and drying completes the required window in the oxide layer. The fig.30 below shows the silicon wafer ready for next diffusion. For Positive photoresists: using Acetone, Trichloroethylene (TCE) and Phenol-based strippers (Indus-Ri-Chem J-100). For Negative photoresists: using Methyl ethyl ketone (MEK), $CH_3COC_2H_5$, Methyl isobutyl ketone (MIBK), $CH_3COC_4H_9$ and Plasma etching with O_2 (ashing) is also effective for removing organic polymer debris [37].

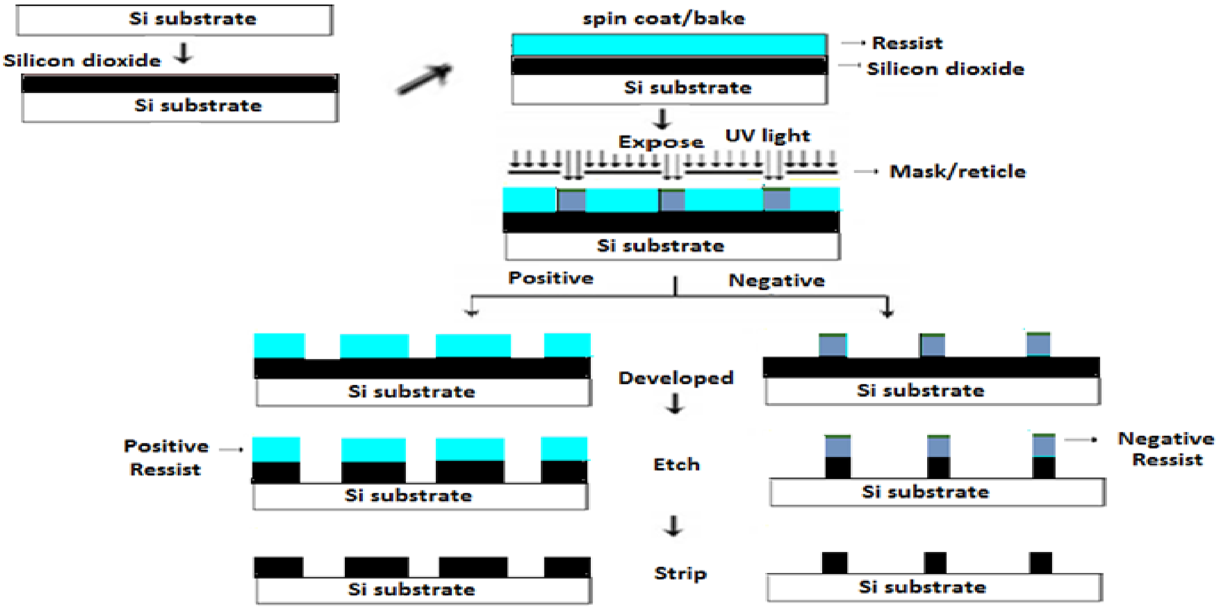


Figure 30 Negative and positive photoresist (tone) (Photolithography process).

Diffusion and Metal Deposition

A concentration gradient will cause a force to redistribute particles until there is no concentration gradient. At elevated temperatures impurity atoms move around the lattice in a random series of jumps. The process of junction formation that is transition from p to n type or vice versa, is typically accomplished by the process of diffusing the appropriate dopant impurities in a high temperature furnace. Impurity atoms are introduced onto the surface of a silicon wafer and diffuse into the lattice because of their tendency to move from regions of high to low concentration. Diffusion of impurity atoms into silicon crystal takes place only at elevated temperature, typically 900 to 1100°C [37].

Metal deposition is used to create a thin layer of metal on the exposed surface of the sample. There are two main types of metal deposition: evaporation and sputtering. Evaporation applies a non-conformal layer of the chosen metal or metals straight down on to the sample. Sputtering of metal is more conformal and therefore has better step coverage due to the wider range of delivery angles of the metal atoms [38].

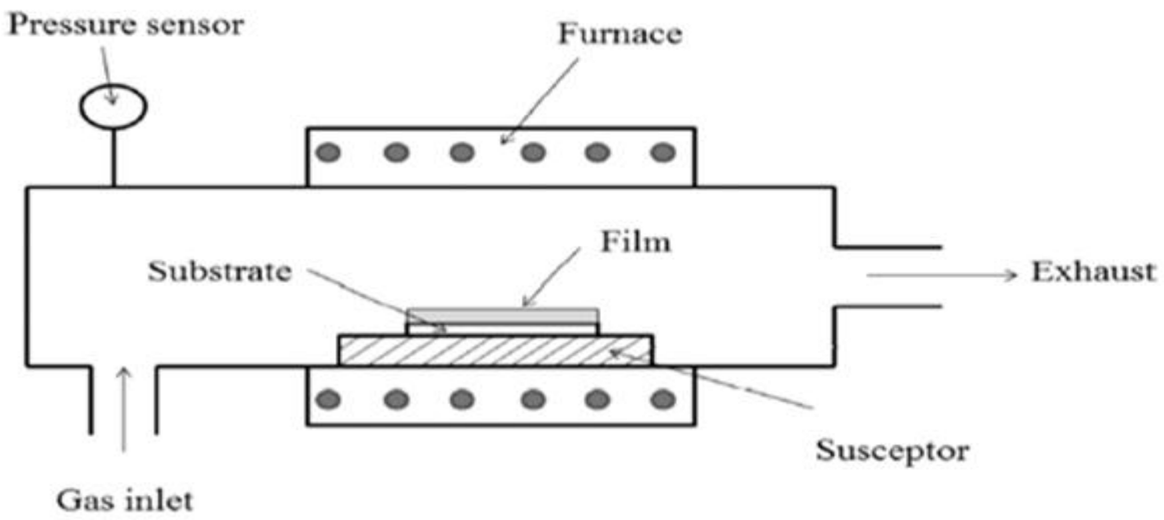


Figure 31 Schematic diagram of typical thin film deposition [38].

3.2 Integrated Circuit

3.2.1 Hybrid-Integrated Circuit

hybrid is a miniaturized electronic circuit constructed of individual devices, such as semiconductor active devices (e.g. transistors and diodes) and passive components (e.g. resistors, inductors, transformers, and capacitors), bonded to a substrate or printed circuit board (PCB) to form an electronic module.

3.2.2 Monolithic-Integrated Circuit

The word 'monolithic' comes from the Greek words 'monos' and 'lithos' which means 'single' and 'stone'. As the name suggests, monolithic IC's refer to a single stone or a single crystal. The single crystal refers to a single chip of silicon as the semiconductor material, on top of which all the active and passive components needed are interconnected and are formed simultaneously by a diffusion process. The comparative advantage of monolithic over discrete and hybrid are listed below. This is the best mode of manufacturing IC as they can be made identical, and produces high reliability. The cost factor is also low and can be manufactured in bulk in very less time. Increase in transistor density as predicted by Moore's law is due to constant reduction of physical MOS device dimensions that has helped improve design performance. Traditional benefits of scaling include (i) Integration: chip area decreases thus enabling higher transistor density and cheaper ICs (ii) Performance: chip frequency doubles with reduction in feature length every technology generation, and (iii) Power: chip supply voltage is reduced and hence power consumption decreases [39].

3.2.2.1 Electronics IC fabrication

Production of Czochralski silicon

High-purity, semiconductor-grade silicon (only a few parts per million of impurities) is melted in a crucible at 1425 degree Celsius, usually made of quartz. Dopant impurity atoms such as boron or phosphorus can be added to the molten silicon in precise amounts to dope the silicon, thus changing it into p-type or n-type silicon, with different electronic properties. A precisely oriented rod-mounted seed crystal is dipped into the molten silicon. The seed crystal's rod is slowly pulled upwards and rotated simultaneously. By precisely controlling the temperature gradients, rate of pulling and speed of rotation, it is possible to extract a large, single-crystal, cylindrical ingot from the melt [40].

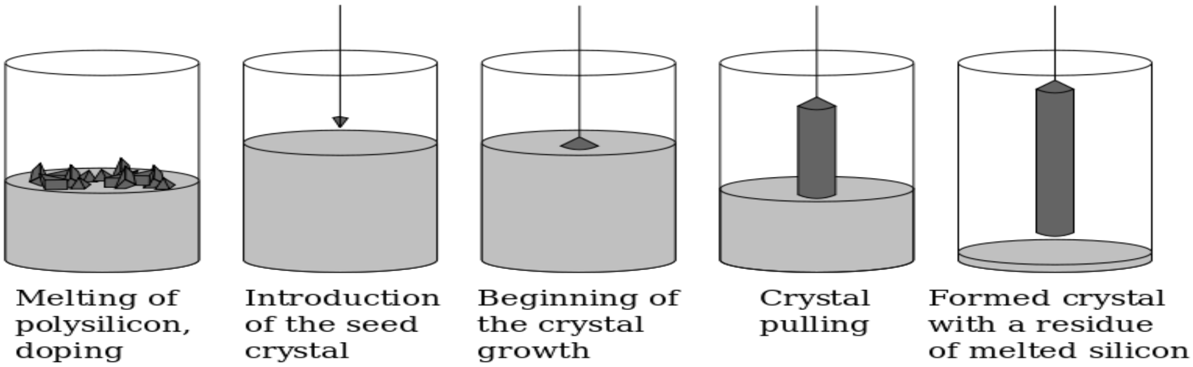


Figure 32 Silicon purification and crystal formation by the Czochralski process [40].

Figure 33 Crystal of Czochralski grown silicon [40].

An integrated circuit consists of a number of circuit components (e.g. transistors, diodes, resistors etc.) and their inter connections in a single small package to perform a complete electronic function. These components are formed and connected within a small chip of semiconductor material. The basic production processes for the monolithic ICs are as follow:

p-Substrate. This is the first step in the making of an IC. A cylindrical p-type silicon crystal is grown having typical dimensions 25 cm long and 2.5 cm diameter [See Fig.34 below (i)] the crystal is then cut by a diamond saw into many thin wafers like Fig.34 (ii), the typical thickness of the wafer being 200 µm. One side of wafer is polished to get rid of surface imperfections. This wafer is called the substrate. The ICs are produced on this wafer [41].

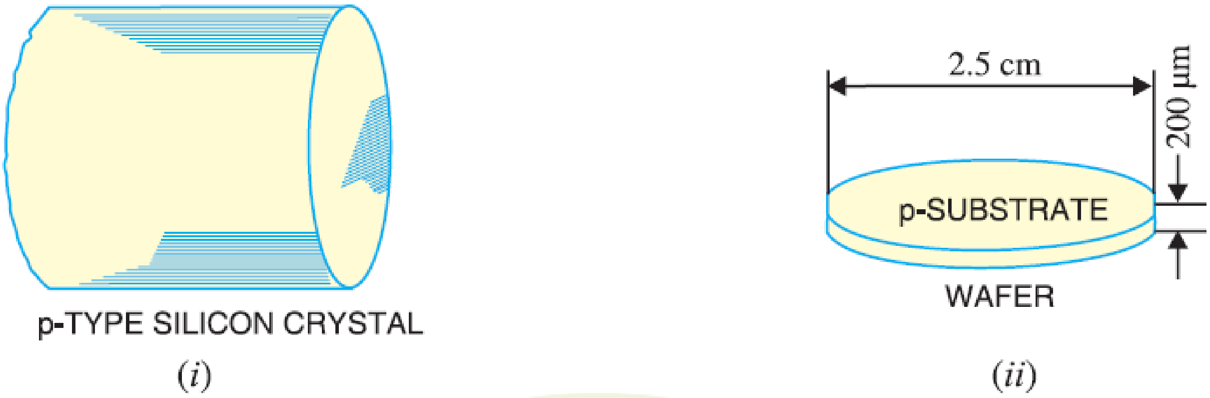


Figure 34 Silicon wafer preparation [41].

Epitaxial n- Layer. Epitaxy refers to the deposition or growth of a single crystal film on top of a crystalline substrate. The overlayer is called an epitaxial film or epitaxial layer. The term epitaxy comes from the Greek roots 'epi', meaning "above", and 'taxis', meaning "an ordered manner". The next step is to put the wafers in a diffusion furnace. A gas mixture of silicon atoms and pentavalent atoms is passed over the wafers. This forms a thin layer of n-type semi-conductor on the heated surface of substrate [See Fig.35 below (i)]. This thin layer is called the epitaxial layer and is about 10 µm thick. It is in this layer that the whole integrated circuit is formed [41].

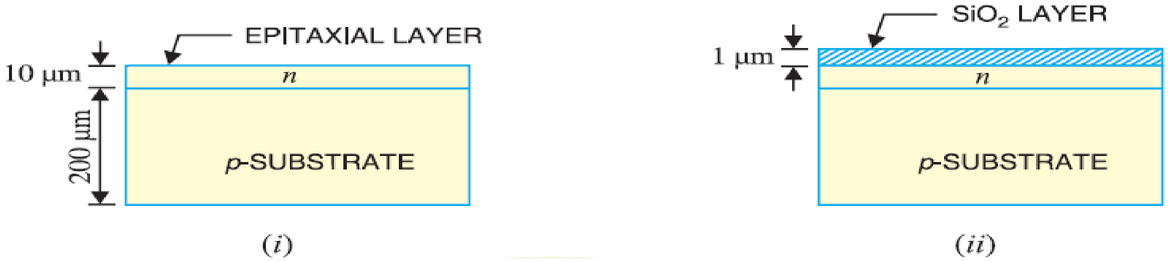


Figure 35 Process of epitaxy n-layer [41].

Insulating layer. In order to prevent the contamination of the epitaxial layer, a thin SiO_2 layer about 1µm thick is deposited over the entire surface as shown in Fig.35 (ii). This is achieved by deposited passing pure oxygen over the epitaxial layer. The oxygen atoms combine with silicon atoms to form a layer of silicon dioxide (SiO_2).

Producing components. By the process of diffusion, appropriate materials are added to the substrate at specific locations to produce diodes, transistors, resistors and capacitors. The production of these components on the wafer is discussed below.

Etching. Before any impurity is added to the substrate, the oxide layer (i.e. SiO_2 layer) is etched. The process of etching exposes the epitaxial layer and permits the production of desired components. The terminals are processed by etching the oxide layer at the desired locations.

Chips. In practice, the wafer shown in Fig.36 below is divided into a large number of areas. Each of these areas will be a separate chip. The manufacturer produces hundreds of alike ICs on the wafer over each area. To separate the individual ICs, the wafer is divided into small chips by a process similar to glass cutting [41].

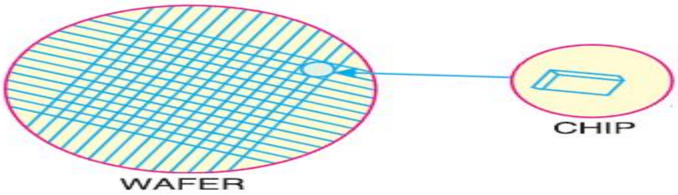


Figure 36 Silicon wafer divided in to chips [41].

It may be seen that hundreds of alike ICs can be produced from a small wafer. This simultaneous mass production is the reason for the low cost of integrated circuits. After the chip is cut, it is bonded to its mounting and connections are made between the IC and external leads. The IC is then encapsulated to prevent it from becoming contaminated by the surrounding atmosphere.

Fabrication of Components on Monolithic IC

The notable feature of an IC is that it comprises a number of circuit elements inseparably associated in a single small package to perform a complete electronic function.

This differs from discrete assembly where separately manufactured components are joined by wires. We shall now see how various circuit elements (e.g. diodes, transistors, resistors etc.) can be constructed in an IC form.

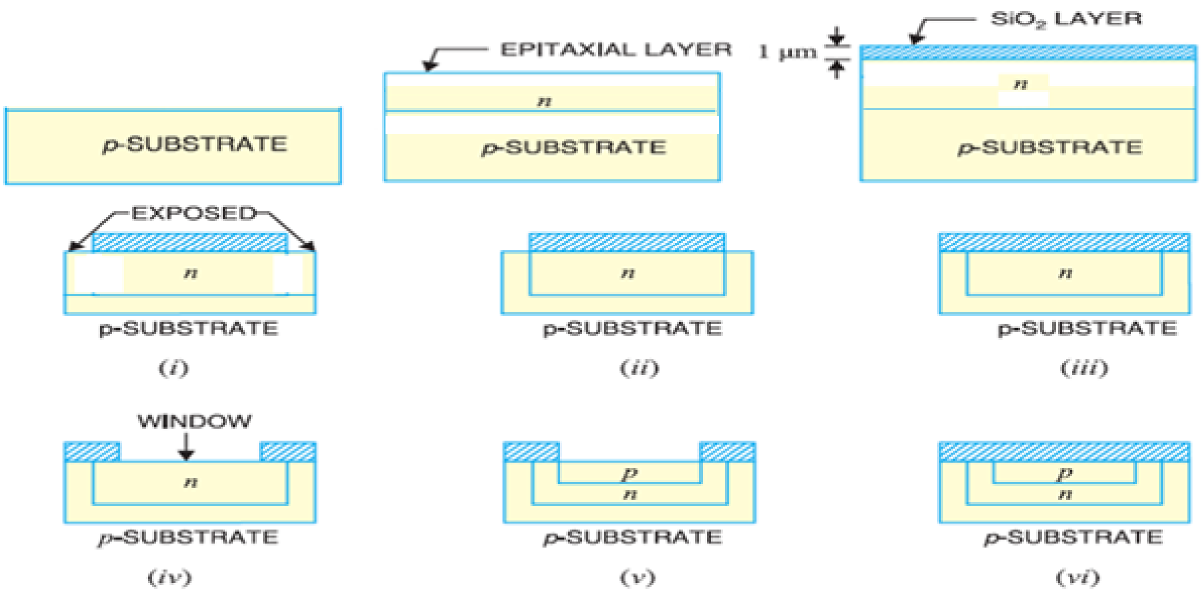


Figure 37 Fabrication of components [41].

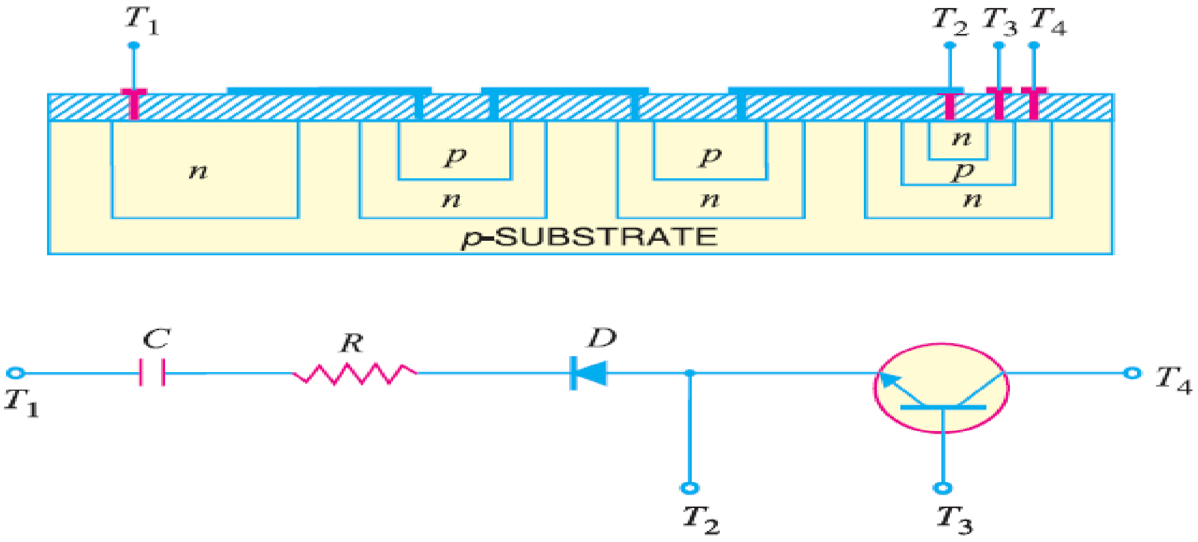


Figure 38 Fabrication of Monolithic [41].

3.2.2.2 Photonic IC fabrication

Waveguide

The technology required to fabricate planar light wave circuit components of such dimensions is therefore common in the well-established Micro-electronic technology, using the tools and techniques of the semiconductor industry. In a waveguide light is trapped by total internal reflection in a film, and therefore the film must have a refractive index greater than the refractive indices corresponding to the upper and lower media. These are usually referred to as the cover and the substrate, respectively, and the film is called the core (silicon), because that is where most of the optical energy is concentrated. The central region of the optical fiber or core (silicon) is surrounded by a material called cladding (silicon dioxide). Of course, the core must have a higher refractive index than the cladding in order to trap light within the structure after total internal reflection. Light beam can propagate along a layer of material between two different media. The cladding of the Optical waveguides can be readily fabricated from SOI wafers or air [42] and [43].

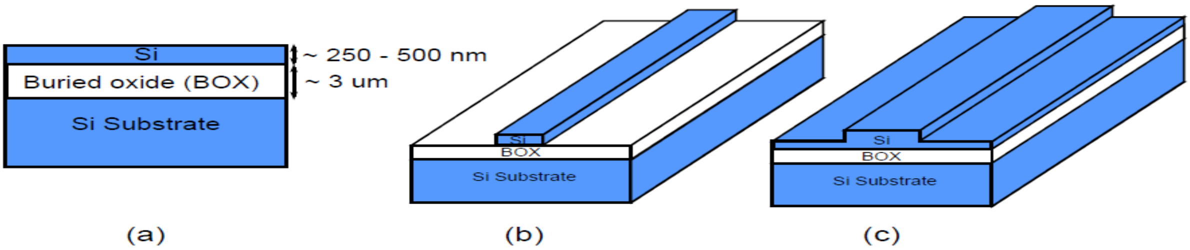


Figure 39 (a) SOI stack (b) Strip waveguide (c) Rib waveguide air [43].

Laser, Detector and Modulator

They demonstrated a prototype of the single-chip photonic TRx based on a bulk silicon substrate for λ ~ 850 nm optical interconnects at high data rates, proving that this approach can offer compact low-cost I/O solutions for electronic-photonic integration [44].

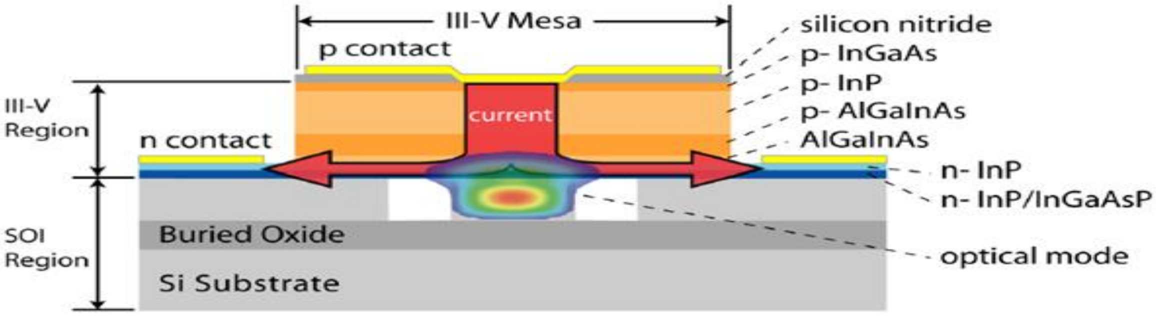


Figure 40 Device cross section for the electrically pumped silicon evanescent pulsed Laser [44].

III-V Lasers on Si Direct gap semiconductors have demonstrated that they can be used to produce efficient electrically pumped lasers. The vast majority of semiconductor lasers are of this type. Direct gap III-V materials can be directly grown on Si but the large lattice mismatch results in misfits and dislocations which increase optical loss. An alternative is to grow the III-V materials on a lattice matched SiGe alloy buffer grown on Si. Realizing a compact chip-level light source is a serious issue for practical implementation of a silicon photonic I/O scheme on a silicon electronic chip [45].

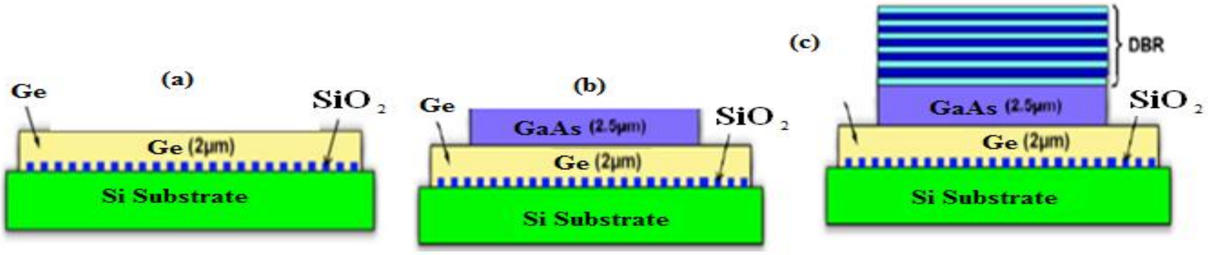


Figure 41 Integrated photonics (a) Detector Ge (b) Detector GaAs (c) Laser [45].

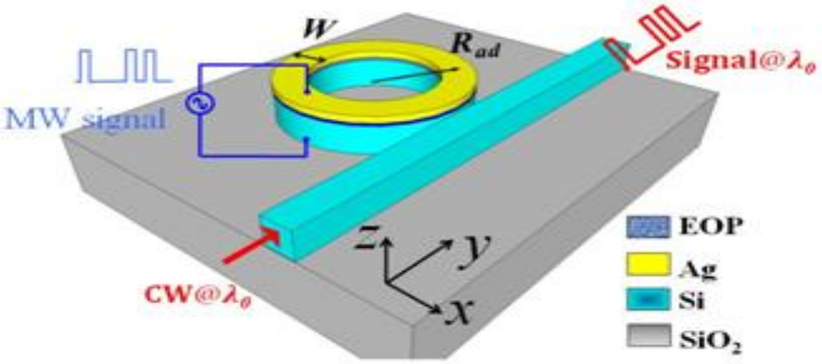


Figure 42 Electro-optic polymer modulator (plasmonic micro-ring resonator) Si waveguide [17].

CHAPTER 4: RESULT AND DISCUSSION

The first experimental set up was held at Physics Department (Optics Laboratory). The main reason of the experimental set up in physics department was: first, in optics laboratory, there were similar cross sectional area having different sizes of glass rods (30, 10 & 5 cm). Voltage and current output from the system of electrophotonic interconnects was measured using these glasses. Second, there were different shapes of glasses like prism, rectangular, triangular, semi-circular, circular and curved gasses in the optics laboratory. So the path of laser light ray was demonstrated by propagated in any direction like in straight line or in curved path using these different shapes of glasses based on total internal reflection. So this experimental set up has shown and proved that laser light was led to any interest of direction of propagation path by using different optical devices.

The second experimental set up was held at Electrical and Computer Engineering (Applied Electronics Laboratory). All electronic and photonic devices including power supply, dual channel oscilloscope, optical (laser and detector) and other materials were found in school of electrical and computer engineering (AAIT) laboratory for delay and power measurement. And different diameters of waveguides (glass rods) that were gathered from chemistry department (arat kilo), chemical and environmental engineering (amst kilo).

4.1 Output Voltage and Current Measurements from systems

Figure 43 (a) full experimental set up (b) laser light source (c) laser detector.

In the fig.43 shown that (a) full experimental contained (i) dual channel oscilloscope used to measure delay in both interconnect (ii) DC power supply to modulate the modulator ((v) 555 based oscillator circuit built on breadboard) (iii) multi meter used to measure voltage and current (iv) laser light source (v) breadboard contained 555 timer IC and other electronic components used to modulate the continuous laser light to optical pulses at a frequency of (50, 75 & 100)KHz (vi) detector that convert the optical pulse to equivalent electrical pulse (vii) different diameters of glass rods and Cu wires for interconnecting input and output ports. (b) Laser source that used to emitted light when DC power is ON. (c) Detector that detects light and converts to electrical signal.

For both interconnects the supplied voltage and current were equal for both interconnects and written as voltage input to laser $V_L(V)$ or $V_{IN}(V)$ and current input to laser $I_L(A)$ or $I_{IN}(A)$. After some voltage drop and consuming current in the system, the output voltage and current was obtained as system generated $V_{OUT}(V)$ and $I_{OUT}(A)$.

a b

Figure 44 (a) Three glass rods having length of (5, 10 & 30) cm (b) three Cu wires having length of (5, 10 & 30) cm

In fig.44 (a) three glass rods having similar diameter of 1cm but different lengths of (5, 10 & 30) cm (b) three Cu wires having similar diameter of 1mm but different lengths (5, 10 & 30) cm. These glass rods and Cu wires were placed into corresponding interconnects as shown in fig.11 at a time and then the measured voltage and current at the output of both circuits were recorded as shown in the following tables.

Table 2 Voltage and Current output from integrated Electrophotonic Interconnect.

Waveguide Length(cm)	$V_L (V)$	$I_L (A)$	$V_{OUT} (V)$	$I_{OUT} (A)$
30	5.51	0.25	3.15	0.1
10	5.51	0.25	3.85	0.15
5	5.51	0.25	4.35	0.19

Table 3 Voltage and Current output from Electronic Interconnect.

Copper Wire Length(cm)	$V_{IN} (V)$	$I_{IN} (A)$	$V_{OUT} (V)$	$I_{OUT} (A)$
30	5.51	0.25	2.01	0.05
10	5.51	0.25	3.25	0.1
5	5.51	0.25	4.15	0.12

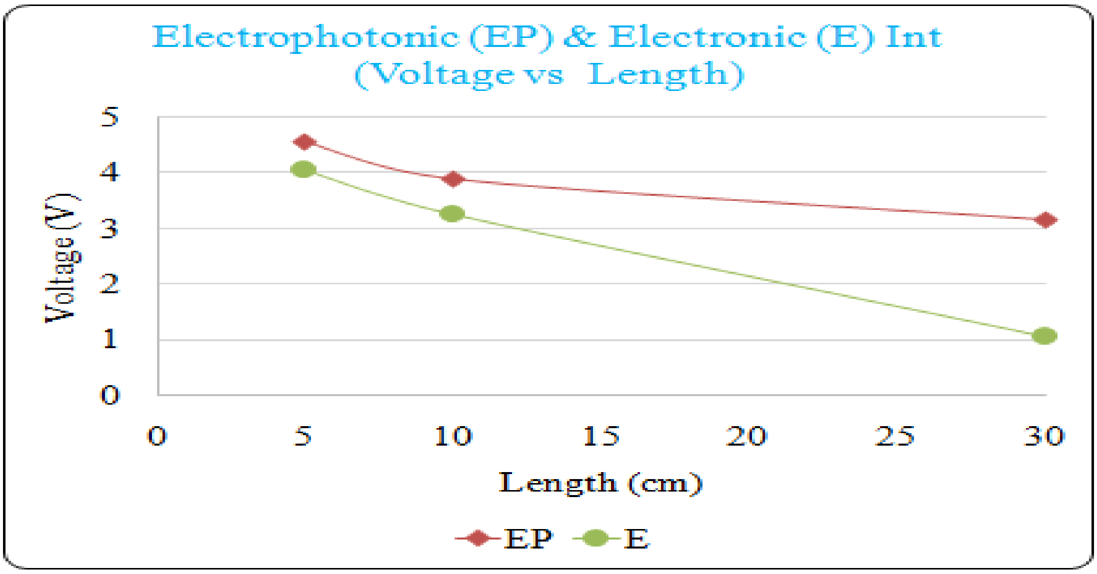


Figure 45 Electrophotonic (EP) and Electronic (E) Interconnect (Int) of the system output Voltage.

The voltage obtained at the output port in electrophotonic was greater than the electronic interconnect at different lengths but at equal inputs of V & I. This shown that in electronic (Cu wire) interconnect was more voltage drop due to metal resistive wire. Whereas on electrophotonic interconnect obtained more voltage at the output port at equal inputs of V & I in the input port due to the absence of resistive material in the glass rod to drop voltage. Therefore, as depicted from the fig.45 at all level of lengths the voltage obtained from the system at equal input in electrophotonic was higher than copper interconnecting. This means the electrophotonic interconnect is lossless than electronic circuit.

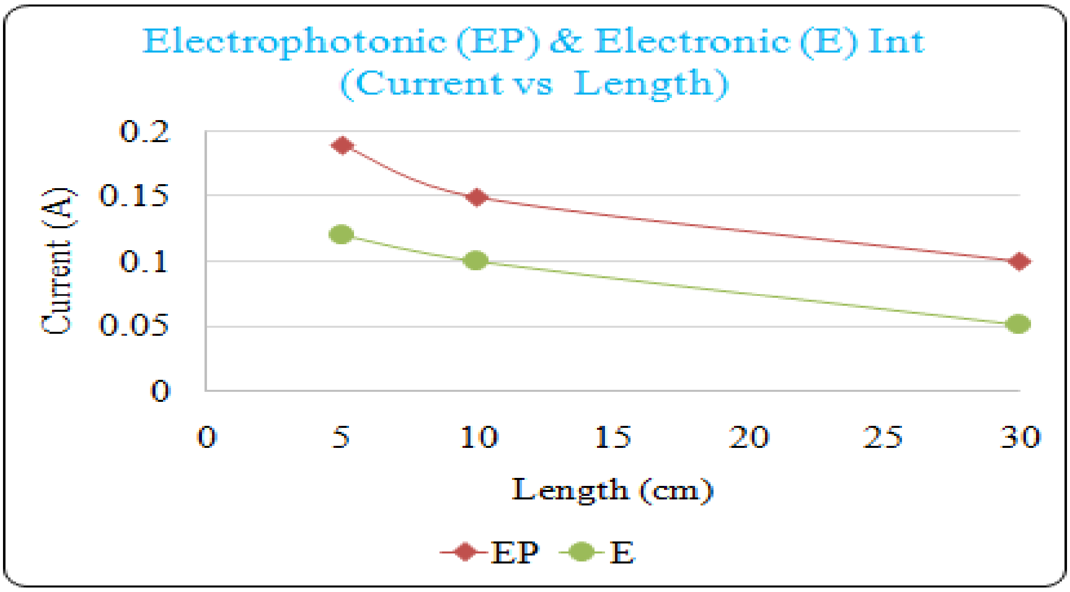


Figure 46 Electrophotonic (EP) and Electronic (E) Interconnect (Int) of the system output Current.

Similarly in fig.46 for current output from the system was higher in electrophotonic interconnect. That means current obtained (output) measured at the final circuit in the integrated electrophotonic interconnect was greater than the electronic interconnect at equal inputs. This shown that in the electronic circuit current was consumed more than in electrophotonic interconnect due to the resistance in the copper wire.

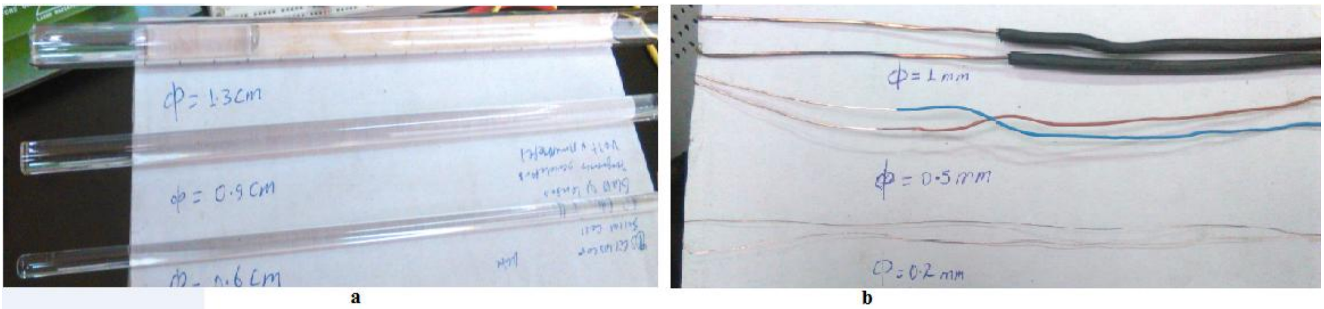


Figure 47 Three 25 cm long (a) glass rods (6, 9 &13) mm (b) Cu wires (0.2, 0.5 & 1) mm.

In fig.47 (a) three glass rods length of 25cm having different diameters ϕ (6, 9 &13) mm (b) three Cu wires length of 25cm having different diameters ϕ (0.2, 0.5 & 1) mm. The delay measurement in oscilloscope is hard with naked eye due to fast sweeping at higher clock frequencies. But by taking video or picture by camera, it is easy to measure the delay at both interconnects by taking the difference of the two channels as shown in fig.48 (b).

4.2 Delay

In order to compare delay of both interconnects, connect both interconnects (waveguide & Cu wires) in fig.47 in to circuits of interconnects in fig.12 and then the following tables were recorded.

Figure 48 Oscilloscope (a) dual channel zero reading (b) reading after input and output were connected.

To measure delay in the system, first connect channel one to input and channel two to the output of interconnects. And set the dual channel to zero reading as shown in fig.48 (a) by setting OFF input. Then as the input is ON, the input and output channel were swept as seen in shown in gig.48 (b). The input (the upper channel) led the output (lower reading) by a length of grid divisions. By counting number of grids (divisions) that the input leads the output and changing this screen length in to time by multiplying the scale to determine the delay in the interconnect. Based on this the following tables were filled.

Table 4 Electrophotonic interconnects Delay in a 25 cm long at 50 KHz.

Diameter $\phi(mm)$	13	9	6
Delay $\tau(\mu s)$	0.852	0.852	0.852

Table 5 Electronic interconnect Delay in a 25 cm long at 50 KHz.

Diameter $\phi(mm)$	1	0.5	0.2
Delay $\tau(\mu s)$	0.891	1.202	2.853

Table 6 Electrophotonic interconnects Delay in a 25 cm long at 75 KHz.

Diameter $\phi(mm)$	13	9	6
Delay $\tau(\mu s)$	0.634	0.634	0.634

Table 7 Electronic interconnects Delay in a 25 cm long at 75 KHz.

Diameter $\phi(mm)$	1	0.5	0.2
Delay $\tau(\mu s)$	1.881	2.352	3.871

Table 8 Electrophotonic interconnects Delay in a 25 cm long at 100 KHz.

Diameter $\phi(mm)$	13	9	6
Delay $\tau(\mu s)$	0.309	0.309	0.309

Table 9 Electronic interconnects Delay in a 25 cm long at 100 KHz.

Diameter $\phi(mm)$	1	0.5	0.2
Delay $\tau(\mu s)$	2.512	3.385	4.745

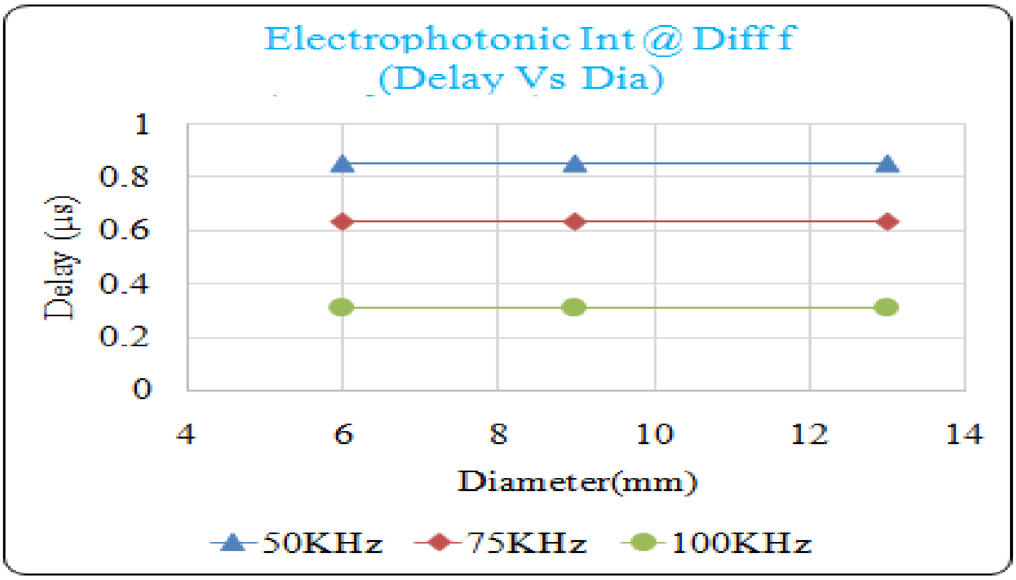


Figure 49 Electrophotonic Interconnect (Int) at different (Diff) frequency (f) (Delay Vs Diameter).

The delay remained constant at different cross sectional area of waveguide (glass rod) in electrophotonic interconnects. But as clock frequency increased, the delay reduced since electrophotonics is free of RC delay and speed is proportional to clock f.

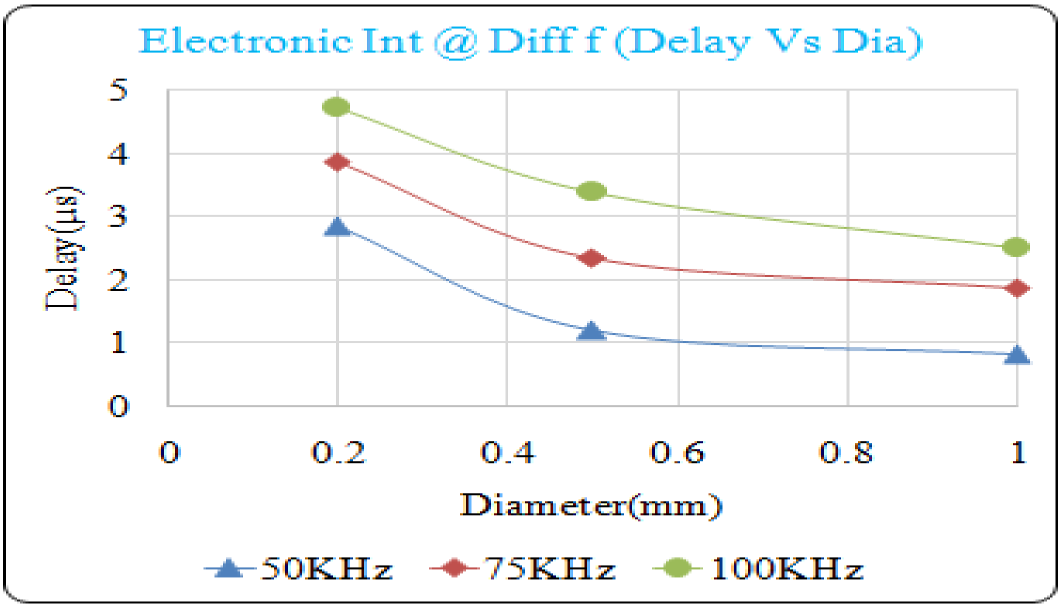


Figure 50 Electronic interconnect (Int) at different (Diff) frequency (f) (Delay Vs Diameter).

The delay increased as cross section of Cu wire get decreased and clock f increased since RC delay is increased with both thickness and f in electronic interconnect. The delay of the integrated electrophotonic interconnect was lowered as increased clock frequency. In contrast, the delay of the conventional copper interconnect was slowly increased both as scaling down of Cu wire and increased clock frequency due to proportionally increased in resistance. The delay measured in the integrated electrophotonic interconnects at different cross sectional area had constant value. Because the dimension of waveguide does not affect delay in electrophotonic interconnect. While delay in the copper interconnect varied both with dimension and clock frequency. The oscillation of electrons in copper wire is always increased with clock frequency and scaling down of Cu wire. Hence, friction of electrons in the wire leading to heating that caused to increase resistance of the wire. This again led increased the delay associated with capacitive effect of the dielectric material (increased in RC delay) in electronic circuit.

Table 10 Electrophotonic interconnects Delay verses frequency at Diameters (13, 9, 6) mm.

Frequency $f(KHz)$	50	75	100
Delay $\tau(\mu s)$	0.852	0.634	0.309

Table 11 Electronic interconnect Delay verses frequency at Diameter 1mm.

Frequency $f(KHz)$	50	75	100
Delay $\tau(\mu s)$	0.891	1.381	2.512

Table 12 Copper interconnect Delay verses frequency at Diameter 0.5mm.

Frequency $f(KHz)$	50	75	100
Delay $\tau(\mu s)$	1.202	2.352	3.385

Table 13 Copper interconnect Delay verses frequency at Diameter 0.2mm.

Frequency $f(KHz)$	50	75	100
Delay $\tau(\mu s)$	2.853	3.871	4.745

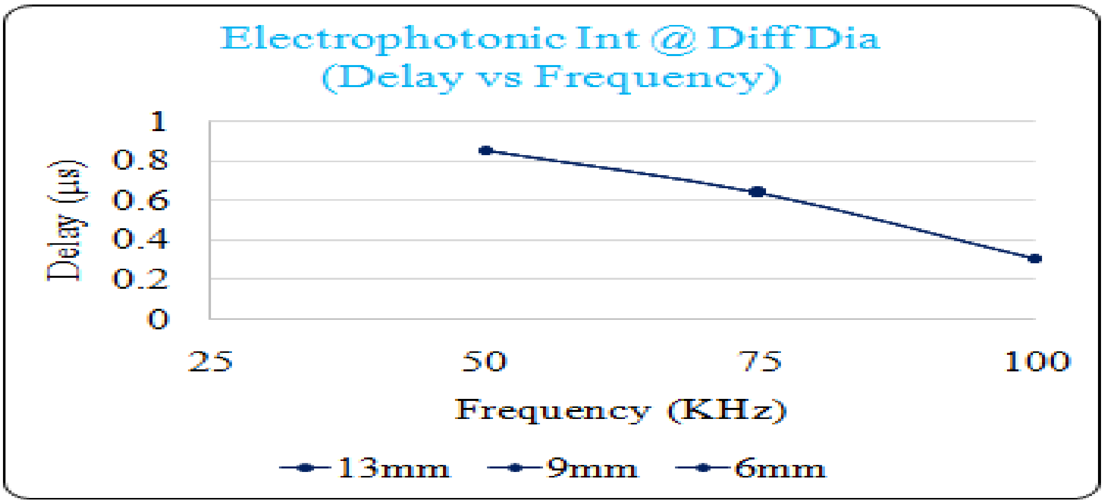


Figure 51 Electrophotonic Interconnect (Int) at different(Diff) diameter (Dia) overlap at one line (Delay Vs Frequency).

As we have seen above in electrophotonic interconnect delay depends only with clock f not on the cross sectional area of waveguide. At different diameter the data is similar but as increased in clock f the delay became reduced.

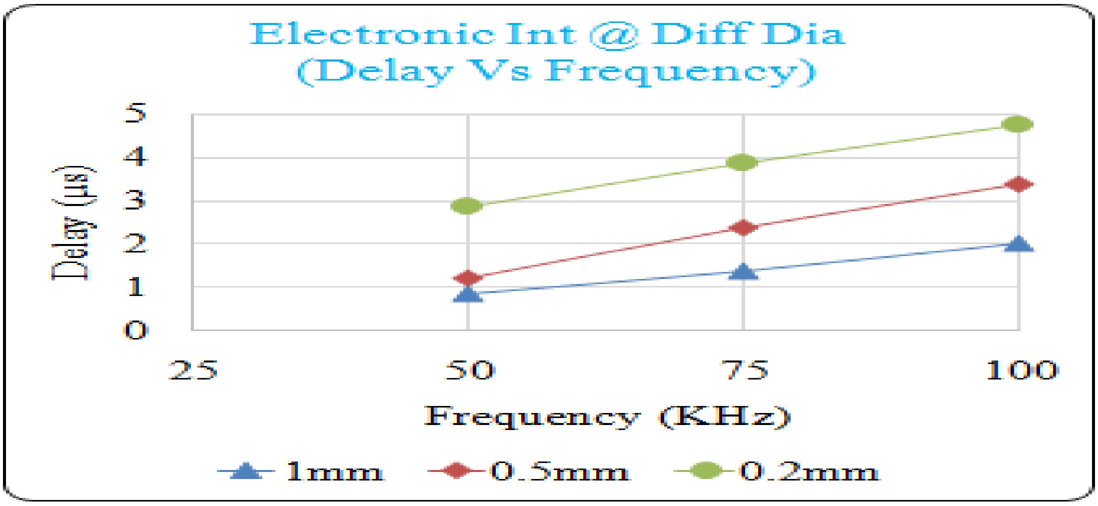


Figure 52 Electronic Interconnect (Int) at different (Diff) diameter (Dia) (Delay Vs Frequency).

In electronic interconnect delay increased as both scale down the diameter of Cu wire and clock frequency increased. This became due to increased in frequency and reduced in diameter of wire increased resistance of the wire that led to increased RC delay on the circuit.

Table 14 Delay compared electrophotonic and electronic interconnect.

Frequency & Length	@ 50kHz			@75kHz			@100kHz		
	Length (25 cm)			Length (25 cm)			Length (25 cm)		
Components	ϕ@ 13mm	ϕ@ 9mm	ϕ@ 6mm	ϕ@ 13mm	ϕ@ 9mm	ϕ@ 6mm	ϕ@ 13mm	ϕ@ 9mm	ϕ@ 6mm
Electrophotonic(μs)	0.831	0.831	0.831	0.634	0.634	0.634	0.309	0.309	0.309

Frequency & Length	@ 50kHz			@75kHz			@100kHz		
	Length (25 cm)			Length (25 cm)			Length (25 cm)		
Components	ϕ@ 1mm	ϕ@ 0.5mm	ϕ@ 0.2mm	ϕ@ 1mm	ϕ@ 0.5mm	ϕ@ 0.2mm	ϕ@ 1mm	ϕ@ 0.5mm	ϕ@ 0.2mm
Electronic(μs)	0.831	1.202	2.853	1.881	2.232	3.871	2.512	3.385	4.745

Table 15 Average Delay compared Electrophotonic and electronic interconnect (Int).

Frequency $f\,(KHz)$	**50**	**75**	**100**
Electrophotonics $\tau(\mu s)$	0.852	0.634	0.309
Electronic $\tau(\mu s)$	1.679	2.661	3.547

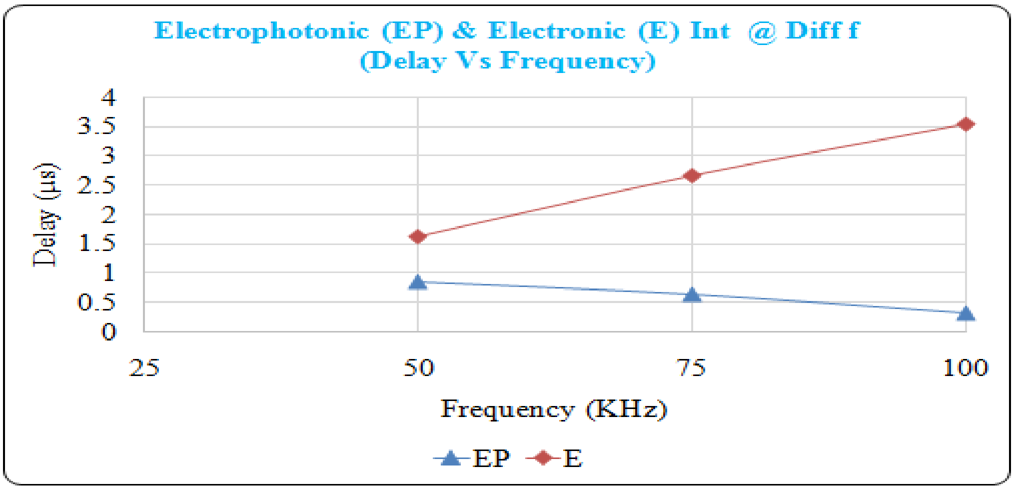


Figure 53 performance comparison of Electrophotonic (EP) and Electronic (E) Int (Delay Vs Frequency).

To compare both interconnects at similar platform; as clock f increased delay increased in electronic while decreased on electrophotonic interconnect. The delay on Cu wire increased with higher rate as clock f increased as shown above in fig.53. Because as clock f increased, the electrons increased in oscillation. In turn, this led to more heating on the Cu wire by increased the resistance of the wire to increased RC delay. While on the electrophotonic interconnect the delay reduced with increased clock f due to lack of RC delay in glass rods. So Delay of the electrophotonic (EP) decreased as the frequency increased. And the delay of copper interconnects increased with frequency increased caused to increased resistance. Delay on electrophotonic interconnect was lowered than electronic interconnect as interconnect scaled down. It is clear from the results that integrated electrophotonic interconnects gave better results as compared to copper interconnects in terms of delay. This shown that integrated electrophotonic interconnect is better performed than conventional interconnects.

4.3 Power dissipation

To measure power dissipation on both interconnects: connect both interconnect in fig.47 in to circuit of corresponding circuits in fig.12 and then the following tables were recorded.

Table 16 Electrophotonic interconnects Power dissipation in 25cm long at 50 KHz.

Diameter $\phi(mm)$	13	9	6
Power $p(mW)$	0.315	0.39	0.502

Table 17 Electronic interconnects Power dissipation in 25cm long at 50KHz.

Diameter $\phi(mm)$	1	0.5	0.2
Power $p(mW)$	0.55	1.12	1.75

Table 18 Electrophotonic interconnects Power dissipation in 25cm long at 75 KHz.

Diameter $\phi(mm)$	13	9	6
Power $p(mW)$	0.48	0.556	0.633

Table 19 Electronic interconnects Power dissipation in 25cm long at 75 KHz.

Diameter $\phi(mm)$	1	0.5	0.2
Power $p(mW)$	1.62	2.23	2.94

Table 20 Electrophotonic interconnects Power dissipation in 25cm long at 100 KHz.

Diameter $\phi(mm)$	13	9	6
Power $p(mW)$	0.658	0.735	0.845

Table 21 Electronic interconnects Power dissipation in 25cm long at 100 KHz.

Diameter $\phi(mm)$	1	0.5	0.2
Power $p(mW)$	2.73	3.40	4.12

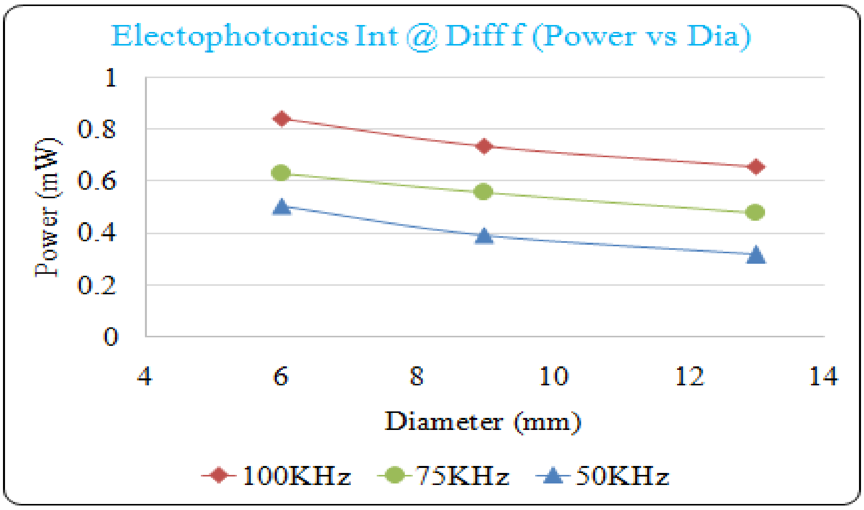


Figure 54 Electrophotonic Interconnect (Int) at different (Diff) frequency (f) (Power dissipation Vs Diameter).

Power dissipation increased as increased clock f and reduced diameter of both interconnects. The power dissipation in electrophotonic was due to the electronic parts (in laser & detector) associated in interconnect part. And the contribution of the scaling down diameter of glass rod to power dissipation was the intensity of light was reduced and led to power lost by diffraction (spread out) of light.

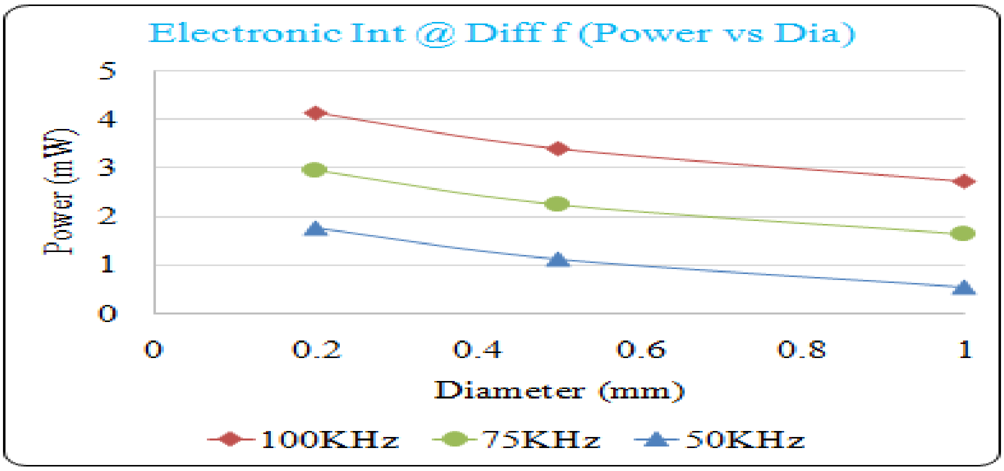


Figure 55 Electronic Interconnect (Int) at different frequency (Power dissipation Vs Diameter).

Power dissipation increased as both diameter of Cu wire reduced and clock f increased. As clock f increased and scaling down of Cu wire led increased the resistance of the wires. Thereby increased the power dissipation (in the form of heat) on interconnects.

Table 22 Electrophotonic interconnects at Diameter 13mm.

Frequency $f\,(KHz)$	50	75	100
Power $p(mW)$	0.315	0.48	0.658

Table 23 Electronic interconnect at Diameter 1mm.

Frequency $f\,(KHz)$	50	75	100
Power $p(mW)$	0.55	1.62	2.73

Table 24 Electrophotonic interconnect at Diameter 9mm.

Frequency $f\,(KHz)$	50	75	100
Power $p(mW)$	0.39	0.556	0.735

Table 25 Electronic interconnect at Diameter 0.5mm.

Frequency $f\,(KHz)$	50	75	100
Power $p(mW)$	1.12	2.23	3.40

Table 26 Electrophotonic interconnect at Diameter 6mm.

Frequency $f\,(KHz)$	50	75	100
Power $p(mW)$	0.502	0.633	0.845

Table 27 Electronic interconnect at Diameter 0.2mm.

Frequency $f\,(KHz)$	50	75	100
Power $p(mW)$	1.73	2.94	4.12

As shown below in fig.56 & 57, power dissipation on electrophotonic interconnects was increased as reduced diameter (diffraction of light) and increased clock f. Power dissipation increased on electronic interconnect was also due to reduced of diameter of the wire and increased clock frequency.

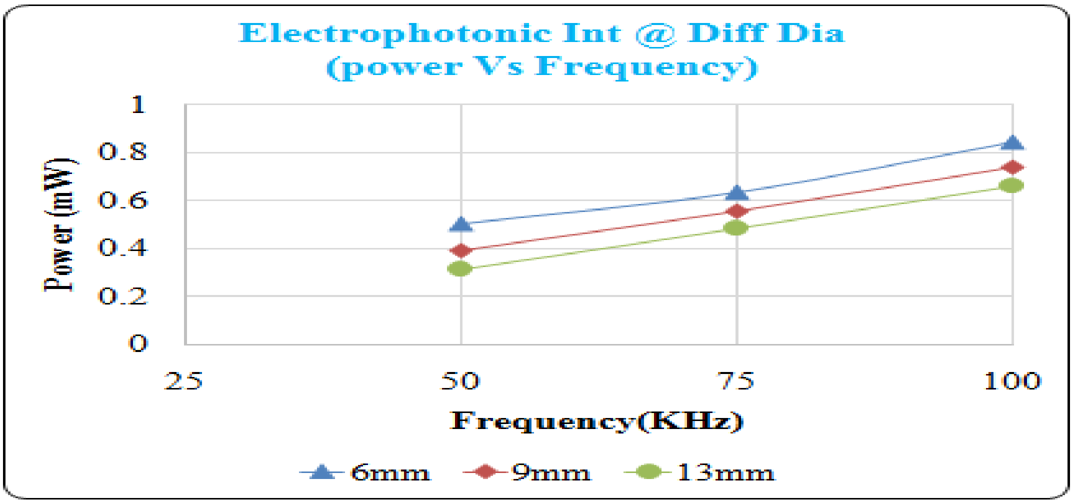


Figure 56 Electrophotonic Interconnect (Int) at different diameter (Power dissipation Vs Frequency).

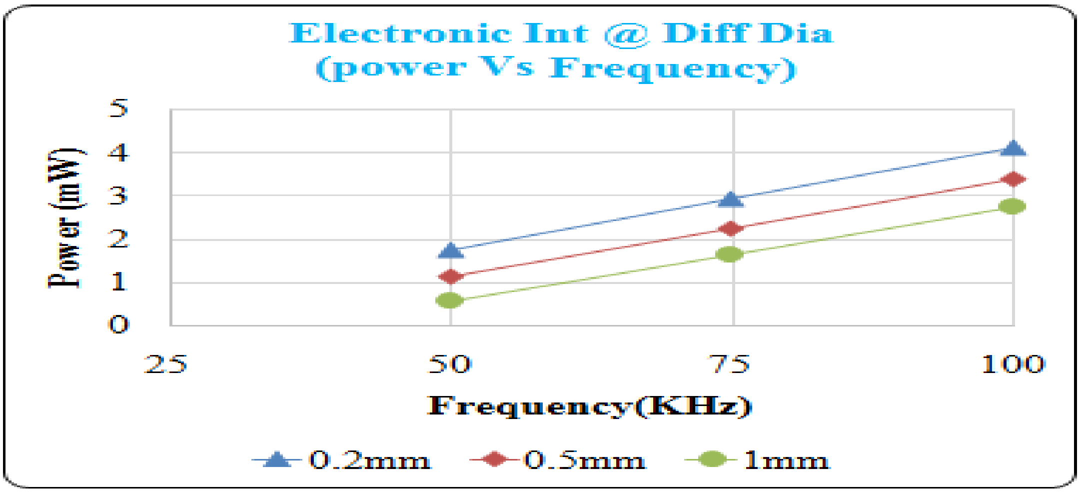


Figure 57 Electronic Interconnect (Int) at different (diff) diameter (dia) (Power dissipation Vs Frequency).

Table 28 Power dissipation compared Electrophotonics with Electronic interconnects.

Frequency & Length Components	@ 50kHz			@75kHz			@100kHz		
	Length (25 cm)			Length (25 cm)			Length (25 cm)		
	ϕ@ 13mm	ϕ@ 9mm	ϕ@ 6mm	ϕ@ 13mm	ϕ@ 9mm	ϕ@ 6mm	ϕ@ 13mm	ϕ@ 9mm	ϕ@ 6mm
Electrophotonic P(mw)	0.315	0.39	0.502	0.48	0.556	0.633	0.658	0.735	0.845

Frequency & Length Components	@ 50kHz			@75kHz			@100kHz		
	Length (25 cm)			Length (25 cm)			Length (25 cm)		
	ϕ@ 1mm	ϕ@ 0.5mm	ϕ@ 0.2mm	ϕ@ 1mm	ϕ@ 0.5mm	ϕ@ 0.2mm	ϕ@ 1mm	ϕ@ 0.5mm	ϕ@ 0.2mm
Electronic p(mw)	0.55	1.12	1.75	1.62	2.23	2.94	2.73	3.40	4.12

Table 29 Comparison of Electrophotonic and Electronic interconnects (Int) (Power Vs Frequency).

Frequency $f\,(KHz)$	**50**	**75**	**100**
Electrophotonic $p(mW)$	0.402	0.556	0.746
Electronic $p(mW)$	1.140	2.263	3.417

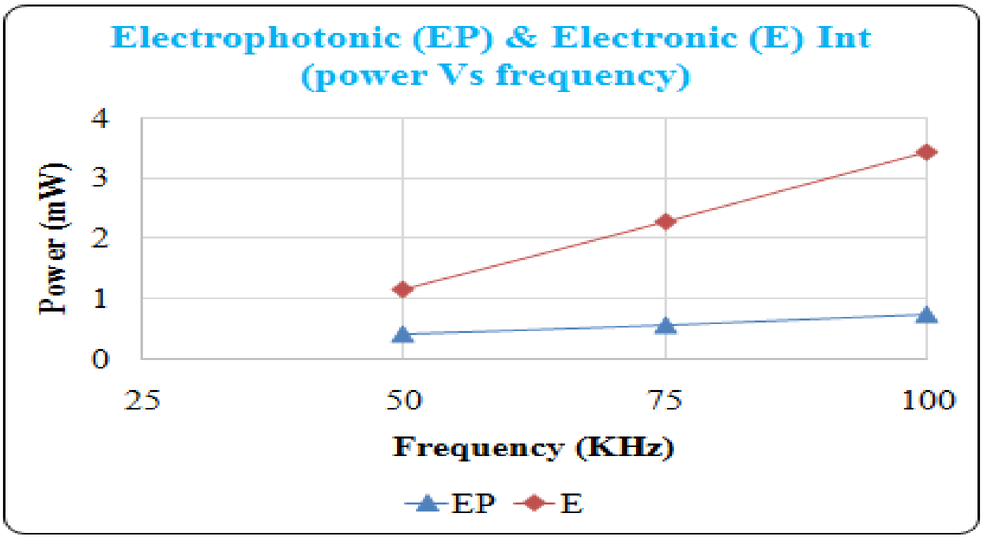


Figure 58Performance comparison of Electrophotonic (EP) and Electronic (E) interconnect (Int) (Power Vs Frequency).

The power dissipation of both interconnects were increased as clock f increased and scaled down of both interconnects. But the rate of increment was higher on electronic (Cu wire) due to increased clock f and reduced in diameter Cu. So the increment in resistance of the wire made electronic circuit to dissipated more power in the form of heat than the glass rod. So the power dissipation on electronic interconnects was higher with larger rate than electrophotonic. Because scaled down of cross sectional area (diameter) of Cu wire and increased clock frequency led to increased more leakage Current in copper wire. But the power dissipation in electrophotonic interconnects was less than electronic interconnect at any levels of frequency. This shown that electrophotonic was more efficient than electronic interconnects. Therefore, Electrophotonic interconnects gave better performance in terms of power as compared to conventional electronic interconnects at any level of operating clock frequency.

CHAPTER 5: CONCLUSION AND RECOMMENDATION FOR FUTUR WORK

5.1 Conclusion

Data transport across electrical wires is limited by bandwidth, crosstalk, delay and power dissipation (heat), which creates a performance bottleneck for semiconductor microchips in modern computer systems from mobile phones to large-scale data centers. Copper based interconnects are also facing many challenges like dispersion, reflections, ringing and frequency dependent attenuation in high speed signal. The performance of parallel links in conventional devices is also limited by the cross talk due to coupling from neighboring signals. Copper interconnects are responsible for 70 to 80% of the signal delay in high-speed systems at deep submicron technology.

These limitations can be overcome by using optical communications based on chip-scale electronic–photonic systems enabled by silicon-based photonic devices. Optical interconnects can be considered as another alternative to meet these requirements. Optical interconnect due to its high bandwidth, low signal attenuation, Low signal delay, less power dissipation and cross talk, is an ideal candidate to tackle the challenges imposed by copper interconnects for on-chip applications. So the increasing demands of silicon Photonics for bandwidth in communication systems are driving the rapid shift from electronics to photonics. Copper wires have been replaced by optical cables with shorter interconnect length, from long distance telecommunications to the rack-to-rack, even board level interconnects in high-performance computing systems. Therefore, chip-scale photonic systems become possible that on-chip optical interconnects, which visualize optics would replace electronics at all the levels in the near future. But integration of electronics and photonics is presented in this thesis as a technology of a transition from electronics to photonics for the future technology.

To solve the shortcoming of conventional electronic faced in bandwidth, power (heating), interference and speed limitations, an integrated electrophotonic (optical) interconnect is seen as a potential alternative solution since it can directly address these problems at the chip and chip-to-chip level and meet the performance requirements of current and future generation of data interconnection by replacing copper wire and using photons as information carriers. As seen from the experimental result obtained, the voltage and current measured at the final circuit for optical interconnect was larger than to the counterpart of electronic interconnect. This shows that there was voltage drop along the copper wire larger than in electrophotonic interconnect due to the resistance of Cu wire. And from the delay data obtained that the time took the photons propagated in the optical waveguide which was shorter and contributed 18.6% of the total delay and electrons in the copper wire was propagated slowly and contributed 81.4% of the total delay. This shows again the photonic interconnect has well performed in speed over the counterpart electronic interconnects. This means the delay in conventional electronics was higher than the electrophotonic interconnect by 62.8%. And the power dissipation in the copper interconnects was contributed 80%. While the electrophotonic interconnect was contributed 20% of the total dissipation in the systems. This means power dissipation in conventional electronics was higher than the electrophotonic interconnect by 60%.

Another disadvantage of electronic interconnects with large power dissipation on the copper wire leads to heating of the device that is shorten the life span of the electronic devices. Therefore, the integration of both technologies will be better than the conventional electronic (copper) interconnects for speed, power and durability of the devices. From the results shown that for future ICs fabrication, the electrophotonic interconnects has been proposed as better alternative to copper interconnects for next super computing, communicating and control systems. This thesis combined the advantages of both technology worlds i.e. photons (as information carriers) and electrons (for data processor and storage), which may potentially trigger another round of information technology revolution.

5.2 Recommendation for Future Work

Integrated electrophotonic interconnect was well performed than electronic interconnect in terms of delay and power in the experimental set up. But within the electrophotonic interconnect there were two gaps between laser light source -&- waveguide and between detector -&- waveguide. These gaps might be cause for optical losses that reduce the performance of electrophotonic interconnect as shown in the fig.59 (a). So in order to avoided these gap losses and to improved the performance at chip level more than that we have seen in the experimental set up at device level (as shown in fig. 59 (b)), a simulating or fabricating electrophotonic IC on monolithic silicon substrate is required. The main objective of this thesis was studying of integrated electronic and photonic devices on monolithic silicon substrate **at chip level.** But due to lack of simulating software or photonic laboratory the study was forced and carried out with experimental setup **at device level**. Therefore, the next duty will be simulating using software or fabricating using photonic laboratory at chip level for actual comparison of both interconnects on monolithic silicon substrate with the core parameters on similar platform as shown on fig. 59 (b).

From the fig. 59 (a), interconnect at device level, the core was glass rod with refractive index of 1.5 (Online) [50] and the cladding was air with refractive index of 1. But interconnects at the chip level will be looks like in fig. 59 (b) on-chip electrophotonic interconnect have not gaps to cause for optical loss. And the core will be silicon and cover or cladding will be silicon dioxide at chip level for both on-chip and chip-to-chip interconnections. With this fact for chip level interconnection, the waveguide will be fabricated from silicon with refractive index of 3.5 on the chip and surrounded cover (cladding) by silicon dioxide with refractive index 1.47 [19] and Waveguide (optical fiber) made of silicon and silicon dioxide is transparent at wavelength range from 1300 nm –to- 1550 nm [7]. Based on these things, silicon waveguide on chip level will have larger refractive index than the glass rod on what we have seen on experimental set up. And the cladding on chip level will have higher than the refractive index than the air on experimental set up. So light intensity on the electrophotonic interconnect will be confined much higher in a medium of higher refractive index as in fig.59 (b) on simulation at chip level than as fig.59 (a) on experimental set up at device level. Therefore, the future duty will be to proof the performance of integrated electrophotonic at chip level will higher than at device level using simulating software or other photonic equipments.

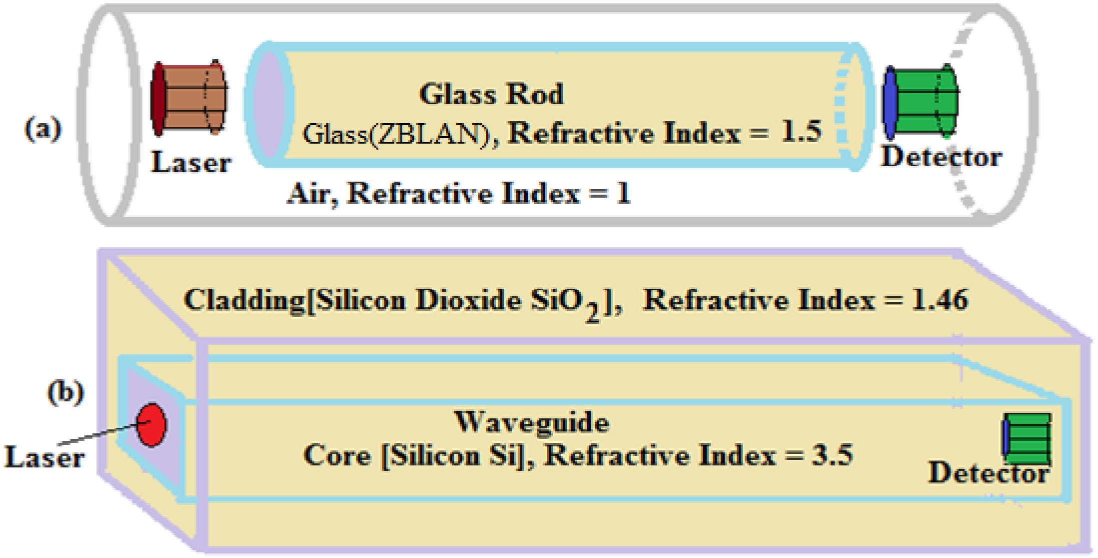


Figure 59 Interconnects (a) Experimental set up done at device level (b) for future to be done at chip level.

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