SIMULATION OF THREE-LAYER SOLID STATE MEMCAPACITOR

By

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Abstract

Memcapacitors are capacitors whose capacitance depends on the past states through which the system has evolved. The focus of this thesis is on the possible realization of a three-layer solid-state memory capacitive (memcapacitive) system. The functioning of this device is based on the slow polarization rate of a medium between plates of a regular capacitor. To achieve this goal, this work considers a three-layer structure embedded in a capacitor. The three layer structure is formed by metallic layers separated by an insulator so that non-linear electronic transport between the layers can occur. Unlike conventional capacitor, the capacitance of this device depends on the history of the system. Our calculation shows non-pinched hysteretic charge-voltage and capacitance-voltage curves, and both negative and diverging capacitance within certain ranges of the field. This property of memcapacitive system makes it a good candidate for non-volatile memory application.

Chapter 1

INTRODUCTION

1.1 Development of memory devices

Since the very first days of the mid-1960s, when the potential of metal-oxide semiconductor (MOS) technology to realize semiconductor memories with superior density and performance than would ever be achievable with the commonly used magnetic core memories became known, chip makers have thought of solutions to overcome the main drawback of the metal-oxide semiconductor (MOS) memory concept, that is, its intrinsic volatility. The first sound solutions to this problem, with applicability beyond the mere read-only memory (ROM) function, were the floating gate concept [1] and the metal-nitride-oxide-semiconductor (MNOS) memory device [2], both of which were proposed in 1967. A 1 Kbit UV-erasable programmable read-only memory (PROM) (EPROM) part, based on the floating gate concept, became readily available in 1971, shortly after 1 Kbit random access memories (RAM) came on the market. The ultimate solution - a genuine nonvolatile RAM that retains data without external power, can be read from or programmed like a static or dynamic RAM, and still achieve high-speed, high - density, and low - power consumption at an acceptable cost - remains unfeasible to this day. Yet tremendous progress has been made over the years in realizing the "alternative best" idea of a reliable, high-density, user-friendly reprogrammable ROM memory. Reprogrammable nonvolatile memories can be subdivided into the following classes:

1. UV-erasable programmable read-only memory (EPROM) and one-time programmable (OTP) devices.

2. Electrically erasable programmable read-only memory (EEPROM) memories, which can be further subdivided into full-feature electrically erasable programmable read-only memory (FF-EEPROMs) and Flash EEPROMs.

3. Nonvolatile RAM (NOVRAM), which combines the nonvolatility of electrically erasable programmable read-only memory (EEPROM) with the ease of use and fast programming characteristics of static RAM.

4. Ferroelectric RAM (FRAM).

Adding in-system reprogrammability to PROM memories (leading to FFEEPROMs and to Flash EEPROMs), however, yields increased system flexibility and opens a broad new range of applications such as intelligent controllers; self adaptive, reconfiguring, and remotely adjustable systems; programmable/adaptable logic; artificial intelligence; and numerous others [3]. The term Flash refers to the fact that the contents of the whole memory array, or of a memory block (sector), is erased in one step. In 1983, 16 Kbit electrically erasable programmable read-only memory (EEPROMs) based on both the metal-nitride-oxide-semiconductor (MNOS) and the floating gate concept were introduced, many analysts projected that EEPROMs would grow into a high-volume market and gradually even replace erasable programmable read-only memory (EPROM) as the standard program storage medium in microprocessor-controlled systems. They are at present the fastest growing MOS memory segment, and it is expected that they will eventually constitute the third largest segment behind dynamic random access memory (DRAM) and static random access memory (SRAM). The EEPROM market did not grow as previously predicted because of their high cost per bit as compared to EPROM, the lack of large-scale applications for full-featured EEPROMs, and the poorly understood reliability of these components. The reliability issues of EEPROMs and Flash memories have, however, recently been thoroughly investigated and are now much better known and

documented. In addition, recent lower pricing and increased performance of Flash memories have stirred new interest in these parts. New large-scale applications are emerging (i.e., memory cards, small, compact, and portable memories). These Flash EEPROMs were themselves developed in the late 1980s and introduced around 1990 when manufacturers were searching for nonvolatile devices that were still electrically erasable, but that could become nearly as cost effective as EPROMs. They combined the best concepts of EPROM and traditional EEPROM into a single transistor Flash EEPROM.

1.2 Circuit elements with memory: Memristors, Memcapacitors, and Meminductors

Circuit elements that store information without the need of a power source would represent a paradigm change in electronics, allowing for low-power computation and storage. In addition, if that information spans a continuous range of values analog computation may replace the present digital one. Such a concept is also likely to be at the origin of the workings of the human brain and possibly of many other mechanisms in living organisms so that such circuit elements may help us understand adaptive and spontaneous behavior, or even learning. A recent experimental demonstration of a nanoscale memory resistor (memristor for short) [4] has sparked numerous investigations in the area of materials and systems that show history-dependence in their current-voltage characteristics [5,6,7,8,9,10]. This has also led to the recent proposal and theoretical investigation of memcapacitors and meminductors, namely capacitors and inductors whose capacitance and inductance, respectively, depends on the past states through which the system has evolved [11]. Together with the memristor, the whole class of these memory-circuit elements promises new and unexplored functionalities in electronics, and the combination of these memory devices with their "standard" counterpart may find application in disparate areas of science and technology, including the study of neuromorphic circuits to simulate

biological processes [12].

This thesis work focuses on memcapacitors particularly on solid-state memcapacitors with three identical metal layers embedded in a parallel plate capacitor. Several systems are known to exhibit memcapacitive behaviour including vanadium dioxide metamaterials [7], nanoscale capacitors with interface traps or embedded nanocrystals [13,14,15,16], and elastic capacitors [17,18]. Though the numbers of experimentally identified memcapacitors are limited, memcapacitors have been simulated by electronic circuits and memcapacitive effects may also accompany memresistive effects in nano structures, since in many of them the morphology of conducting regions changes in time [4]. Moreover, memcapacitors can be simulated by electronic circuits [19]. However, the number of experimentally identified memcapacitive systems is still very limited. In addition, it would be of great importance to identify a mamcapacitive system that can be fabricated relatively easily, and is flexible enough to cover a wide range of capacitances. Here, we suggest a possible realization of such a system based on the slow polarization of a medium between regular capacitor plates. There are several physical mechanisms that can potentially provide a slowly polarisable medium. Examples include tunneling, activated drift of charged vacancies/impurities, slow ion penetration through a membrane, etc. This work will consider the tunneling mechanism and discuss a solid-state memcapacitive system consisting of metal layers embedded into a parallel-plate capacitor as schematically shown in Fig. 1.1.

In this realization, the internal metal layers together with the insulator material form a "metamaterial" characterized by a long polarization /depolarization time. The application of an external voltage to the capacitor leads to a charge redistribution between the embedded metal layers. The tunneling current between the layers depends almost exponentially on the applied voltage. This feature is important for the operation of the suggested device allowing for the "writing" of information (in the form of medium polarization) with high-voltage pulses, and "holding" such information when low/zero voltages are applied. The resulting memcapacitor exhibits not only hysteretic charge-voltage and

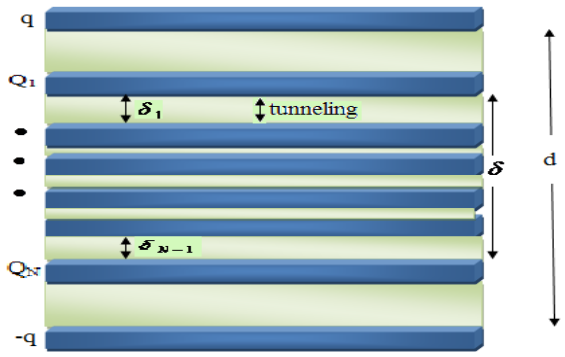


Figure 1.1: General scheme of a solid-state memcapacitor. A metamaterial medium consisting of N metal layers embedded into an insulator is inserted between the plates of a "regular" capacitor.

capacitance-voltage curves but also both negative and diverging capacitance within certain ranges of the field. Due to its simplicity and unusual capacitance features we thus expect it to find use in memory applications.

The rest of the work is organized as follows: In chapter two a three-layer metamaterial embedded between the regular plate capacitor is proposed as a model.The dynamics of its internal charges as well as its equivalent circuit are presented. Chapter three describes the methodology of the simulations and in the fourth chapter the results of the simulation is explained in detail. Finally summary and conclusion is given in chapter four.

1.3 Objective of the thesis

The main objectives of this thesis are:

1. To simulate the memory capacitive effect of a solid-state memcapacitor for a three metal layers embedded in a parallel plate capacitor.

2. To realize the possibility of making a Three-Layer solid state memory capacitor used in electronic circuits.

Chapter 2

SOLID STATE MEMCAPACITOR

This chapter describes the basic equations that are used to understand the properties of memcapacitors.

2.1 Memcapacitative systems

Circuit elements with memory are obtained from analyzing a circuit which has four fundamental variables which are charge, current, voltage, and magnetic flux. The four different variables lead to six different couple of variables: the time derivative of charge is related to current and the time derivative of magnetic flux is related to voltage, current and flux are related to inductance, charge is related to voltage by a capacitor, voltage and current are related by resistance, while magnetic flux and charge are related by memory resister. Quite generally, if x denotes a set of n-state variables describing the internal state of the system, $u(t)$ and $y(t)$ are any two complementary constitutive variables (i.e., current, charge, voltage, or flux) denoting input and output of the system, and g is a generalized response, we can define a general class of n^{th}-order u-controlled memory devices as those described by the following relations:

$$y(t) = g(\mathbf{x}, u, t)u(t) \tag{2.1.1}$$

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, u, t) \tag{2.1.2}$$

where **f** is a continuous n-dimensional vector function and we assume on physical grounds that, given an initial state $u(t = t_o)$ at time t_0, admits a unique solution.The generalization of the definition from Eqs. 2.1.1 and 2.1.2 yields port and state equations of current-controlled, voltage-controlled, charge-controlled and flux controlled systems of circuit elements. According to Eqs.2.1.1 and 2.1.2 the systems are of n^{th}-order, meaning that **x** is a vector containing n-state variables i.e $\mathbf{x} = (x_1, x_2, ..., x_n)$. Since my concern is only on memcapacitors based on Eqs. (2.1.1, 2.1.2) the model for a charge controlled memcapacitive system is expressed by the equations below

$$V_c(t) = C^{-1}(\mathbf{x}, q, t)q(t) \tag{2.1.3}$$

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, q, t) \tag{2.1.4}$$

where q(t) is the charge on the capacitor at time t, $V_c(t)$ is the applied voltage and C is the memcapacitance which depends on the state of the system and can vary in time.

2.2 Three-layer solid-state memcapacitive system

As shown in fig. 2.1 for a system of solid-state memcapacitor with three metal layers embedded in between the plates of a regular capacitor with separation 'd' and the three metal layers together with the insulation between them has a thickness of δ, in the simulation we assuming that the insulating material is the same as the one of regular capacitor and the memcapacitor is designed in such a way that there is no electron exchange between the external plates and those embedded (i.e a higher potential barrier is generated between the plates and the embedded metallic layers). The metallic layers together with the insulating material form a "metamaterial" characterized by long polarization /depolarization time and memcapacitive effect. As there is a higher potential barrier generated between the plates and the embedded metallic layers no electron exchange between them and the only electron exchange is between the metal layers via tunnelling that results the conservation of charge in the metamaterial. Consequently, the total internal charge

Figure 2.1: Three layer memcapacitor

is always zero: $\sum_{k-1}^{3} Q_k = 0$, where Q_k (t) is the charge on the internal metal layers at time t.

The application of external electric field leads to a charge redistribution between the embedded metal layers and results in the polarization of the metamaterial. Since the tunnelling current between the layers depend almost exponentially on the applied voltage, and this property is important for the operation of the memcapacitor for the writing of information in the form of polarization with high-voltage pulses and holding such information when low or zero voltages are applied. The polarization of the metamaterial develops an electric field between the layers in opposite to the electric field due to the plate charges, and thus the internal charges tend to decrease the voltage or equivalently to increase the capacitance. Since a charged plane creates a uniform electric field perpendicular to the plane with magnitude $E = \sigma/2\epsilon_o\epsilon_r$, where $\sigma = q/S$ is the surface (of area S) charge density, ϵ_o is the vacuum permittivity, and ϵ_r is the relative dielectric constant of the insulating material. Using this expression, we find that, in the structure shown in Fig. 1.1, the external plate voltage is given by:

$$V_C = 2dE_q + \delta E_{Q1} + [\delta - 2\delta_1]E_{Q2} + [\delta - 2(\delta_1 + \delta_2)]E_{Q3} + ... + [\delta - 2(\delta_1 + ... + \delta_{k-1})]E_{Qk} ... - \delta E_{QN} \tag{2.2.1}$$

For three-layer memcapacitor Eq. 2.2.1 can be expressed as

$$V_C = 2dE_q + \delta E_{Q1} + [\delta - 2\delta_1]E_{Q2} - \delta E_{Q3}, \tag{2.2.2}$$

where $E_q = q/2\epsilon_o\epsilon_r S$ is the electric field due to the charge q at the external plate and $E_k = Q_k/2\epsilon_o\epsilon_r S$ is the electric field due to the charge Q_k at the k^{th} embedded metal layer. Eq. 2.2.1 can also be written as follows

$$V_C = \frac{q}{C_o}[1 + \Delta\frac{Q_1}{2q} + (\Delta - 2\Delta_1)\frac{Q_2}{2q} + ... + (\Delta - 2\Delta_{k-1})\frac{Q_k}{2q}... - \Delta\frac{Q_N}{2q}] \tag{2.2.3}$$

where $\Delta = \delta/d, \Delta_i = \sum_{j=1}^{i}\delta_j/d, i = 1, 2, 3, ..., N-1, \delta_j$ is the spacing between consecutive metal layers, $\Delta_o = 0, C_o = \epsilon_o\epsilon_r S/d$ is the capacitance of the system without internal metal layers, Q_i is the charge on the i^{th} metal plate and q is the charge on the regular capacitor plates. For three-layer memcapacitor, Eq. 2.2.3 can also be expressed as

$$V_C = \frac{q}{C_o}[1 + \Delta\frac{Q_1}{2q} + (\Delta - 2\Delta_1)\frac{Q_2}{2q} - \Delta\frac{Q_3}{2q}] \tag{2.2.4}$$

The capacitance of the whole structure is also express as

$$C = \frac{q}{V_C} = \frac{2C_o}{2 + \sum_{i=1}^{N}[\Delta - 2\Delta_{i-1}]\frac{Q_i}{q}}. \tag{2.2.5}$$

For three-layer memcapacitor Eq. 2.2.5 can be expressed as,

$$C = \frac{2C_o}{2 + \Delta\frac{Q_1}{q} + (\Delta - 2\Delta_1)\frac{Q_2}{q} + (\Delta - 2\Delta_2)\frac{Q_3}{q}} \tag{2.2.6}$$

From Eq. 2.2.5/6 it is already clear that, unlike a conventional capacitor, there may be instants of time in which the denominator of Eq. 2.2.5/6 is zero while the numerator is finite. This may happen when the internal metal layers screen completely the external field, despite the presence of a finite charge q on the external capacitor plates. At these times one would then expect diverging values of capacitance. In addition, Eq. 2.2.5/6 does not enforce a positive capacitance. At certain instants of time the internal metal layers may over-screen the external field, resulting in a negative capacitance. It is interesting

to note that a hysteretic negative and diverging capacitance has been found also in ionic memcapacitors, namely nanopore membranes in an ionic solution subject to external time-dependent perturbations [20]. A negative capacitance has been experimentally observed in different solid-state systems [21,22,23], but not accompanied by hysteretic and diverging values of capacitance.

2.3 Description of the dynamics of the internal charges of the system

Charge dynamics is essentially determined by the distance between the layers and the potential energy barrier between adjacent layers. The potential difference between two consecutive (k and k+1) metal layers is defined by $V_k = -E_{k,k+1}\delta_k$, where $E_{k,k+1}$ is the electric field between two neighboring metal layers and obtained by summing the electric fields due to charges at all layers and at the external metal plates. Thus $E_{k,k+1}$ is obtained by;

$$E_{k,k+1} = -2E_q - E_1 - E_2 ... - E_k + E_{k+1} ... + E_N = \frac{-2q - (Q_1 + ... + Q_k) + (Q_{k+1} + ... + Q_N)}{2S\epsilon_o\epsilon_r} \tag{2.3.1}$$

The dynamics of the charge at a metal layer k is determined by the tunneling current flowing to and from that layer. Theoretically it is described by the equation below.

$$\frac{dQ_k}{dt} = I_{k-1,k} - I_{k,k+1}, \tag{2.3.2}$$

where $I_{k,k+1}$ is the tunneling electron current flowing from layer k to layer k + 1 (note that for the top and bottom layers(k=1, N), there is only one term on the right hand side of Eq. 2.3.2). By considering the layer charges Q_k as state variables, we immediately notice that Eq. 2.3.2 is similar to Eq. 2.1.4. This demonstrates that the system under consideration is indeed a charge-controlled memcapacitive system. If U is the potential barrier height between two adjacent metal layers, the tunneling current induced by the voltage difference V_k between the two can be calculated using the following expression

[24].

$$I_{k,k+1} = \frac{Se}{2\pi h\delta_k^2}[\alpha exp[-\frac{4\pi\delta_k\sqrt{2m}}{h}\sqrt{\alpha}] - \beta exp[-\frac{4\pi\delta_k\sqrt{2m}}{h}\beta]] \tag{2.3.3}$$

if $eV_k < U$ and

$$I_{k,k+1} = \frac{Se^3V_k^2}{4\pi hU\delta^{2_k}}[exp[\frac{-4\pi\delta_k\sqrt{m}U^{\frac{3}{2}}}{ehV_k}] - \gamma exp[\frac{-4\pi\delta_k\sqrt{m}U^{\frac{3}{2}}}{ehV_k}\gamma]] \tag{2.3.4}$$

if $eV_k > U$.

In the above equation $\alpha = (U - \frac{eV_k}{2})$, $\beta = U + \frac{eV_k}{2}$, $\gamma = 1 + \frac{2eV_k}{U}$, h is the Planck constant, S is the surface area of the capacitor, m is mass of an electron, and e is the charge of an electron. In the above equation, a strong increase in current with increase of V_k is clearly observed. This is an important property for the operation of the suggested memcapacitor.

2.4 Equivalent circuit model of solid-state three-layer memcapacitor

The memcapacitor can also be derived from the equivalent circuit model. In the equivalent circuit model each insulator spacing between adjacent metal layers (including capacitor plates) is represented by a separate capacitor as shown in figure 2.2 and to use non-linear resistors in order to mimic the electron tunneling between the layers and energy loss in the thermalization processes accompanying the tunneling. The top and bottom surfaces of each internal layer are considered as plates of adjacent circuit model's capacitors while the metallic material of the layer itself plays the role of the conductor connecting these capacitors. Fig. 2.2 shows the equivalent circuit of a three-layer memcapacitor. The circuit is composed by four capacitors connected in series.

The parameters of capacitors are determined by the usual parallel plate capacitor expression and related to the parameters of memcapacitor in the following way:

$$C_1 = \frac{\epsilon_o\epsilon_r S}{\frac{d-\delta}{2}} = \frac{2\epsilon_o\epsilon_r S}{d(1-\Delta)} = \frac{2C_o}{1-\Delta} \tag{2.4.1}$$

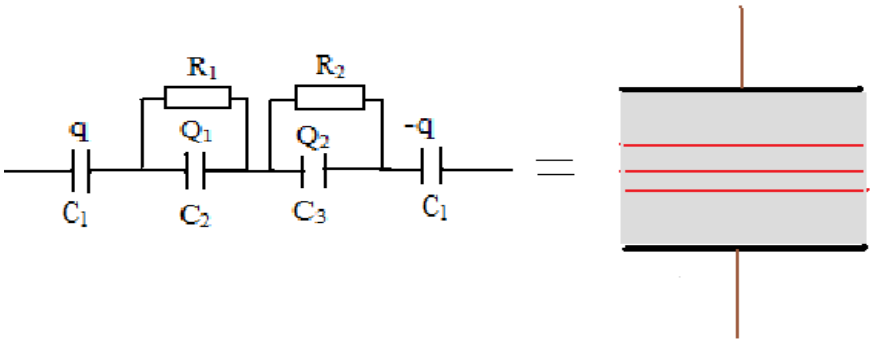


Figure 2.2: Equivalent circuit model of three-layer memcapacitor. Here, C_1, C_2 and C_3 are usual capacitors; R_1 and R_2 are a non-linear resistor.

$$C_2 = \frac{\epsilon_o \epsilon_r S}{\delta_1} = \frac{\epsilon_o \epsilon_r S}{\Delta_1 d} = \frac{C_o}{\Delta_1} \tag{2.4.2}$$

$$C_3 = \frac{\epsilon_o \epsilon_r S}{\delta_2} = \frac{\epsilon_o \epsilon_r S}{\Delta_2 d} = \frac{C_o}{\Delta_2} \tag{2.4.3}$$

Accordingly, the total voltage drop is given by

$$V_C = \frac{2q}{C_1} + \frac{Q_1}{C_2} + \frac{Q_2}{C_3} \tag{2.4.4}$$

By substituting Eqs. 2.4.1, 2.4.2, and 2.4.3 in equation 2.4.4, we obtain the total capacitance of the whole structure

$$C = \frac{C_0}{1 - \Delta + \frac{Q_1 \Delta_1}{q} + \frac{Q_2 \Delta_2}{q}} = \frac{C_o}{1 - \Delta + \sum_{i=1}^{N} \frac{Q_i \Delta_i}{q}} \tag{2.4.5}$$

One then immediately notices that Eq. (2.4.5) and Eq. (2.2.5) are exactly the same. From the equations of the memcapacitance (Eqs. 2.2.5 and 2.4.5) unlike conventional capacitor, there may be instant of time in which the capacitance of the whole structure,

C can be diverging when the electric field by the internal layers completely screen the electric field of the plates, despite of the presence of finite charge q on the outer plate of the capacitor and also C may be negative when the electric field of the internal layers over-screen the external electric field.

Chapter 3

METHODOLOGY

To simulate the memcapacitive effect of a three layer periodic and non-periodic memory capacitor we simplified and developed the dynamical equations for a three layer charge-controlled memcapacitor from the quite general model of a circuit with memory described by Eqs. 2.1.1 and 2.1.2. After we simplified and developed the dynamical equations for a three-layer solid state charge-controlled memory capacitor which are described by Eqs. 2.1.3, 2.3.2, 2.2.5 and 4.0.1 we put the appropriate parameters such as potential energy barrier height and separation between the layers. Then, we developed the mathematica code that solves Eq. 2.2.5 together with Eqs. 2.1.3, 2.3.2, and 4.0.1 and we analyzed, compared and contrasted the result with each other (non-periodic and periodic) and with previously done two-layer solid-state memcapacitor [26]. The program code is given in the appendix and the input parameters are given below:

Parameters with their SI unit

The relative dielectric constant of the insulating material, $\epsilon_r = 7$;

$\epsilon = \epsilon_r(8.85x10^{12})$;

Separation b/n external plate, d $=1x10^{-7}$;

Surface area of the plate, $a = 1x10^{-4}$;

capacitance of the system without internal metal layers, $C_o = a\epsilon/d$;

$\Delta = 2/3$;

$\delta = \Delta$d;

Sinusoidal voltage, $V[t] = 7.7 \sin 2\pi f t$;

Frequency, f=10000;

Resister, R=1Ω;

charge on an electron, e = $1.6x(10^{-19})$;

Planck's constant, h =$6.6x(10^{-34})$;

mass of an electron, m = $9x(10^{-31})$;

potential barrier height between two adjacent metal layers, U = (1/3)e;

period, $T = 5/f$;

number of layer embedded between external plates, n = 3;

Chapter 4

RESULTS AND DISCUSSION

This section explains results of numerical simulations obtained for the case of a sinusoidal voltage $V(t) = V_0 \sin(2\pi f t)$ of amplitude V_0 and frequency f applied to a memcapacitor C connected in series with a resistor R. Such a circuit is described by the equation

$$V(t) = R\frac{dq}{dt} + \frac{q}{C}, \tag{4.0.1}$$

where, for C, we use Eq. 2.2.5.

Eq. 4.0.1 is solved numerically together with Eq. 2.3.2 describing the internal charge dynamics. In this simulations, a small value of $R = 1\Omega$ is selected so that the voltage drop on the resistor is negligible.

The simplest system exhibiting polarization memory next to a two-layer memcapacitor is a three-layer memcapacitor. The only interesting difference between two-layer memcapacitor embedded periodically between the regular plates of a parallel plate capacitor and three-layer memcapacitor embedded non-periodically between the regular plates of a parallel plate capacitor as shown in Fig 4.1 (a) and Fig 4.2 is that in the case of three-layer memcapacitor, a richer internal charge dynamics can be observed. Charge dynamics is essentially determined by the distance between the layers and the potential energy barrier between adjacent layers. In Fig. 4.1 we illustrate simulation results of three-layer memcapacitor embedded non-periodically between the regular plates of a parallel plate capacitor. Starting at the zero-charge state, the sinusoidal applied voltage induces elec-

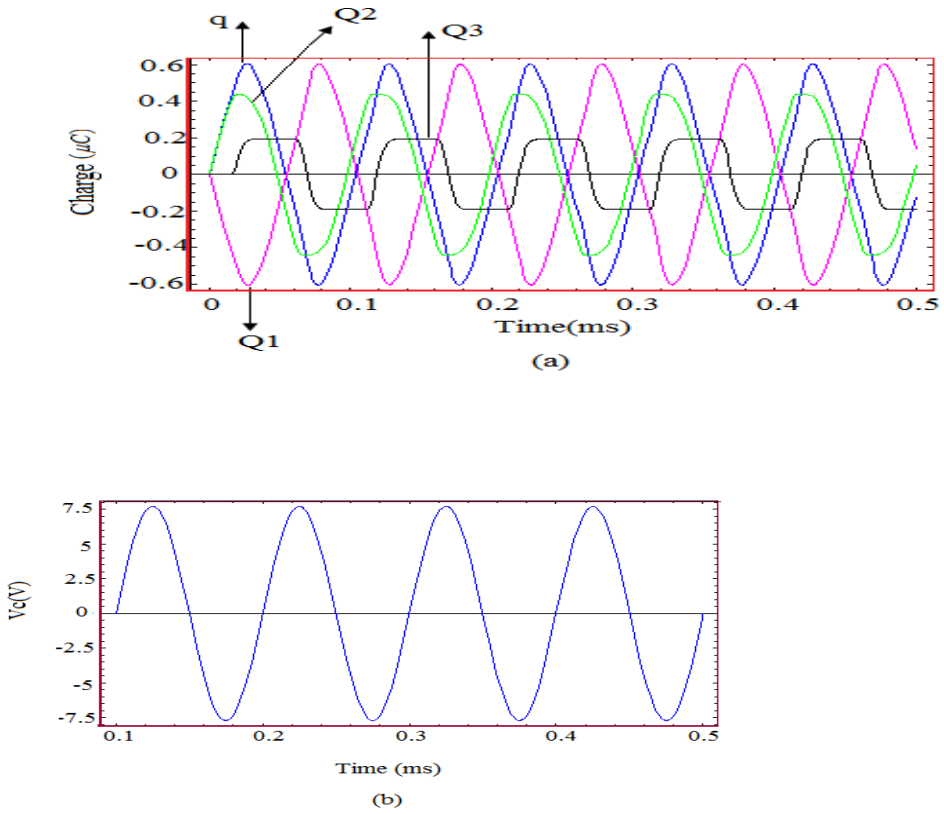


Figure 4.1: Simulation of *three-layer* memcapacitor with non-periodically positioned internal layers of a) the charge on internal metallic layers and memcapacitor plates as a function of time t b) Voltage on memcapacitors,Vc, as a function of time t. These plots were obtained using the parameter values V_0=7.7V, f=10kHz, d=100nm, a=$10^{-4}m^2$, ϵ_r=7.0, U=0.33eV, δ=66.6nm, R=1Ω, $\delta_1 = 0.047619\delta$, $\delta_2 = 0.952381\delta$

tron tunneling between the internal metal layers resulting in non-zero charges Q_1, Q_2, and Q_3. As it is shown in Fig. 4.1 positive half periods of V induce negative Q_1, positive Q_2 and at a certain time t, Q_3 close to zero and then induce positive Q_3 charges. In turn, these cause a screening electric field opposite to the electric field of plate charges. In Fig. 4.3 we illustrate simulation results of three-layer memcapacitor embedded periodically between the regular plates of a parallel plate capacitor. As it is shown in Fig. 4.3 positive half periods of V induce negative Q_1, and positive Q_3 charges but concerning the charge on the second layer, it is essentially close to zero. These types of devices is explained by

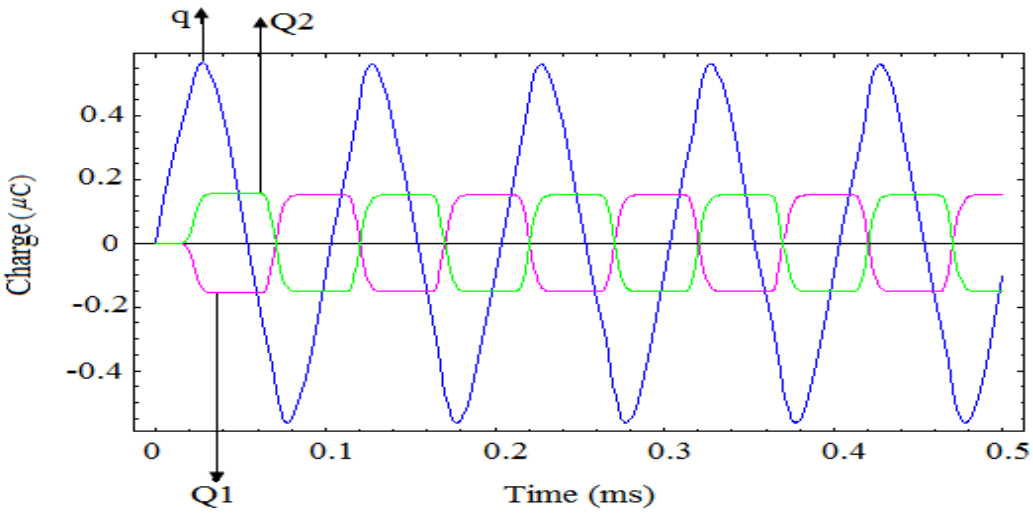


Figure 4.2: Simulation of two-layer memcapacitor with periodically positioned internal layers. The charge on internal metallic layers and memcapacitor plates as a function of time t. These plots were obtained using the parameter values V_0=7.7V, f=10kHz, d=100nm, δ= 66.6nm, $a = 10^{-4}m^2$, ϵ_r=7.0, U =0.33eV, R=1Ω [26].

a tendency of maximum charge separation [26].

It is interesting that on the charge - voltage plot (Fig. 4.4), q versus V_C forms a non-pinched hysteresis loop. This is a quite unusual feature of a memory device, especially, in view of the fact that, at the present time, only memristive devices exhibiting pinched hysteresis loops have been observed experimentally. Physically, it is clear that when an internal polarization in the memcapacitor is present and the plate charge is zero (q = 0), the internal polarization creates a non-zero voltage drop on the device $V_C \neq 0$. Alternatively, this voltage drop can be compensated by plate charges, but then we get $V_C = 0$ at $q \neq 0$.

This explains why the curve does not pass through the (0,0) point. The corresponding capacitance hysteresis is shown in Fig. 4.5. As expected, we find both negative and

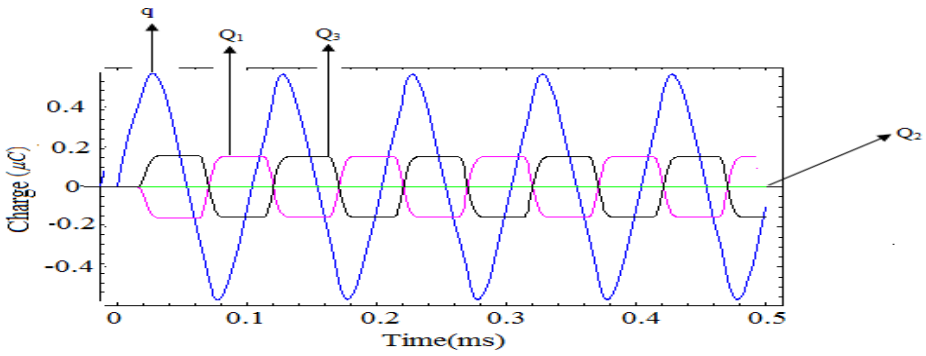


Figure 4.3: Simulation of three-layer memcapacitor with periodically positioned internal layers of the charge on internal metallic layers and memcapacitor plates as a function of time t. This plots were obtained using the parameter values V_0=7.7V, f=10kHz, d=100nm, a=$10^{-4}m^2$, ϵ_r=7.0, U=0.33eV, δ=66.6nm, R=1Ω, $\delta_1 = \delta_2 = 0.5\delta$

diverging capacitance values. In the vicinity of $V_C = 0$, the capacitance changes from $+\infty$ to $-\infty$ at both sweep directions. One can also see that the capacitance hysteresis and the added/removed energy of three-layer memcapacitor embedded non-periodically between the regular plates of a parallel plate capacitor (Fig. 4.5 (a) and Fig. 4.7, respectively) are similar to those of the two-layer and three-layer memcapacitor embedded periodically between the regular plates of a parallel plate capacitor as shown in Fig. 4.5 (b) and Fig. 4.6.

Next, we consider the added/removed energy to/from the capacitor which is defined as

$$U_C = \int_0^t V_C(\tau) I(\tau) d\tau. \tag{4.0.2}$$

From Fig. 4.7 it is clear that the present solid-state memcapacitor operates as a dissipative device since the amount of added energy is on average larger than the amount of removed energy (resulting in positive values of U_C at all times). This occurs because the electron tunneling between internal layers is accompanied by energy dissipated in thermalization processes due to the different electrochemical potential energies of metal

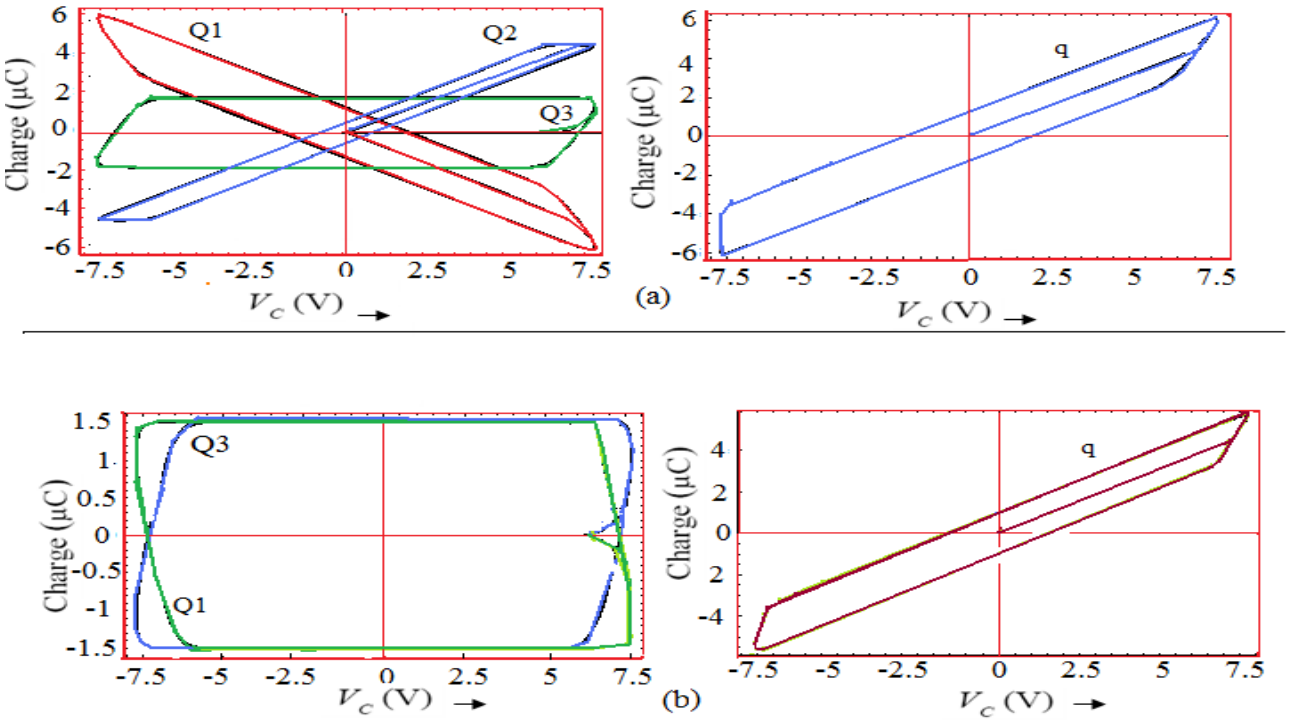
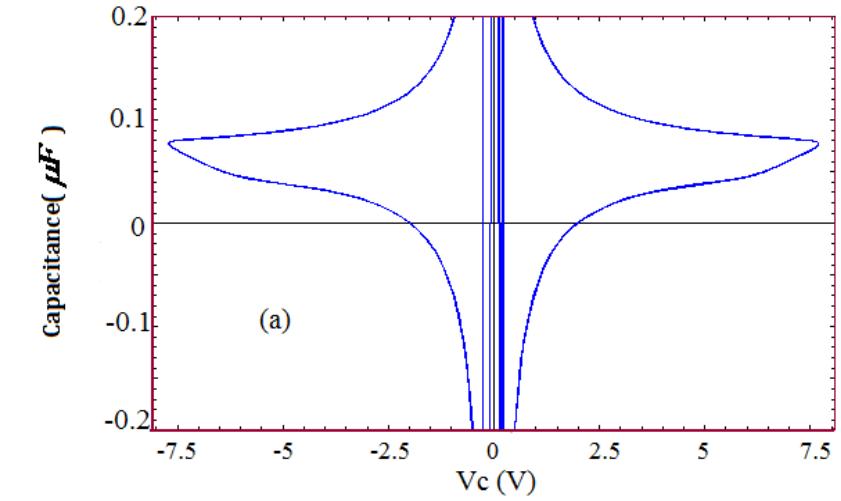


Figure 4.4: Simulation of three-layer memcapacitor with (a) non-periodically positioned internal layers, and (b) periodically positioned internal layers of charge-voltage plot. Plot (a) were obtained using the parameter values as fig. 4.1 and plot (b) were obtained using the parameter values as Fig. 4.3.

layers. In addition, in a real device we cannot exclude the phenomenon of local heating that would also contribute to dissipation of energy [25].

Finally, the frequency behavior of the charge-voltage hysteresis loop is shown in Fig. 4.8. It is clearly seen that the hysteresis shrinks at higher frequencies. This is a typical behavior of memory devices [8] related to the fact that at high frequencies the internal degrees of freedom of a memory device do not have enough time to respond to the external perturbation. Similarly, with increasing frequency, we have observed a decrease in capacitance hysteresis as well as in the rate of energy dissipation.



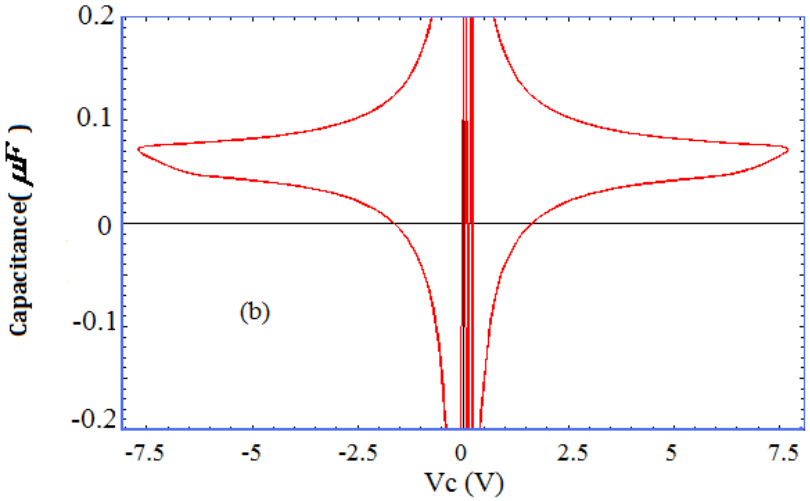


Figure 4.5: Simulation of three-layer memcapacitor with a) non-periodically positioned internal layers, and (b) periodically positioned internal layers of capacitance-voltage plot. Plot (a) were obtained using the parameter values as Fig. 4.1 and plot (b) were obtained using the parameter values as Fig. 4.3.

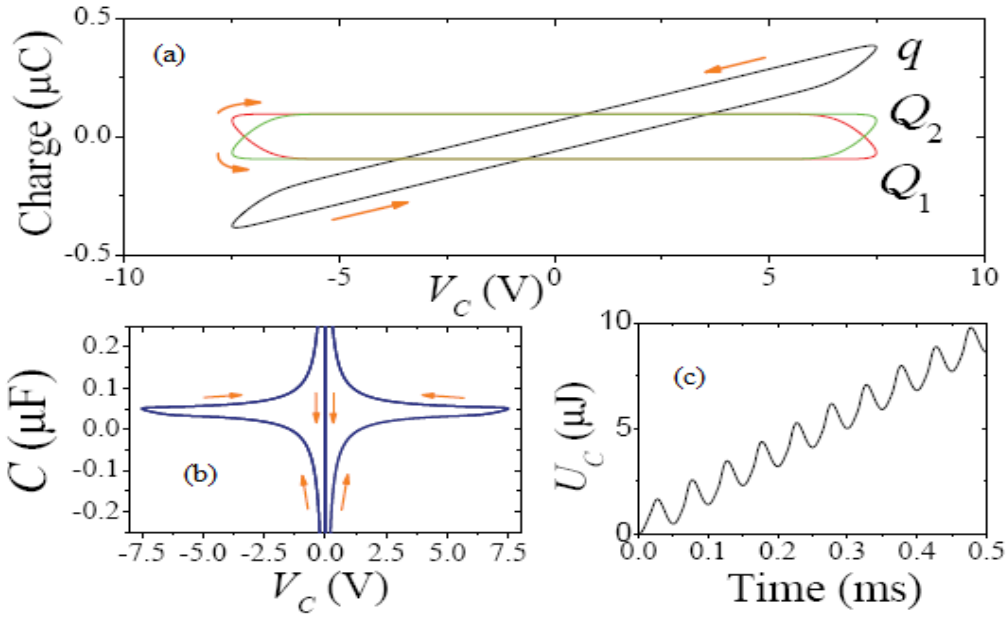


Figure 4.6: Simulation of two-layer memcapacitor with periodically positioned internal layers of (a) charge-voltage, (b)capacitance-voltage (c) add/removed energy as a function of time plots [26]. These plots were obtained using the parameter values as Fig. 4.2

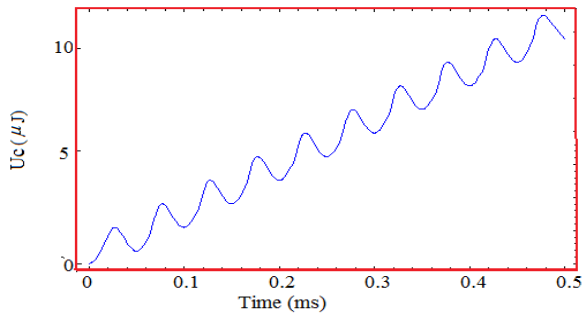


Figure 4.7: Simulation of three-layer memcapacitor with non-periodically positioned internal layers of the Added/removed energy as a function of time. These plots were obtained using the parameter values as Fig. 4.1

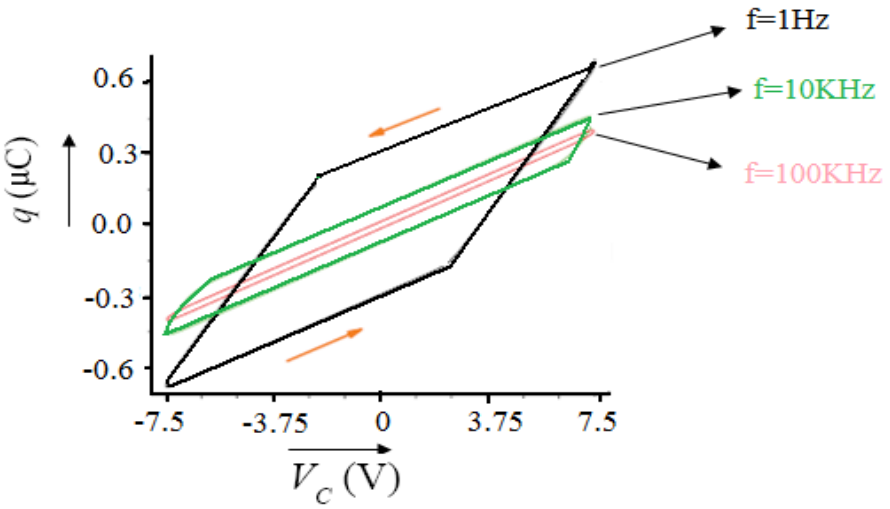


Figure 4.8: Charge-voltage plot at different applied voltage frequencies f . The decrease of the hysteresis at higher frequencies is a signature of memcapacitors[8] . The calculation and device parameters are as in Fig. 4.1

Chapter 5

SUMMARY AND CONCLUSION

5.1 Summary

In summary, this work has suggested and analyzed a solid-state memcapacitor made of a three-layer structure embedded in a capacitor. An interesting difference can be observed between two-layer memcapacitor embedded periodically between the regular plates of a parallel plate capacitor and three-layer memcapacitor embedded non-periodically between the regular plates of a parallel plate capacitor as shown in Fig 4.1 and Fig 4.2. Three-layer memcapacitor has a richer internal charge dynamics than the two-layer memcapacitor. From the above result we conclude that a richer charge dynamics can be observed by inserting additional layers in between the layers.

It is interesting that on the charge - voltage plot (Fig. 4.3), q versus V_C forms a non-pinched hysteresis loop. This is a quite unusual feature of a memory device. The resulting system has note-worthy features, such a frequency-dependent hysteresis under an ac-voltage, diverging and negative capacitance. These feature emerge due to the slow polarizability of the internal layers structure as a consequence of electron tunneling between the internal metal layers. This gives rise to both complete screening of the field due to the external metal plates - giving rise to diverging capacitances - and over-screening of the same field leading to negative capacitances. Clearly, when combined to an external circuit with finite capacitance, the capacitance divergencies of the proposed

solid-state capacitor would be cut off by the external circuit. Nonetheless, both the information stored in this memcapacitor in a continuous fashion (analog operation) and its negative capacitance in a certain range of the external field, may find useful applications in electronics.

This work has also shown the equivalent circuit model for this memcapacitor based on a combination of regular capacitors and non-linear resistors. This analogy could be useful both in actual calculations with circuit simulators, or in experiments with electronic circuits to reproduce memcapacitive features.

5.2 Conclusion

From our simulation result we conclude that the three-layer memcapacitor is better than the two-layer memcapacitive system. Which indicates that a multi-layer memcapacitor is a better memory device than small number of layer of memcapacitor and the simulation result of three-layer memcapacitor shows the simillar pattern as the multi-layer memcapacitor [26] so that it is useful to mimic the properties of a multi-layer memcapacitor using the three-layer memcapacitor.

Finally, our simulation result shows the possibility of realizing a three-layer solid-state memcapacitor by growing three-layer metamaterial between the plates of a regular parallel plate capacitor.

More generally, since memcapacitors are quite recent findings it is believed that they would have unexplored functionalities in science and technology. we hope this work will be a good background for those who are motivated for more experimental and theoretical studies in this direction.

Appendix

All simulations in this work is calculated by the software Mathematica as given below

(*[VARIABLES, TIMES ...]*)

$Table[\delta\delta[k] = 1, k, 1, n-1];$

$\delta\delta[1] = 0.05;$

total $=\sum_{l=1}^{n-1} \delta\delta[1]$

Table=$[R\delta[k] = \frac{\delta\delta[k]}{total}$, [k, 1, n - 1]

Table=$(*[R\delta[k] = \frac{1}{n-1}$, [k, 1, n - 1]*)

$\Lambda[0] = 0;$

Table$\Lambda[k]= \delta \sum_{l=1}^{k} R\delta[1], (k, 1, n-1)];$

variables=Flatten$[q[t], Table[Q[k, t], (k, n)]]$

$Table[Voltage[k] = \frac{\Delta R\delta[k]}{2c_o}(2q[t] + \sum_{m=1}^{k} Q[m, t] - \sum_{m=k+1}^{n} Q[m, t]), (k, 1, n-1)];$

$i[0, t] = 0;$

$i[n, t]= 0;$

$j_1[k, v]=\frac{ea}{2\pi h\delta^2 R\delta[k]^2}\ ((V_o-\frac{ev}{2})Exp[-\frac{4\pi\sqrt{2m}\delta R\delta[k]}{h}\sqrt{V_o-\frac{ev}{2}}]-(U-\frac{ev}{2})Exp[-\frac{4\pi\sqrt{2m}\delta R\delta[k]}{h}\sqrt{U+\frac{ev}{2}}])$

$j_2[k, v]=\frac{ae^3 vAbs[v]}{4\pi hU\delta^2 R\delta[k]^2}(Exp[-\frac{4\pi\sqrt{m}\delta R\delta[k]U^{\frac{3}{2}}}{heAbs[v]}])-(1+\frac{2eAbs[v]}{U})Exp[-\frac{4\pi\sqrt{m}\delta R\delta[k]U^{\frac{3}{2}}}{heAbs[v]}(1+\frac{2eAbs[v]}{U})]$

$ii[k, v]= UnitStape[v](j_1[k, v](1 - UnitStape[v - U/e]) + j_2[k, v]UnitStape[v - U/e]$

$+UnitStape[-v](j_1[k, v]UnitStape[v + U/e] + j_2[k, v](1 - UnitStape[v + U/e]))$

$Table[i[k, t] = ii[k, Voltage[k]], (k, 1, n-1)];$

$Plot[ii[1, x]/a, (x, -1.5, 1.5), PlotRange \to All, PlotStyle \to Thick]$

==========

(*__DYNAMICAL SYSTEM (CHARGES AND CAPACITANCE)__*)

DEquation = Flatten[q'[t]== $\frac{V[t]}{R} - \frac{\sum_{k=1}^{n}(\Delta - 2\Lambda[k-1])Q[k,t]+2q[t]}{2RC_o}), q(0) == 10^{-20}$,

Table[(D[Q[m, t], t] == -i[m, t] + i[m - 1, t], Q[m, 0] == 0), (m, n)]] ,Simplify;

qq = $NDSolve[DEquation, variables, (t, 0, T), MaxSteps \rightarrow 20000, AccuracyGoal \rightarrow$ 20];

$Plot[Evaluate[[variables, 10^{-12}V[t]]/.qq], (t, 0, T), PlotRange \rightarrow All]$

$(*TotalQ = \sum_{k=1}^{n} Q[k, t];$

$plot[Evaluate[TotalQ/.qq], (t, 0.T)]*)$

$C = \frac{2C_0}{2+\sum_{k=1}^{n}(\Delta - 2\Lambda[k-1])\frac{Q[k,t]}{q[t]}};$

$(*Plot[Evaluate[(c, 10^{-}10V[t])/.qq], (t, 0, T), PlotRange- > (-5x10^{-9}, 5x10^{9}), PlotStyle- > Thick]*)$

$(*Plot[Evaluate[(Q[1, t] + Q[2, t] + Q[3, t])//.qq], (t, 0, T)]*)$

==========

(*__PHASE DIAGRAMS__*)

$V_C = \frac{q[t]}{C};$

$ParametricPlot[Evaluate[(VC, 10^8 c)/.qq], (t, 1/f, T),\ PlotRange \rightarrow (All, (-15, 15)),$

$PlotStyle \rightarrow Thick]$

$(*Show[Table[ParametricPlot[Evaluate[(VC, 10^9 Q[i, t])/.qq], (t, 0, T), PlotRange \rightarrow (All, All)], (i, 1, n)]*)$

$Current = \frac{V[t]}{R} - \frac{\sum_{k=1}^{n}(\Delta - 2\Lambda[k-1])Q[k,t]+2q[t]}{2RC_o};$

$Plot[Evaluate[Current/.qq], (t, 0, T), PlotRange \rightarrow All]$

$(*ParametricPlot[Evaluate[(VC, 10^8 Current)/.qq], (t, 0, T), PlotRange \rightarrow (All, (-20, 20))]*)$

$ParametricPlot[Evaluate[(VC, 10^{11} q[t])/.qq], (t, 1/f, T), PlotRange \rightarrow (All, All), PlotStyle \rightarrow Thick]$

$(*Plot[NIntegrate[Evaluate[V_C Current/.qq], (t, 0, a)], (a, 0, T), PlotStyle \rightarrow Thick]*)$

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Declaration

This thesis is my original work, has not been presented for a degree in any other University and that all the sources of material used for the thesis have been dully acknowledged.

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Place and time of submission: Addis Ababa University, June 2010

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